Y.Sun

**PWM Controller of High-performance Current Mode**

***Product Specification***

## GENERAL DESCRIPTION

The YS2263 is a highly integrated low cost current mode PWM controller, which is ideal for small power current mode of offline AC-DC fly-back converter applications. Making use of external resistors, the IC changes the operating frequency and automatically enters the PWM (Burst Mode) under light-load/zero-load conditions. This can minimize standby power consumption and achieve power-saving functions. With a very low start-up current, the YS2263 could use a large value start-up resistor (2Mohms). Built-in synchronized slope compensation enhances the stability of the system and avoids sub-harmonic oscillation. Dynamic peak current limiting circuit minimizes output power change caused by delay time of the system over a universal AC input range. Leading blanking circuit on current sense input could remove the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. Cycle-by-Cycle current

limiting ensures safe operation even during short-circuit. Excellent EMI performance is achieved built-in soft start with 1.2mS, soft driver and frequency jitter. The YS2263 offers perfect protection like OVP (Over Voltage Protection) 、OLP (Over Load Protection) 、Power Limiting Protection and OCP (Over current protection). The YS2263 output driver is soft clamped to maximum H18V to protect the power MOSFET. YS2263 is offered in SOT-23-6L, SOP-8 and DIP-8 packages.

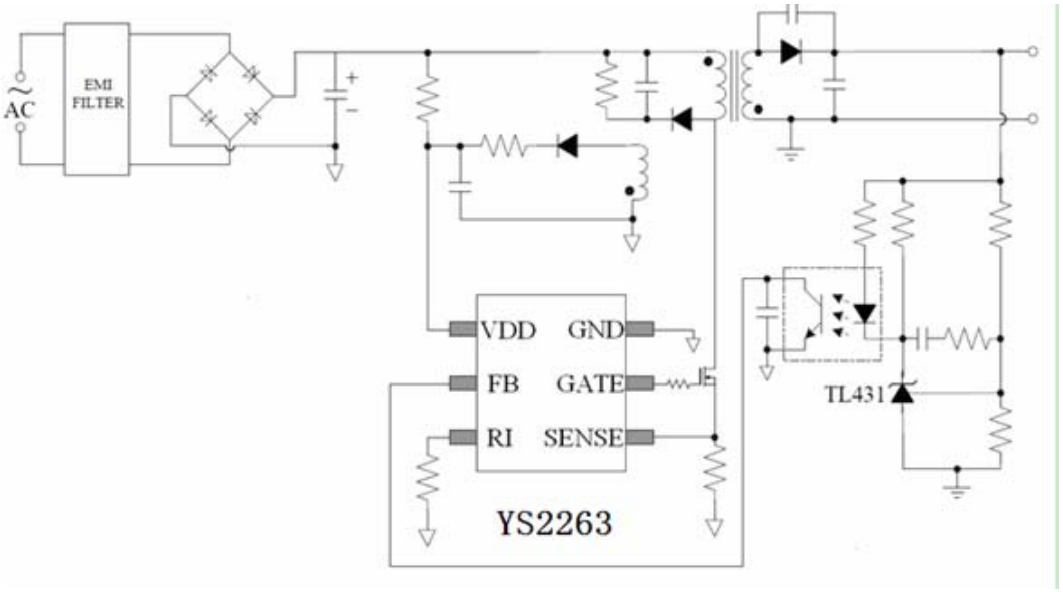
## FEATURES

- Low Cost, PWM (Burst Mode)
- Low Start-up Current (typical 3μA)
- Low Operating Current (typical 1.4mA)
- Current Mode Operation
- Built-in Synchronized Slope Compensation
- Built-in Frequency jitter for better EMI Signature
- Totem-Pole output driver in Soft-Start Switching
- Programmable PWM Frequency
- Audio Noise Free Operation
- Leading edge Blanking on Sense input
- Constant output power limiting for universal AC Input Range
- SOT-23-6L 、SOP8 and DIP-8 Pb-Free Packaging
- Compatible with SG6848 (2263) /SG5848/LD7535(7550)
- / OB2262 (2263)/RT7730 (RT7731)
- Complete Protection with
  - Soft Clamped GATE output voltage 18V
  - VDD over voltage protect 28V
  - Cycle-by-cycle current limiting
  - Power Limiting Protection
  - Under Voltage Lockout (UVLO)
  - Output OLP (Over Load Protection)
  - High-Voltage CMOS Process with ESD

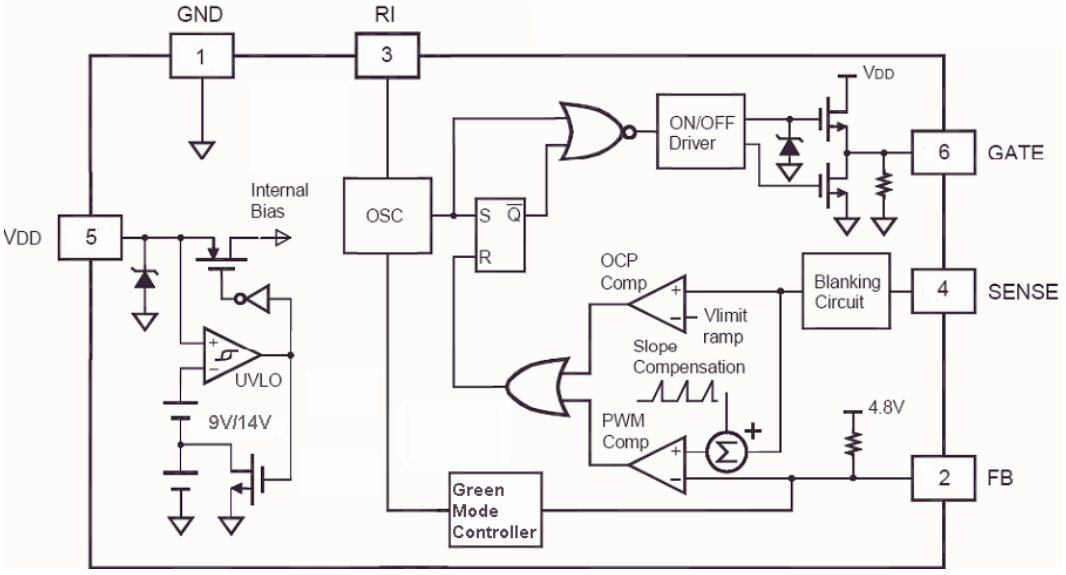
## APPLICATIONS

- Switching AC/DC Adaptor
- Battery Charger
- Open Frame Switching Power Supply
- Standby Power Supplies
- Set-Top Box Power Supplies

## TYPICAL APPLICATION



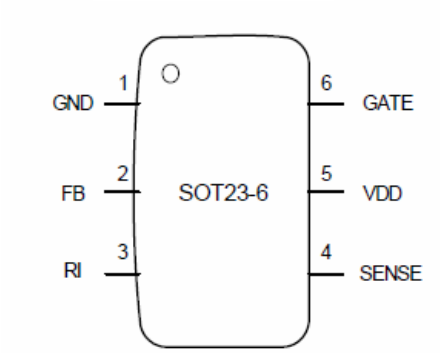

## BLOCK DIAGRAM

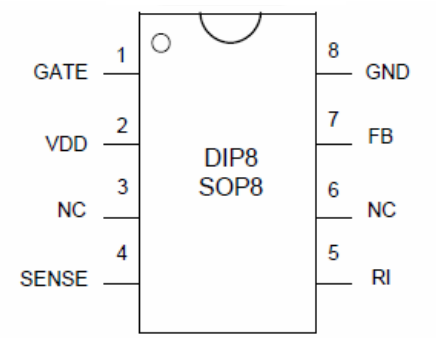


## GENERAL INFORMATION

### Pin Configuration

The YS2263 is offered in SOT23-6L, SOP8 & DIP8 package as shown below.




### TERMINAL ASSIGNMENTS

| Pin No. | Symbol SOT23-6/DIP-8 | Description |
|---|---|---|
| Gate | 6/1 | Totem-pole output to drive the external power MOSFET. which is internally clamped below 18V |
| VDD | 5/2 | Power Supply The internal protection circuit disables PWM output if VDD is over voltage |
| NC | /3 | NC Pin |
| Sense | 4/4 | Current sense pin, a resistor connects to sense the MOSFET current |
| RI | 3/5 | This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency. |
| NC | /6 | NC Pin |
| FB | 2/7 | Voltage feedback pin. Output current of this pin could controls the PWM duty cycle, If FB voltage exceeds the threshold; the internal protection circuit disables PWM output. |
| GND | 1/8 | GND Pin |

**Absolute Maximum Ratings**

| symbol | parameter | value | unit |
|---|---|---|---|
| VDD | DC supply voltage | 30 | V |
| $V_{FB}$ | FB Pin input voltage | -0.3 — 7 | V |
| $V_{SENSE}$ | SENSE Pin input voltage | -0.3 — 7 | V |
| $V_{RI}$ | RI Pin input voltage | -0.3 — 7 | V |
| $T_J$ | Operation Junction Temperature | -20 — 150 | ℃ |
| $T_{STG}$ | Storage Temperature | -55 — 160 | ℃ |
| $V_{CV}$ | VDD clamp voltage | 28 | V |
| $V_{CC}$ | VDD DC clamp current | 10 | mA |

**ELECTRICAL CHARACTERISTICS**

(TA = 25C, VDD=VDDG=16V, if not otherwise noted)

| Supply Voltage (VDD) | | | | | | |
|---|---|---|---|---|---|---|
| **symbol** | **parameter** | **Test condition** | **Min** | **Typ** | **Max** | **Unit** |
| VDD_OP | Operation voltage | | | | 30 | V |
| UVLO_ON | Turn on threshold Voltage | | 13 | 14 | 15 | V |
| UVLO_OFF | Turn-off threshold Voltage | | 8 | 9 | 10 | V |
| I_VDD_ST | Start up current | VDD=12V,RI=100K | | 3 | 20 | uA |
| I_VDD_OP | Operation current | VDD=16V,RI=100K,$V_{FB}$=3V, GATE with 1nF to GND | | 1.4 | | mA |
| VDD_Clamp | VDD Zener ClampVoltage | I(VDD)=10mA | | 28 | | V |

| Feedback Input Section | | | | | | |
|---|---|---|---|---|---|---|
| **symbol** | **parameter** | **Test condition** | **Min** | **Typ** | **Max** | **Unit** |
| A_PWM | PWM input gain | | | 2 | | |
| $V_{FB\_th\_L}$ | Zero duty cycle FB threshold | | | | 0.75 | |
| $V_{FB}$_Open | $V_{FB}$ Open Loop Voltage | | | 4.8 | | V |
| $I_{FB}$_Short | FB pin short current | | | 0.8 | | mA |
| $V_{TH}$_PL | Power limit FB Threshold | | | 3.7 | | V |
| $T_D$_PL | Power limit De-bounce | | | 35 | | ms |
| $Z_{FB}$_IN | Input Impedance | | | 6 | | kΩ |
| Max_Duty | Maximum duty cycle | | | 75 | | % |

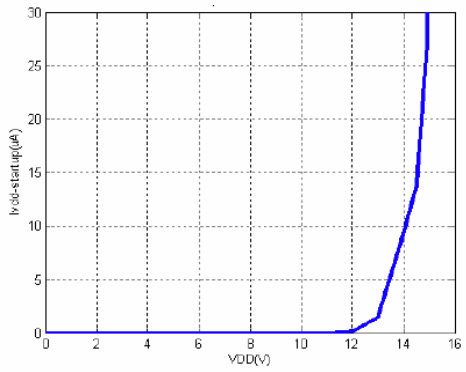
| Current Sense Section | | | | | | |
|---|---|---|---|---|---|---|
| **symbol** | **parameter** | **Test condition** | **Min** | **Typ** | **Max** | **Unit** |
| TLEB | Leading-edge Blanking Time | | | 300 | | ns |
| $Z_{sense}$ | Input impedance | | | 40 | | kΩ |
| $T_D$_OC | OCP control delay | | | 75 | | ns |
| $T_{TH}$_OC | OCP threshold | | 0.70 | 0.75 | 0.80 | V |

| Oscillator Section | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **parameter** | **Test condition** | **Min** | **Typ** | **Max** | **Unit** |
| Fosc | Frequency | Oscillation @RI=100K,CS=0 | 45 | 65 | 85 | KHz |
| Fosc_BM | Burst mode Frequency | Oscillation @RI=100K,CS=0 | | 22 | | KHz |
| Δf_Temp | Freq.var. vs.Temp.Deviation | Temp = (-20℃to 100℃) | | 5 | | % |
| Δf_VDD | Freq. variation vs. VDD | VDD = 12 - 25V | | 5 | | % |
| V_RI_Open | RI open Load Voltage | | | 2 | | V |
| RI_Range | RI pin Resistor Value | | 50 | 100 | 150 | kΩ |
| $F_{JITTER}$ | Frequency jitter | RI=100Kohm | -3 | | 3 | % |

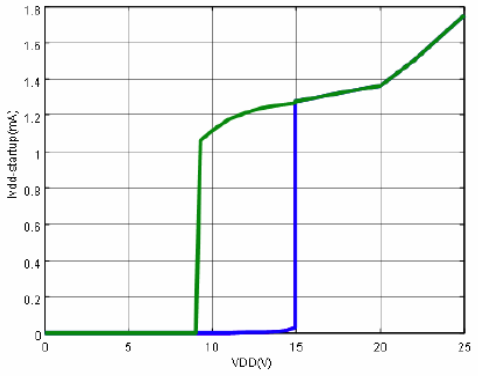
| GATE Output Section | | | | | | |
|---|---|---|---|---|---|---|
| **symbol** | **parameter** | **Test condition** | **Min** | **Typ** | **Max** | **Unit** |
| VOL | Output voltage Low | VDD = 16V, Io = -20mA | | | 0.8 | V |
| VOH | Output voltage high | VDD = 16V, Io = 20mA | 10 | | | V |
| VClamp | Output clamp voltage | | | 18 | | V |
| Tr | Rising time | VDD = 16V, CL = 1nF | | 220 | | ns |
| Tf | Falling time | VDD = 16V, CL = 1nF | | 70 | | ns |

## CHARACTERIZATION PLOTS

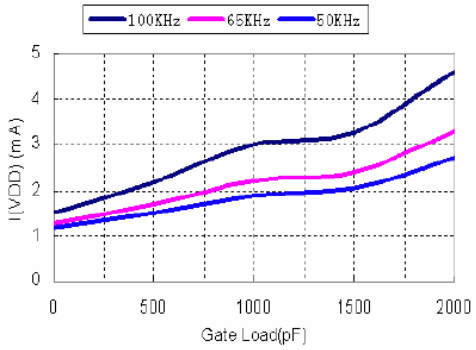
(The characteristic graphs are normalized at Ta=25℃)



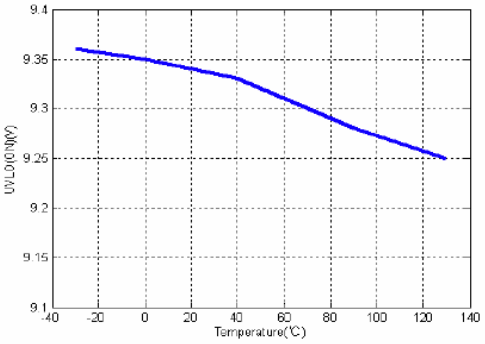

Start Current Vs VDD Voltage



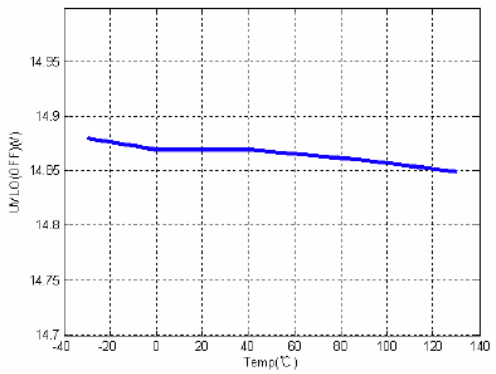

UVLO Voltage& Operation Current



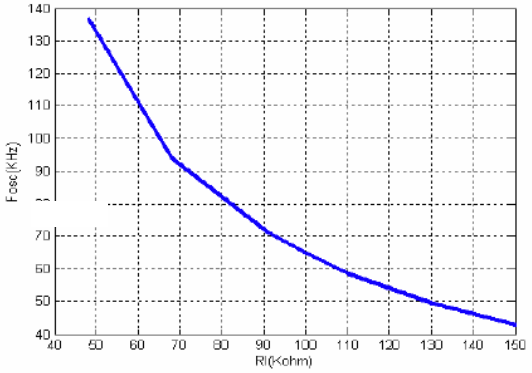

Operation Current VS Load




UVLO (On) Voltage VS Temp



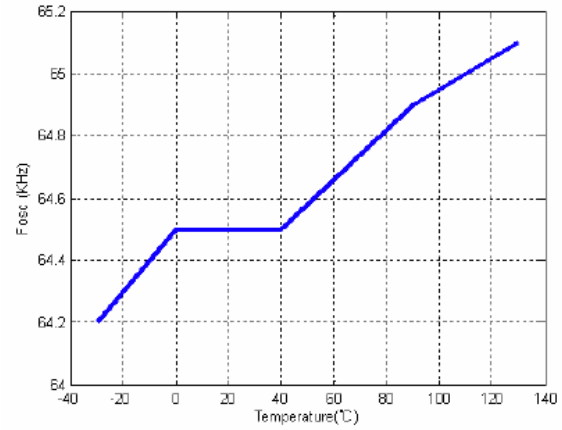

UVLO (Off) Voltage VS Temp




Operation Frequency VS RI

## CHARACTERIZATION PLOTS

(The characteristic graphs are normalized at Ta=25℃)




Operation Frequency VS Temp

## OPERATION DESCRIPTION

- **Current Mode**

Compared to voltage mode control, current mode control has a current feedback loop. When the voltage of the Sense resistor peak current of the primary winding reaches the internal setting value VTH, the register resets and the power MOSFET cuts off. So, to detect and modulate the peak current cycle-by-cycle could control the output of the power supply. The current feedback has a good linear modulation rate and a fast input and output dynamic impact, and avoid the pole that the output filter inductance brings and the two-class system descends to the one-class. So it widens the frequency range and optimizes overload protection and short circuit protection.

- **Startup Current and Under Voltage Lockout**

The startup current of YS2263 is set to be very low so that a large value startup resistor can be used to minimize the power loss. For AC to DC adaptor with universal input ranged design, a 2 MΩ, 1/8 W startup resistor and a 10uF/25V VDD hold capacitor could be used.

The turn-on and turn-off threshold of the YS2263 is designed to 13V/8V During startup, the hold-up capacitor must be charge to 13V through the startup resistor. The hysteresis is implemented to prevent the shutdown from the voltage dip during startup.

- **Internal Bias and OSC Operation**

A resistor connected between RI pin and GND pin sets the internal constant current source to charge or discharge the internal fixed capacitor. The charge time and discharge time determines the

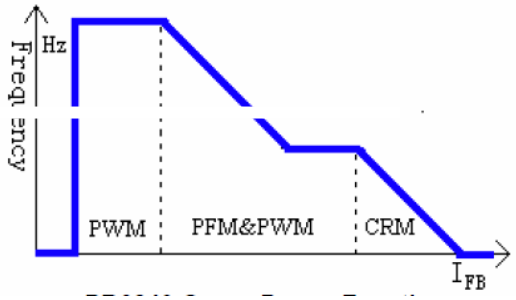
$$F_{OSC} = \frac{6500}{RI(K\Omega)} \quad (kHz)$$

For example, a 100kΩ resistor RI could generate a 20uA constant current and a 65KHz PWM switching frequency. The suggested operating frequency range of YS2263 is within 50 KHz to 130 KHz.

- **Green Power Operation**

The power dissipation of switching mode power supply is very important in zero load or light load condition. The major dissipation results from conduction loss switching loss and consume of the control circuit. However, all of them relates to the switching frequency. There are many difference topologies has been implemented in different chip. The basic operation theory of all these approaches intends to reduce the switching frequency under light-load or no-load condition.

The YS2263 green power function adapts. When RI resistor is 100kΩ, the PWM frequency is 65kHz in medium or heavy load operation. Through modifying the pulse width, The YS2263 could control output voltage. The current of FB pin increases when the load is in light condition and the internal mode controller enters Burst Mode & PWM when the feedback current is over 1.0mA. The operation frequency of oscillator is to descend gradually. When the feedback current is over 1.4mA, the frequency of oscillator is invariable, namely 22 KHz.To decrease the standby consumption of the power supply. If the feedback current
is over 1.4mA, mode controller of the YS2263 would reset internal registerall the time and cut off the GATE pin. While the output voltage is lower than the set value, the register would be set, the GATE pin operate again. So the frequency of the internal OSC is invariable, the register would reset some pulses so that the practical frequency is decreased at the GATE pin.



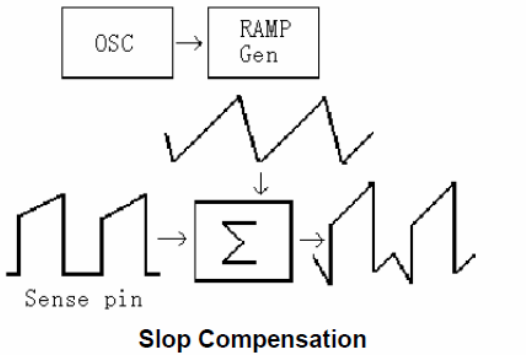

**YS2263 Green-Power Function**

## OPERATION DESCRIPTION

- **Internal Synchronized Slop**

Although there are more advantages of the current mode control than conventional voltage mode control, there are still several drawbacks of peak-sensing current-mode converter, especially the open loop instability when it operates in higher than 50% of the duty-cycle. To solve this problem, the YS2263 is introduced an internal slope compensation adding voltage ramp to the current sense input voltage for PWM generation. It improves the close loop stability greatly at CCM, prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

$$V_{SLOP} = 0.33 \times \frac{DUTY}{DUTY_{MAX}} = 0.4389 \times DUTY$$




**Slop Compensation**

- **Current Sensing & Dynamic peak limiting**

The current flowing by the power MOSFET comes into being a voltage VSENSE on the Sense pin cycle-by-cycle, which compares to the internal reference voltage, and controls the reverse of the internal energy is $E = \frac{1}{2} \times L \times I_{MAX}^{\ 2}$ So adjusting the RSENSE can set the maximal output power of the power supply. The current flowing by the power MOSFET has an extra $(\otimes I = \frac{V_{IN}}{L_P} \times T_D)$ due to the system delay time that is from detecting the current through the Sense pin to power MOSFET off in the YS2263 (Among these, VIN is the primary winding voltage of the transformer and LP is the primary wind inductance).

VIN ranges from 85VAC to 264VAC. To guarantee the output power is a constant for universal input AC voltage, there is a dynamic peak limit circuit to compensate the system delay T that the system delay brings on.

$$IPEAK_{MAX} = \frac{0.65}{R_{SENSE}} \ (V_{IN} = 264V)$$

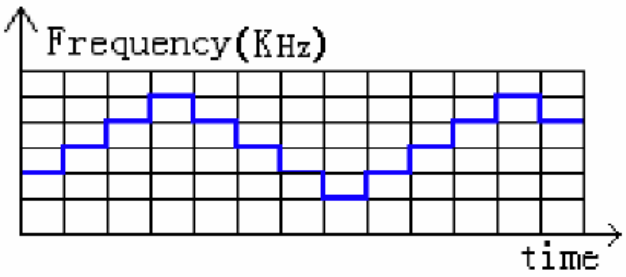
$$IPEAK_{MAX} = \frac{0.85V}{R_{SENSE}} \ (V_{IN} = 85V)$$

- **Soft Start**

The YS2263 features is an internal soft start during the initial power on. As soon as VDD reaches ON, the voltage on the internal fixed capacitor is gradually increased from zero up to the maximum internal clamping level. The time of the soft start is fixed about 1.2mS for the constant charge current and the fixed capacitor.

- **Frequency Jitter**

The frequency jittering is introduced in the YS2263 As following figure, the internal oscillation frequency is modulated by itself. A whole surge cycle includes 8 pulses and the jittering ranges from -3% to +3%. Thus, the function could minimize the electromagnetic interferer from the power supply module.




**Frequency Jitter**

## OPERATION DESCRIPTION

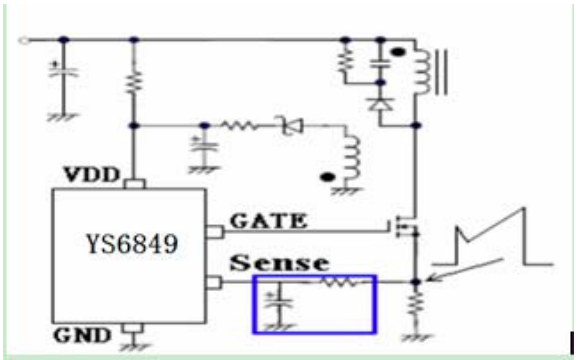
- **OLP&SCP**

To protect the circuit from being damaged under the over load or short circuit condition, a smart OLP&SCP function is implemented in the YS2263. When short circuit or over load occurs in the output end, the feedback cycle would enhance the voltage of FB pin, while the voltage is over 4.8V or the current from FB is below 100uA, the internal detective circuit would send a signal to shut down the GATE and pull down the VDD voltage, then the circuit is restart. To avoid the wrong operation when circuit starts, the delay time is set. When the RI resistance is 100Kohm, the delay time TOLP&SCP is between 33mS and 50mS.The relationship between RI and TOLP&SCP follows the below equation.

$$\frac{RI\times 2}{6\times 10^3}(mS) < T_{OLP\&SCP} < \frac{RI\times 3}{6\times 10^3}(mS)$$

- **Leading-edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the Sense pin, which would disturb the internal signal from the sampling of the RSENSE. There is a 300 nS leading edge blanking time built in to avoid the effect of the turn-on spike, and the power MOSFET cannot be switched off during the moment. So that the conventional external RC filtering on sense input is no longer required. The applications same all green chip PWM control.




- **Over Voltage Protection (OVP)**

There is a 28V over-voltage protection circuit in the YS2263 to improve the credibility and extend the life of the chip. When the VDD voltage is over 28V, the GATE pin is to shutdown immediately and the VDD voltage is to descend rapidly.

- **Auto Self-Recovery Mode**

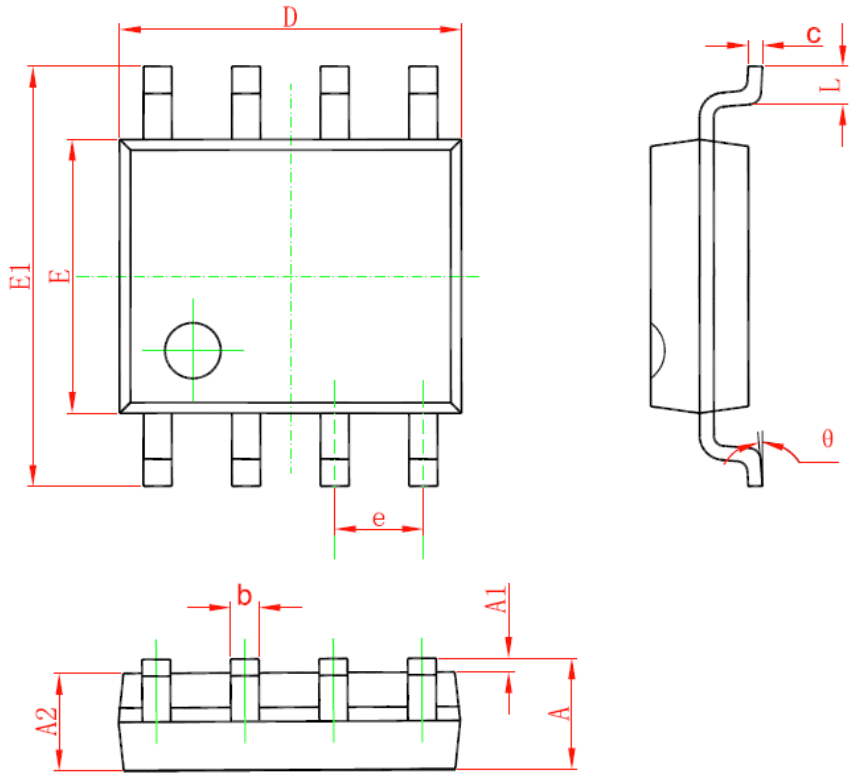
In some applications, operation for SCP&OLP may be necessary. The YS2263 offer this function. When the output is OLP or SCP, the YS2263 could cut off GATE output and pull down VDD voltage immediately, and enter Auto Self-Recovery Mode. To restart the power supply.

- **GATE Driver & Soft Clamped**

The YS2263 output designs a totem pole to drive a periphery power MOSFET. The dead time is introduced to minimize the transfixion current during the output operating. The novel soft clamp technology is introduced to protect the periphery power MOSFET from breaking down and current saturation of the Zener.

## PACKAGE MECHANICAL DATA

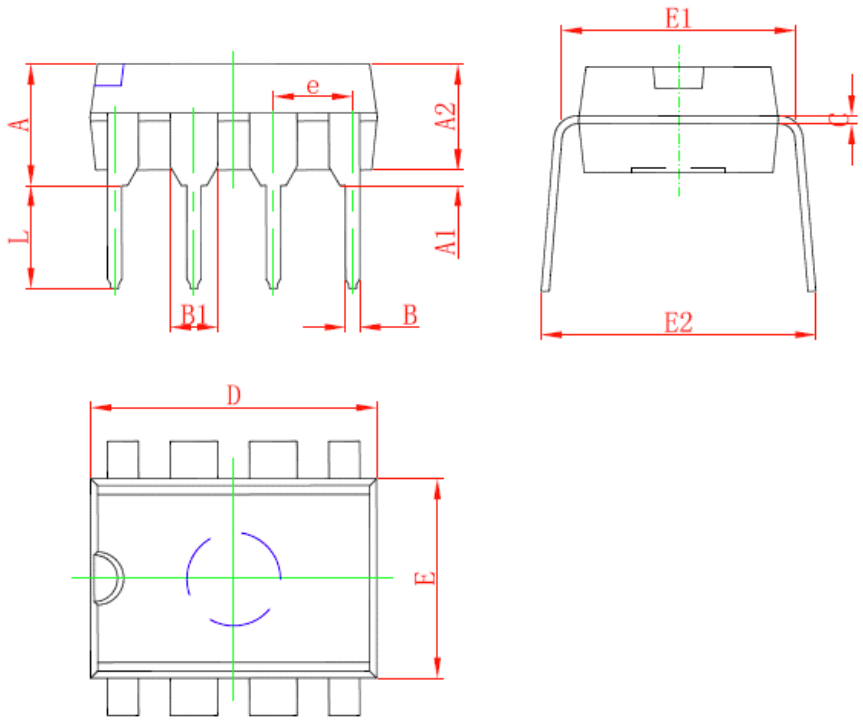
### SOP8 PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.050 | 0.250 | 0.002 | 0.010 |
| A2 | 1.250 | 1.650 | 0.049 | 0.065 |
| b | 0.310 | 0.510 | 0.012 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.150 | 0.185 | 0.203 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.05 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

**PACKAGE MECHANICAL DATA**

**8-Pin Plastic DIP**

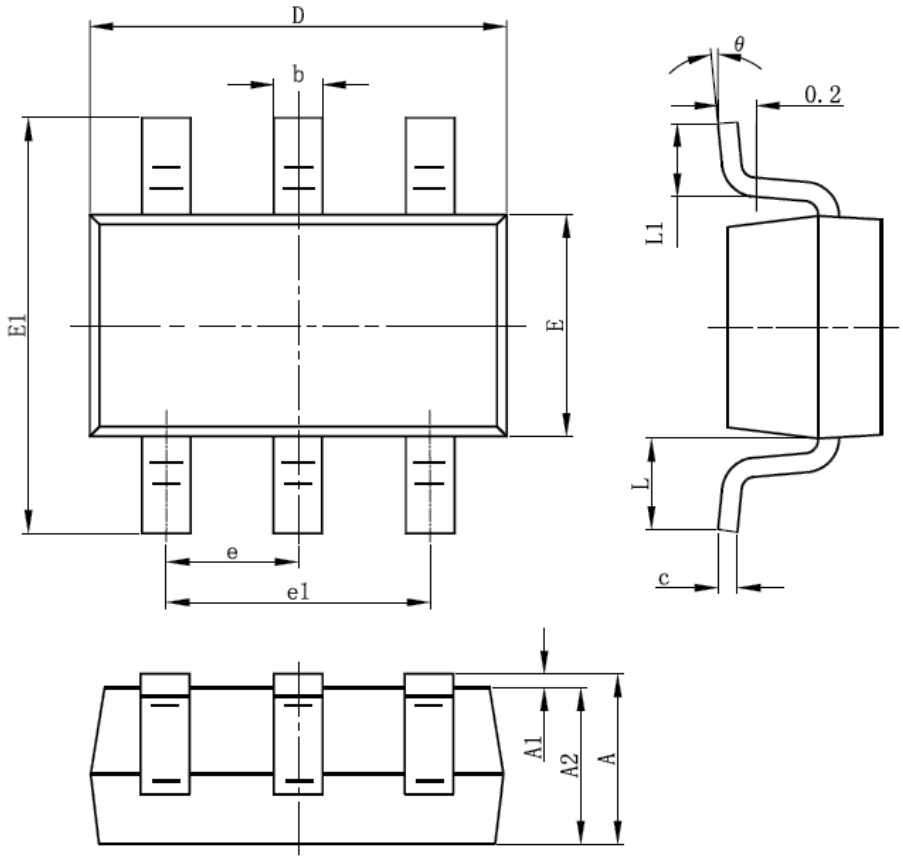



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 4.310 | 0.146 | 0.170 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.600 | 0.126 | 0.142 |
| B | 0.380 | 0.570 | 0.015 | 0.022 |
| B1 | 1.524 (BSC) | | 0.060 (BSC) | |
| C | 0.204 | 0.360 | 0.008 | 0.014 |
| D | 9.000 | 9.400 | 0.354 | 0.370 |
| E | 6.200 | 6.600 | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | 0.288 | 0.312 |
| e | 2.540 (BSC) | | 0.100 (BSC) | |
| L | 3.000 | 3.600 | 0.118 | 0.142 |
| E2 | 8.400 | 9.000 | 0.331 | 0.354 |

**PACKAGE MECHANICAL DATA**

**SOT23-6L**

SOT-23-6L PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.050 | 1.250 | 0.041 | 0.049 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 1.050 | 1.150 | 0.041 | 0.045 |
| b | 0.300 | 0.400 | 0.012 | 0.016 |
| c | 0.100 | 0.200 | 0.004 | 0.008 |
| D | 2.820 | 3.020 | 0.111 | 0.119 |
| E | 1.500 | 1.700 | 0.059 | 0.067 |
| E1 | 2.650 | 2.950 | 0.104 | 0.116 |
| e | 0.950TYP | | 0.037TYP | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.700REF | | 0.028REF | |
| L1 | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |