AVR433: Power Factor Corrector (PFC) with AT90PWM2 Re-triggable High Speed PSC

8-Bit AVR® Microcontrollers

Application Note

Features:

- **Boost Architecture**
- **High Power Factor and low Total Harmonic Distortion**
- **Use few CPU time and few microcontroller resources:**
  - **2 ADC input channels**
  - **1 Analog comparator**
  - **1 PCS channel with re-trigger function and fault protection**
  - **1 optional timer base time**

1. Introduction

This application note explains how to develop a stand alone PFC (Power Factor Corrector) with the AT90PWM2.

A PFC, often required by standards (Example EN 61000-3-2), requires to keep current and voltage in phase in a sinusoidal power supply while also keeping the total harmonic distortion to a minimum.

Implementing a PFC with the AT90PWM2 leaves most peripherals and memory space free for the application (Lighting, motor control...)

Among the many ways to implement a PFC, the solution briefly explained here is based on a current boost topology.

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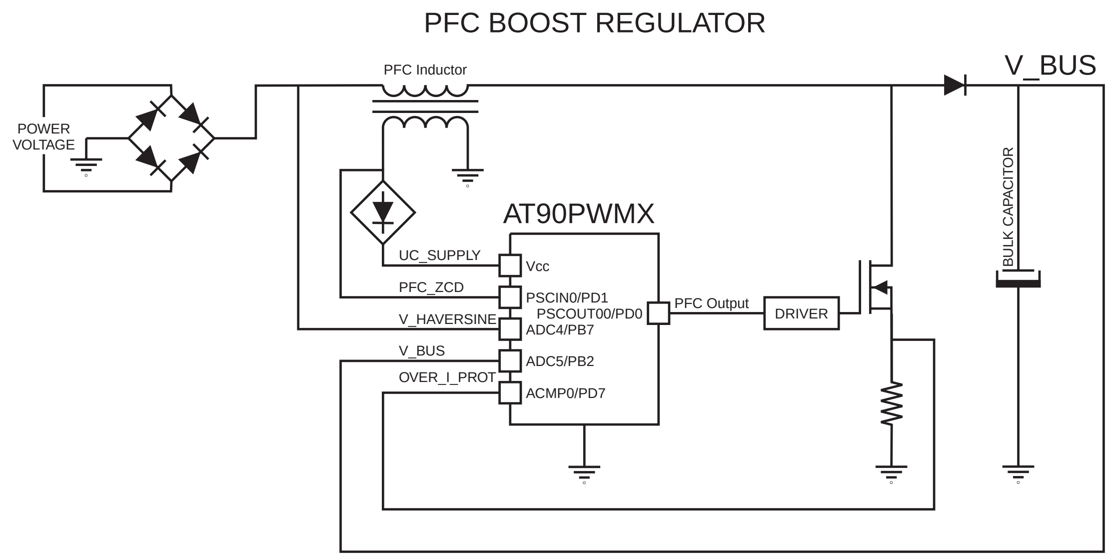
2. Theory of Operation

The current drawn from the line must be sinusoidal and in phase with the line voltage.

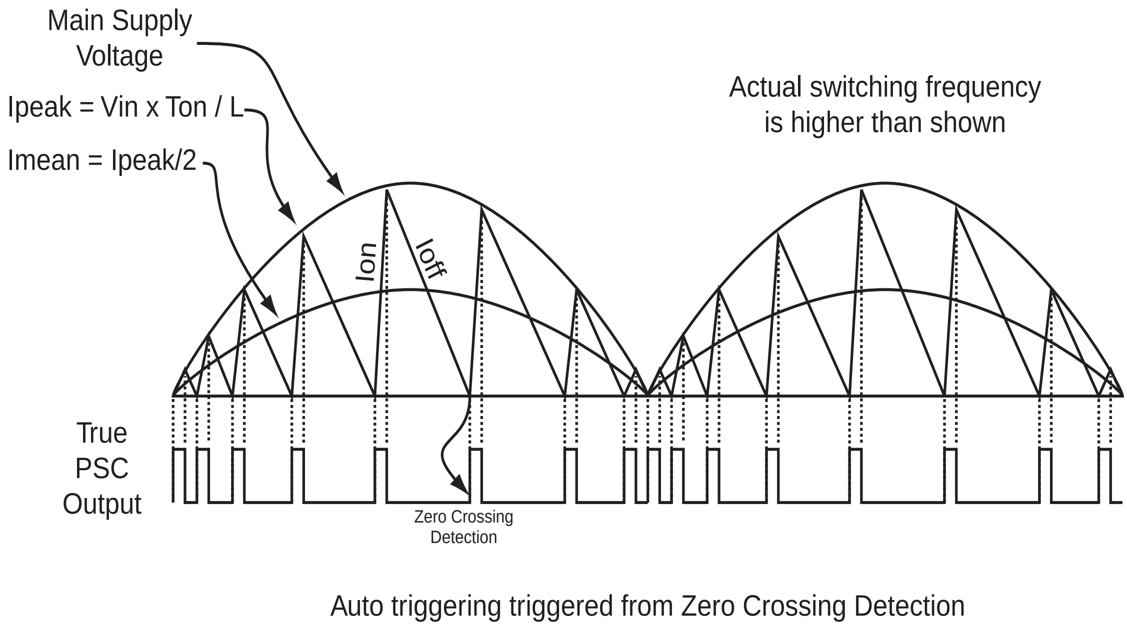
The PFC designed with the AT90PWM2 accomplishes this using a boost converter operating at critical conduction so that the current waveform is triangular. Figure 2-1 shows a block diagram of the PFC (without all detailed discrete components). The magnetic includes a main winding L for PFC and an auxiliary winding for Zero Crossing Detection (ZCD).

Figure 2-1. PFC Boost Regulator Block Diagram



The boost switch ON time is maintained constant over each half cycle of the input sinusoidal voltage. Therefore the peak current for each switching cycle is proportional to the line voltage which is nearly constant during T_{ON}. ($I_{PEAK} = V_{IN} \times T_{ON}/L$). Since the average value of a triangular waveform is half its peak value, the average current drawn is also proportional to the line voltage. See Figure 2-2.

Figure 2-2. PFC main voltage chopping



The TOFF adjustment is automatically done by hardware zero crossing detection while the TON adjustment is done by software each time the main voltage reaches zero Volts (once each half period of the main supply voltage).

3. Hardware Design

The implementation of such a PFC needs the input measurements described below.

3.1 Main Voltage Supply measurement (V_HAVERSINE)

At start-up, the main voltage value is necessary to determine the maximum TON applicable taking into account the maximum current of the PFC transistor.

Moreover, when the PFC is running, this measurement allows to detect when the main supply voltage reaches zero Volt, in order to update the TON.

This measurement is done with an ADC input channel connected to a voltage divider right after the rectifier.

3.2 Current Zero Crossing Detection (ZCD)

The Zero Crossing Detection is necessary to make the PFC run in Critical Conduction Mode.

The Zero Crossing Detection is done thanks to a secondary winding on the PFC coil. This secondary winding allows to detect when the current into the coil reaches zero.

The secondary winding is connected to PSCIN0 pin which directly acts on AT90PWM2 Power Stage Controller 0 (PSC0). Thanks to a special retrig mode on the PSC, as soon as a ZCD is detected, the TOFF is aborted and a new cycle with the TON programmed for the entire main half period cycle is started.

3.3 Output Voltage Measurement (V_BUS)

The output voltage value is necessary to handle the software PFC control loop.

When the main supply voltage reaches zero, PSC parameters are updated in order to get the most stable and accurate output voltage.

This measurement is done thanks to an ADC input channel connected to a voltage divider on the haversine.

3.4 Overcurrent Protection (OVER_I_PROT)

The overcurrent protection allows to switch off by hardware the PSC0 in case of overcurrent in the PFC MOSFET.

A shunt resistor connected between the source of the MOS and the ground is connected at one input of the analog comparator 0. In case the current becomes higher than the transistor can tolerate, the analog comparator output directly switch the AT90PWM2 Power Stage Controller 0 (PSC0) to its predefined dead time value until a software action restarts it.

3.5 MOS Driver Command

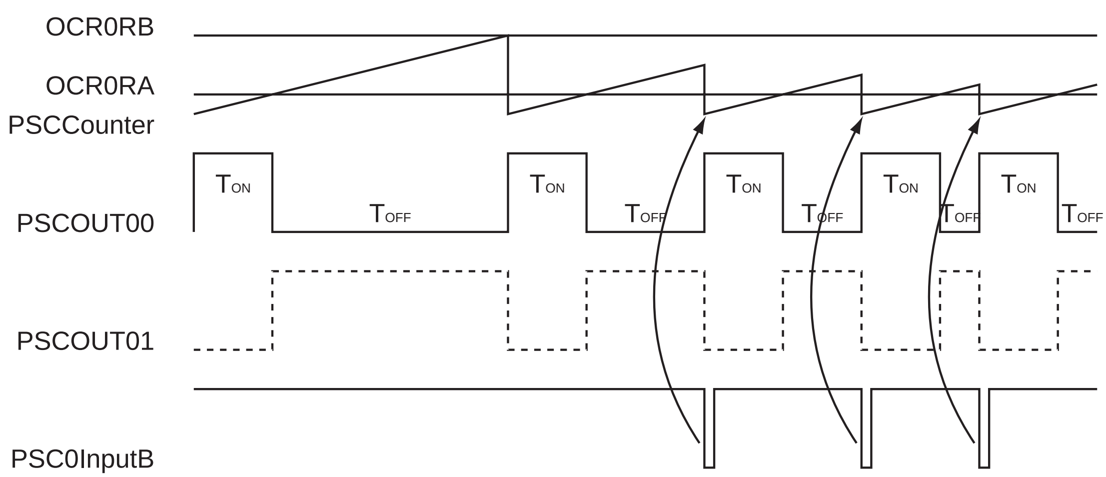
The MOSFET driver is controlled thanks to the Power Stage Controller 0 (PSC0).

As shown in the datasheet on the PSC block diagram, a PSC has two output generators (Waveform generators A and B). Regardless, in order to control the PFC MOSFET, only one output stage is necessary (Stage A), the waveform generator A allows to control the T_{ON} while the waveform generator B allows to control the T_{OFF}.

Thus, in order to adjust the T_{OFF}, the retrig mode 8 is programmed to the waveform generator B even if the output stage B is not used.

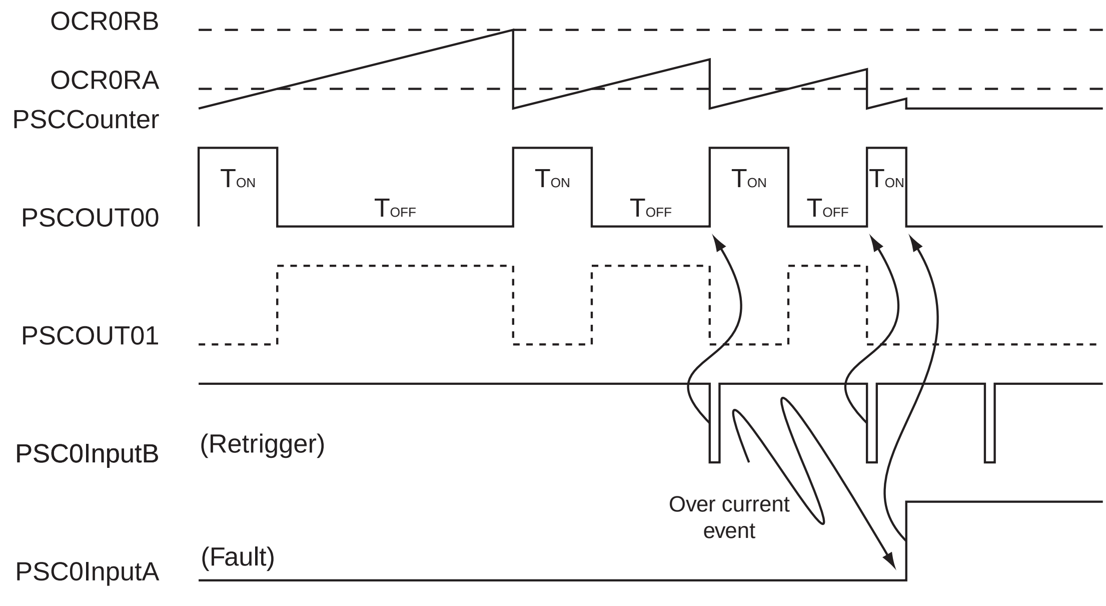
The T_{OFF} adjustment by the mode 8 auto-retrig is shown on Figure 3-1.

Figure 3-1. The PSC input mode 8 allows to start a new cycle each time a ZCD occurs



In order to stop the output in case of overcurrent, fault mode 7 is programmed to the waveform generator A. Indeed, this fault mode acts on both PSC waveform generators and outputs. An example of combined mode 8 auto-retrig and mode 7 fault mode is shown on Figure 3-2.

Figure 3-2. The PSC input mode 7 Allows to stop the PSC in case off overcurrent



4. Software Design

In order to start, the PFC needs a few pre-defined pulses until a zero crossing is detected.

Shortly after, the PFC can run automatically with only few CPU resources.

The adjustment of the PFC T_{ON} and T_{OFF} is down as follows:

- The T_{OFF} is automatically adjusted by hardware at each PFC inductor current zero crossing detection,

- The T_{ON} is adjusted by software accordingly to the Vout measurement each time the main supply voltage reach zero (Each half period of the main voltage supply).

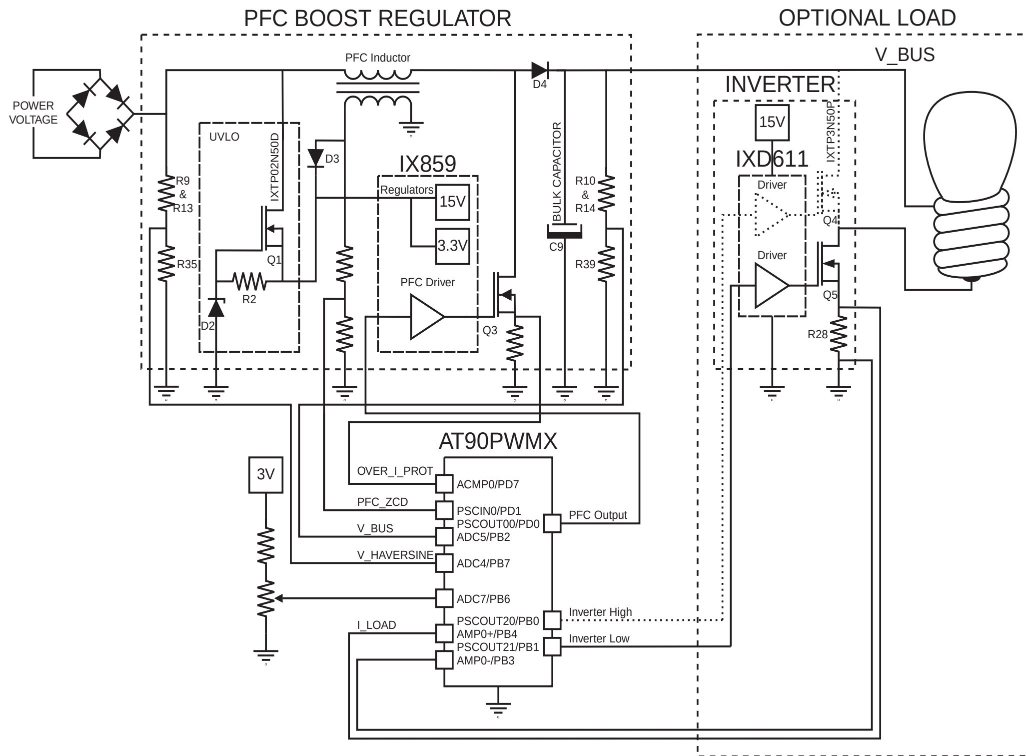
The software can run as follow:

- First all peripherals are initialized, then the ADC is started to run automatically in interrupt mode to capture all necessary values. Then the PFC can be started and run in quasi stand alone mode.

5. Example of complete PFC block diagram

On Figure 5-1, there is an example of block diagram of a complete PFC application. In this example, a second PSC is used in order to control a variable load (lamp).

Figure 5-1. Complete PFC block diagram example



A complete PFC application has been developed on the dimmable fluorescent lamp demonstrator (ATAVRFBKIT / EVLB001). On this document you can find a complete PFC design (including the microcontroller supply). All information and software are available on the ATMEL web site.

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