Investigation of High-density Integrated Solution for AC/DC Conversion of a Distributed Power System

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Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

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May 5th, 2006
Blacksburg, Virginia

Keywords: High frequency, High density, Front-end, DPS, AC/DC, DC/DC, PFC, Three-level, Bridgeless PFC, Resonant converter, LLC, IPEM, Embedded power, Power integration

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ABSTRACT

With the development of information technology, power management for telecom and computer applications become a large market for power supply industries. To meet the performance and reliability requirement, distributed power system (DPS) is widely adopted for telecom and computer systems, because of its modularity, maintainability and high reliability.

Due to limited space and increasing power consumption, power supplies for telecom and server systems are required to deliver more power with smaller volume. As the key component of DPS system, front-end AC/DC converter is under the pressure of continuously increasing power density. For conventional industry practices, some limitations prevents front-end converter meeting the power density requirement. In this dissertation, different techniques have been investigated to improve power density of front-end AC/DC converters.

For PFC stage, at low switching frequency, PFC inductor size is large and limits the power density. Although increasing switching frequency can dramatically reduce PFC inductor size, EMI filter size might be larger at higher switching frequency because of the change of noise spectrum. Since the relationship between EMI filter size and PFC switching frequency is unclear for industry, PFC circuits always operate with switching frequency lower than 150 kHz. Based on the EMI filter design method, together with a simple EMI noise prediction model, relationship between EMI filter corner frequency and PFC switching frequency was revealed. The analysis shows that switching frequency

of PFC circuit should be higher than 400 kHz, so that both PFC inductor and EMI filter size can be reduced.

Although theoretical analysis and experimental results verify the benefits of high switching frequency PFC, it is essential to find a suitable topology that allows high switching frequency operation while maintains high efficiency. Three PFC topologies, single switch PFC, three-level PFC with range switch and dual Boost PFC, were evaluated with analysis and experiments. By using advanced semiconductor devices, together with proposed control methods, these topologies could achieve high efficiency at high switching frequency. Thus, the benefits of high frequency PFC can be realized.

In front-end converter, large holdup time capacitor size is another barrier for power density improvement. To meet the holdup time requirement, bulky holdup time capacitor is normally used to provide energy during holdup time. Holdup time capacitor requirement can be reduced by using wider input voltage range DC/DC converte. Because LLC resonant converter can realized with input voltage range without sacrificing its normal operation efficiency, it becomes an attractive solution for DC/DC stage of front-end converters. Moreover, its small switching loss allows it operating at MHz switching frequency and achieves smaller passive component size. However, lack of design methodology makes the topology difficult to be implemented. An optimal design methodology for LLC resonant converter has been developed based on the analysis on the circuit during normal

operation condition and holdup time. The design method is verified by a 1 MHz switching frequency LLC resonant converter with 76W/in^3 power density.

When front-end converter operates at high switching frequency, negative effects of circuit parasitics become more pronounced. By integrating active devices together with their gate drivers, Active Integrated power electronics module (IPEM) can largely reduce circuit parasitics. Therefore, switching loss and voltage stress on switching devices can be reduced. Moreover, IPEM concept can be extended into passive integration and EMI filter integration By using this power integration technology, power density and circuit performance of front-end converter can be improved, which is verified by theoretical analysis and experimental results.

To Whom

It is needed

ACKNOWLEDGMENT

I would like to thank my advisor, Dr. Fred C. Lee for his guidance and help during my Ph. D. program. His knowledge, research attitude and ways of thinking are most valuable during my years of study and they will keep help me in my future life. I also want to thank his challenge during my past researches, which could always help me find issues in my work and lead to the right direction. Without his challenges, I might not be able to accomplish this

I am grateful to my committee members, Dr. Daan van Wyk, Dr. Fred Wang, Dr. Douglas Lindner and Dr. Guo-Quan. Lu, for their valuable suggestions and numerous help.

It has been a great pleasure to work in the Center for Power Electronics Systems (CPES). I would like to acknowledge the CPES administrative and management staff, Ms. Teresa Shaw, Ms. Linda Gallagher, Ms. Trish Rose, Ms. Ann Craig, Ms. Marianne Hawthome, Ms. Elizabeth Tranter, Ms. Michellel Czamanske, Ms. Linda Long, Mr. Robert Martin, Mr. Steve Chen, Mr. Dan Huff, Mr. Gary Kerr, Mr. Jamie Evans and Mr. Callaway Cass, for their countless help.

I am especially indebted to my teammates in my research group, Dr. Ming Xu, Dr. Peter Barabosa, Dr. Qun Zhao, Dr. Francisco Canales, Dr. Wei Dong, Dr. Bo Yang , Dr. Yong Li, Dr. Yang Qiu, Mr. Liyu Yang, Ms. Manjing Xie, Miss Tingting Sang, Ms. Juanjuan Sun, , and Mr. Dianbo Fu, Mr. Chuanyun Wang, Mr.

Yonghan Kang, Mr. Clark Person, Dr. Zhiguo Lu, Dr. Jinjun Liu, Dr. Zhenxian Liang, Dr. Zhou Chen, Dr. Wenduo Liu, Ms. Yan Liang. It was a pleasure to work with such a talented, hard-working and creative group.

I would like to thank my colleagues, Dr. Jingdong Zhang, Dr. Peng Xu, Dr. Sihua Wen, Dr. Jinghong Guo, Dr. Kaiwei Yao, Mr. Mao Ye, Mr. Yu Meng, Dr. Yuancheng Ren, Dr. Jinghai Zhou, Ms. Li Ma, Dr. Xigen Zhou, Dr. Bin Zhang, Dr. Zhiye Zhang, Dr. Guofeng Bai, Dr. Huiyu Zhu, Dr. Jian Ying, Dr. Ning Zhu, Dr. Haifei Deng, Dr. Xudong Huang, Dr. Huijie Yu, Mr. Wei Shen, Ms. Shen Wang, Mr. Luis Arnemod, Mr. Carson Baisden, Mr. Arthus Ball, Mr. Bryan Charboneau, Mr. Yan Dong, Mr. Jerry Francis, Mr. Bin Huang, Miss Yan Jiang, Dr. Ching-Shan Leu, Mr. Jian Li, Dr. Qian Liu, Mr. Ya Liu, Mr. Anish Prasai, Mr. Andew Shmit, Mr. Honggang Sheng, Mr. Time Thacker, Mr. Alex Uan-Zo-Li, Mr. Yuvcheng Ying. Their friendships and help have made my stay at CPES pleasant and enjoyable.

I would like to give my special thanks to my family, my wife and my parents, their love and support make my life more colorful and meaningful.

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

1.1 Research Background

With the development of information technology, telecom and computer systems become a large market for power supply industry. Recent statistic data show that the demands for these systems are continuously increasing [A-1]. Moreover, because of the improving of integrated circuit technology, which follows Moor's Law, computers and telecom equipments keep increasing their density and functionality. The increasingly functionality requires more power consumption and higher density requires less size on the power supplies. Therefore, the power supplies for the telecom and computer applications are required to provide more power with less size and cost [A-2][A-3].

To meet these requirements, distributed power system (DPS) is widely adopted. Instead of using a single bulky power supply to provide the final voltages required by the load, distributed power system distributed the power processing functions among many power processing unites [A-4]-[A-7]. One typical DPS structure is the intermediate bus structure [A-8][A-9], as shown in Figure 1-1. In this system, the voltages that are needed for loads are generated through two stage approach. In first stages, many front-end converters are parallel together to generate the intermediated bus voltage, which is normally 48V, or 12V. After that, the following load converters then transfer the intermediate bus voltage into the voltages that load need. Because of this modular approach, DPS

system has many advantages comparing with centralized power system, and it is widely adopted for telecom and computer system, such as easier thermal management, higher reliability, modularity and easy maintainability [A-6][A-7].

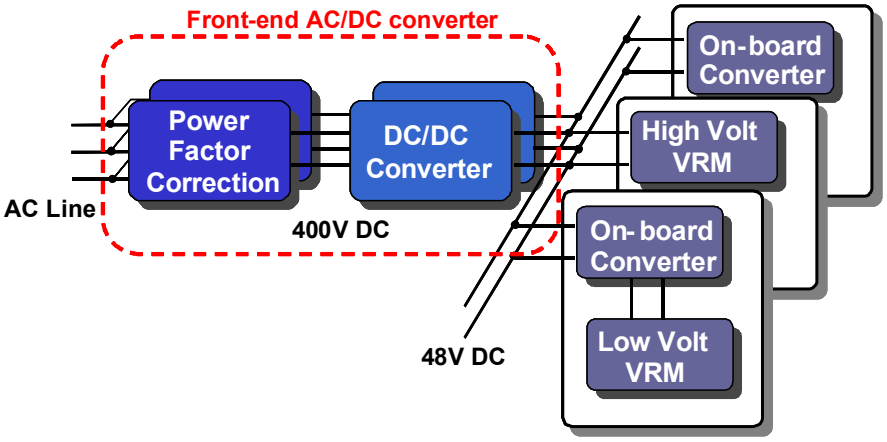


Figure 1-1 Distributed power system

A) Easier thermal management

Because several front-end converters are parallel together to provide the total power, each converter only handles part of the total power. Thus, power loss is distributed among different converter, and the thermal design could be much easier. Moreover, because of less loss generated in each module, each module could have its own thermal management mechanism. The system thermal design is much simplified comparing with centralized power system.

B) Higher reliability

For computer and telecom applications, it is required to have high reliability so that the service providers can continuous pride service to customers. In DPS

systems, because of modular approach, each module only handles part of the total power. Thus, electrical and thermal stresses on the devices are much reduced, which can result in higher reliability.

Besides less stress on the devices, DPS system can also improve its reliability by using N+1 redundancy. If N is defined as the minimum number of modules that is required to provide the total load power, by adding one additional module, higher reliability can be achieved. In this way, system can still maintain availability even with one module fail. Moreover, because the power handling capability of N+1 system is higher than the system power consumption requirement, each module handles even less power, which can further improve the reliability of the system.

C) Modularity

In DPS systems, identical front-end converter modules are parallel together. This modular approach makes the system extendable, easy reconfiguration and less cost.

For instance, one the system power consumption requirement increase, users can simply parallel more modules to meet the requirement. However in the centralized power system, new power system has to be purchased to meet the power consumption requirement. In addition, because each module is identical, the design and manufacturing can be much easier and faster. Moreover, different

standard approvals, such as safety and harmonics standards, can be obtained much faster.

D) Maintainability

Hot-swap becomes popular feather for DPS systems, which allows users replace the deficit power module without interrupting the whole system operation (on-line replacement). Therefore, once the module is failure, power supply manufacture could provide system maintains without shutting down the whole system, which is very desirable for systems that require high availability, such as telecom and data centers.

Furthermore, by using system level controller, the interleaving operation between different modules becomes available. Through interleaving operation of different modules, input and output current ripple and harmonics could be canceled because of phase difference among different modules [A-10][A-11]. Thus, the EMI filter size could be reduced and system can achieve higher power density.

Because of these benefits comparing with the centralized power system, DPS systems are widely adopted by telecom and computer applications. One typical DPS system for server is shown in Figure 1-2. The front-end modules are on the bottom of the rack. It can be seen that several modules are putting side by side to provide the energy. The following stage load converters are on the circuit boards

on the equipment modules locating on the upper side of the rack. Therefore, these load converters are also called on-board modules.

Figure 1-2. DPS for server system.

Because size of the rack is fixed, it is desired to have more space for the equipments such as the telecom boards or computer servers. Thus, the power supply size has to be minimized. On the other hand, increasing of equipments requires more power consumption. The power supplies are in turn required to output more power within less volume, which means higher power density.

Furthermore, because the width of rack is fixed, such as 17U or 19U, and the power modules are vertically slide inside the rack, as shown in the bottom of Figure 1-2. By reducing the profile of power modules, more modules could fit into the rack and provide more power. Therefore, 1U (1.75 inches) becomes a standard profile for present power modules.

For DPS systems, front-end AC/DC converters are under the pressure of continuous increasing power density requirement. As shown in Figure 1-3, the power density of front-end converter for server and telecom is continuously increasing [A-12]. At year 2000, the power density is only around 7~8W/in^3. However, the power density reaches 20W/in^3 at year 2005. And the power density of front-end converter is required to keep increasing. Therefore, the dissertation is mainly focus on the investigation of different techniques to improve the power density of front-end AC/DC converter, which includes higher switching frequency, better topology and the integration solutions.

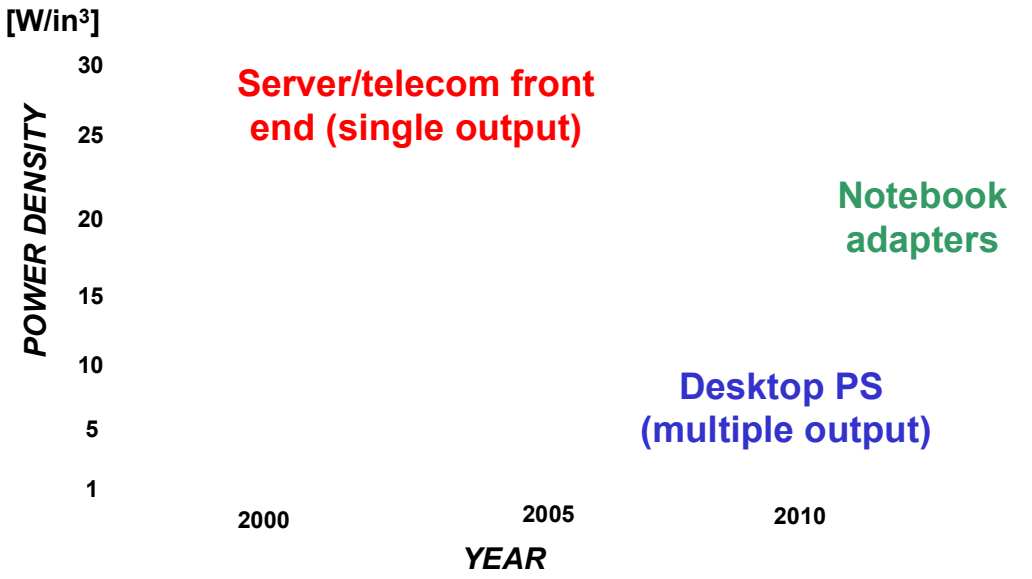


Figure 1-3. Power density trends for front-end AC/DC converters.

1.2 Issues with Existing Solutions

According to the requirements of input current harmonics and output voltage regulation, front-end converter is normally implemented by two-stage approach,

which is power factor correction (PFC) stage followed by the DC/DC stage. PFC stage rectifies the input AC voltage and transfers it into a regulated intermediate DC bus. At the same time, power factor correction function is achieved [A-13][A-14]. The following DC/DC stage then converters the DC bus voltage into a regulated output DC voltage for distribution bus, which is required to meet the regulation and transient requirement.

Due to two-stage power processing, system efficiency depends on the efficiencies on both stages. For instance, if both stages can achieve 90% efficiency, the whole system efficiency is only 81%, which is much lower than that of each stage. Therefore, it is essential to improve the efficiency for both the PFC stage and DC/DC stage.

A typical front-end AC/DC converter is shown in Figure 1-4. Its PFC stage uses single switch continuous conduction mode (CCM) PFC with average current mode control, and DC/DC stage uses phase shift full bridge (PSFB) with current doubler. Because of simple structure and smaller EMI filter size, single switch CCM PFC is wide adopted for power factor correction applications. Meanwhile, PSFB is able to achieve high efficiency with soft switching capability. Thus, it is popular for kilo-watt range power supply designs. Because these circuit topologies have been existed for many years and they have been well understood and adopted by power supply industries.

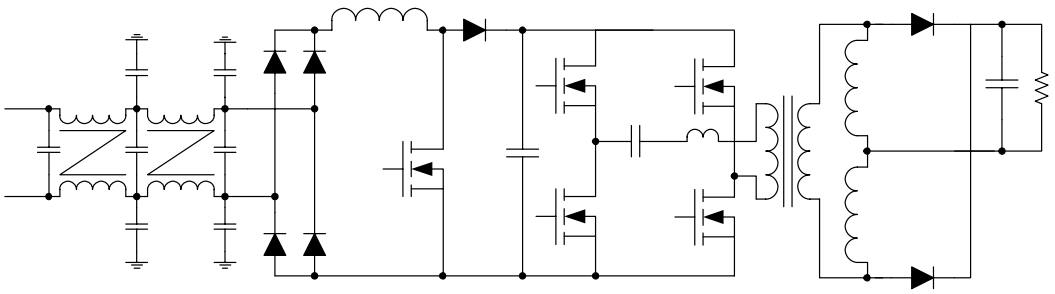


Figure 1-4. Typical front-end AC/DC converter.

However, due to several limitations, it is difficult to further increasing the power density of the existing converters. A state of art front-end AC/DC converter is shown in Figure 1-5, although it can reach 25W/in^3 power density, several issues can still be observed [A-12].

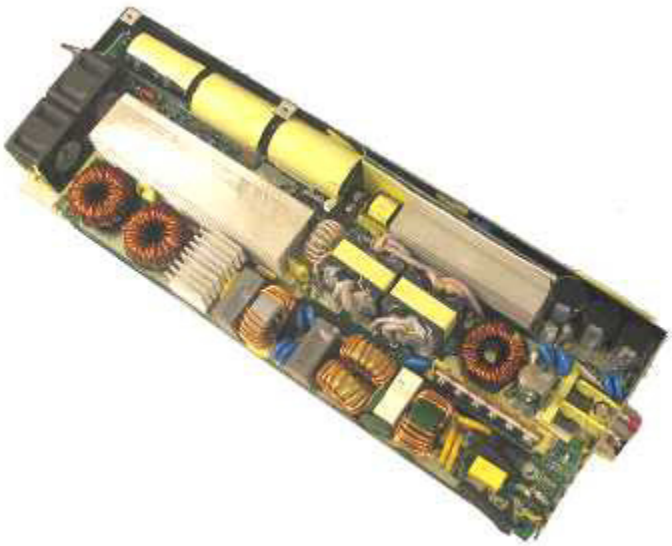


Figure 1-5. State of art front-end converter.

PFC inductor and EMI filters takes about one third of the whole converter volume. PFC inductor is used to achieve power factor correction and shape the input current to be sinusoidal. To ensure smaller ripple current, PFC inductor is designed based on the switching frequency. It is desired to have higher switching

frequency to achieve smaller PFC inductor size. However, due to the large switching loss caused by PFC stage, it is difficult to increase the switching frequency. Meanwhile, the EMI filter is used to attenuate the EMI noise generated by the system. Because of stringent EMI standard requirement, large EMI filter is normally used in front-end converters. Since the relationship between EMI filter size and switching frequency is not clear for the industry, most PFC circuits in the real implementation are switching below 150 kHz [A-15].

As mentioned before, due to two-stage approach, system efficiency is low. Thus, large heat-sinks are required to maintain the thermal handling capability. To achieve higher power density, heat-sink size can be reduced by either improving the system efficiency or improve the system thermal design.

Another large component in front-end converter is the bulky holdup time capacitor. According to the specifications of server systems, front-end AC/DC converters are required to maintain regulated output voltage for more than 20mS when the input AC line is lost. During holdup time, all the energy transferred to the load comes from holdup time capacitor. Therefore, large holdup time capacitors are required to provide the energy during holdup time. Holdup time capacitor requirement is determined by the system power level and the input voltage range of DC/DC converter. Apparently, higher the system power level, more energy is required to transfer to the load. Thus, larger holdup time capacitor is required. On the other hand, wider the DC/DC stage input voltage range, more

energy stored in the holdup time capacitor could be used during holdup time. Thus, less holdup time capacitor can be used. However, in the conventional front-end AC/DC converters, DC/DC stage employs PWM converter, and it is difficult to achieve wide input range together with high efficiency. Therefore, to maintain high system efficiency, large holdup time capacitor has to be used [A-16].

Furthermore, it can be observed that the passive components in the DC/DC stage, such as the transformers and inductors, have large size. Similar to the PFC stage, large switching loss prevents DC/DC stage operating at high switching frequency, which results in large passive components size [A-17].

Moreover, components used in front-end converters are mainly customized designed, and lack of integration. Therefore, costs of components are high, especially for the inductors and transformer. Moreover, large amount of components and lack of integration make front-end converter difficult to be manufactured, which results in higher cost and long manufacturing cycle. [A-18]

To address these issues, the objective of dissertation is to investigation different solutions for front-end converters to achieve higher efficiency, higher power density through high switching frequency topologies and integration technologies.

1.3 Dissertation structure

From the introductions, it can be observed that several fundamental limitations prevent further increasing power density of front-end AC/DC converter. To meet the increasing power density requirement, in this dissertation, different techniques has been investigated to improve the power density of front-end converter, which include high switching frequency, different circuit topologies and integrated solution for front-end converters.

In Chapter 2, switching frequency impacts on PFC circuit has been discussed. For PFC stage, it is desirable to have higher switching frequency to shrink Boost inductor size, since the Boost inductor value is inverse proportional to the switching frequency for given ripple current. However, due to EMI noise standard requirement, EMI filter might increase dramatically even with higher switching frequency. Therefore, it is essential to find out the switching frequency design guideline to achieve higher power density. From the theoretical analysis and experimental verification, it demonstrated that by pushing the switching frequency higher than 400 kHz, both the Boost inductor and EMI filter size keep decreasing and higher power density can be achieved. Furthermore, through the analysis, several switching frequencies should be avoided due to the larger EMI filter size [A-19].

Because high switching frequency of PFC circuit can results in smaller EMI filter size and Boost inductor size, its switching frequency is desired to be higher

than 400 kHz. With higher switching frequency, switching loss is the major concern. To allow PFC circuit operating with switching frequency higher than 400 kHz, in Chapter 3, different solutions have been discussed. Firstly, the CoolMOS^{TM} and SiC Schottky diode are introduced. These new devices can achieve higher switching speed and removes the reverse recovery current, which provides the high switching frequency operation capability. After that different circuit topologies have been discussed [A-20]

Three-level PFC with range switch could dramatically increase circuit efficiency at low input line by reducing the conduction loss and switching loss. Besides, different control method can also be implemented to further improve the converter efficiency at high input line.

For Dual Boost PFC, by removing the input diode bridge, circuit conduction loss is reduced and higher efficiency can be achieved. However, without the input diode bridge, dual Boost PFC suffers from large common mode (CM) EMI noise. A new EMI noise reduction circuit has been proposed to control the CM noise of Dual Boost PFC [A-21].

Because of higher efficiency of these alternative PFC circuit topologies, PFC circuit switching frequency can be further pushed up to achieve even smaller EMI filter and Boost inductor size.

Besides PFC stage Boost inductor and EMI filter, front-end converter also has large holdup time capacitors, which prevents further improving power density. Holdup time capacitor requirement is only determined by the converter power level and DC/DC stage operation range. For conventional PWM DC/DC converters, it is difficult to achieve high efficiency and wide input voltage range together. Therefore, different holdup time extension circuits have been proposed to reduce DC/DC stage operation range requirement. However, these auxiliary circuits are complex and needs extra control circuit. Instead of using extra holdup time extension circuit, LLC resonant converter is able to achieve high efficiency together with wide input voltage range, which gives a promising solution for DC/DC stage of front-end converters. However, lack of design methodology makes the circuit difficult to be adopted by industry. In Chapter 4, an optimal deign methodology has been proposed. Through the analysis of circuit operation at normal condition and during holdup time, it shows that a successful LLC resonant converter design relies on choosing suitable magnetizing inductor and inductor ratio [A-22].

Furthermore, LLC resonant converter has very small switching loss, due to its soft switching capability and soft turn-off of secondary diode. Therefore, it is able to operate at very high switching frequency to achieve high power density while maintain high efficiency. In Chapter 4, an LLC resonant converter with 1MHz switching frequency has been demonstrated and achieves 76W/in^3 power density with 92.5% efficiency at full load.

In Chapter 5, the integration solution for front-end AC/DC converter has been discussed. Because the power supplies are mainly customized design and lack of integration, the cost of manufacturing is high. By introducing Integrated Power Electronics Module (IPEM) concept, front-end converters can be simplified as putting several modules together, which can dramatically reduce the manufacturing cost and make automatically manufacturing capable.

Besides the cost, when front-end converter operates at very high switching frequency, circuit parasitic effects become more pronounced and hurt the circuit performance, especially the switching loss and voltage stress on the devices. By using integration technology, circuit parasitics can be dramatically reduced. Through the theoretical analysis and experimental results, the reduction of circuit parasitics could result in less switching loss and voltage stress.

To demonstrate the benefits of IPEMs, DC/DC converters using asymmetrical half bridge (AHB) and LLC resonant topologies are implemented with Active and Passive IPEM. Power density improvement is demonstrated. Furthermore, IPEM concept is extended to whole front-end converter system. Two identical front-end converters with discrete devices and IPEMs have be built and evaluated in detail. The experimental results show that the IPEM version is able to achieve 1.5 time power density improvement and 2 to 3% efficiency improvement. Meanwhile, due to the higher switching speed and different circuit layout, IPEM version has higher EMI noise comparing with discrete version converter [A-23][A-24].

Chapter 2. Investigation of High Switching Frequency PFC

2.1 Introduction

For distributed power systems (DPS), high power density, low profile begins to be the standard approach. For a typical front-end AC/DC converter shown in Figure 2-1, EMI filter and PFC inductor take about half of the total converter volume. Therefore, it is essential to shrink the size of EMI filter and PFC inductor to achieve higher power density. Since the size of passive components of the converters decrease with the increasing of switching frequency, to achieve higher power density, converters are operating with continuously increasing switching frequencies.

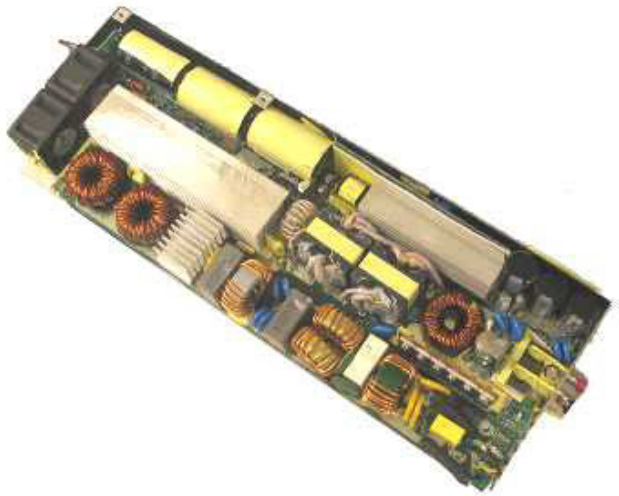


Figure 2-1. Typical Front-end AC/DC converter.

Because PFC inductor design is based on the switching frequency current ripple, its size decreases with increasing switching frequency. Thus, high

switching frequency is desirable to achieve higher power density. Furthermore, the higher switching frequency dramatically reduces PFC inductor size and inductance, as well as the parasitics, which further improves the circuit EMI performance.

However, the relationship between EMI filter size and switching frequency is not clear for PFC designers. As a result, limited efforts has been performed to push the PFC switching frequency higher, since the reduction of PFC inductor size could be easily overwhelmed by the increasing of EMI filter size and heat-sink size due to the higher switching loss.

In this Chapter, based on the simulation results and experimental results, a simple imperial equation was derived to predict the different mode (DM) and common mode (CM) noise for PFC circuit with different switching frequencies. According to the derived EMI noise, EMI filters can be designed for different switching frequencies to meet the EMI standard required. The analysis results showed that the switching frequency needs to be increased to certain level that both the PFC inductor size and EMI filter size can be reduced. According the analysis, switching frequency selection guideline is given. Later the experimental results verified the theoretical analysis.

2.2 Switching frequency impact on the PFC inductor

For power factor correction (PFC) circuit, constant switching frequency single switch PFC with continuous conduction mode (CCM) is the most widely used topology because of its simplicity and smaller EMI filter size [B-1][B-2]. The circuit diagram is shown in Figure 2-2, and it is constructed by the uncontrolled diode bridge, followed by a Boost converter.

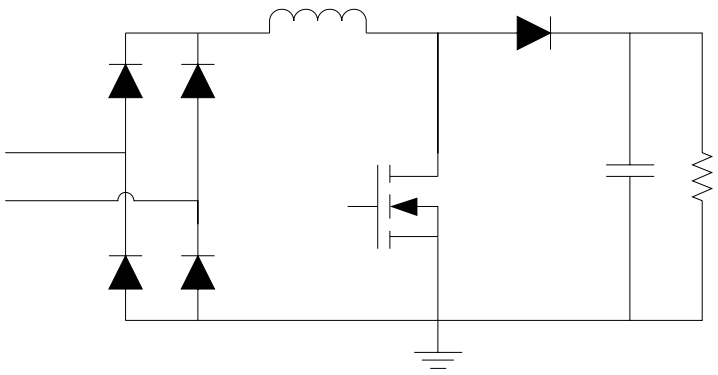


Figure 2-2. Single switch CCM PFC.

For the CCM PFC circuit with constant switching frequency, PFC inductor (PFC inductor) is designed based on the switching frequency current ripple. To ensure smaller EMI filter size, current ripple peak to peak value is normally chosen as 20 to 30 % of maximum input line current. For instance, a 1kW PFC circuit with 150V minimum input voltage, considering 92% efficiency, the maximum input current is

$$I_{\max} = \frac{1000}{150 \times 0.92} \times \sqrt{2} = 10.24A$$

If considering 30% ripple current, the ripple current peak to peak value should be

$$I_{ripple} = 30\% \times I_{\max} = 3.1A$$

Because of the input AC line voltage, duty cycle of PFC circuit changes along with the input line voltage. According to volt-second balancing on PFC inductor, duty cycle of PFC circuit can be calculated as

$$d = 1 - \frac{|v_{in}|}{V_O}$$

In this equation, V_O is the output voltage and v_{in} is the input line voltage instantaneous value. Normally, to ensure universal line input, the output voltage is chosen as 400V. Thus, the duty cycle along a half line cycle under different input line conditions can be calculated and demonstrated in Figure 2-3.

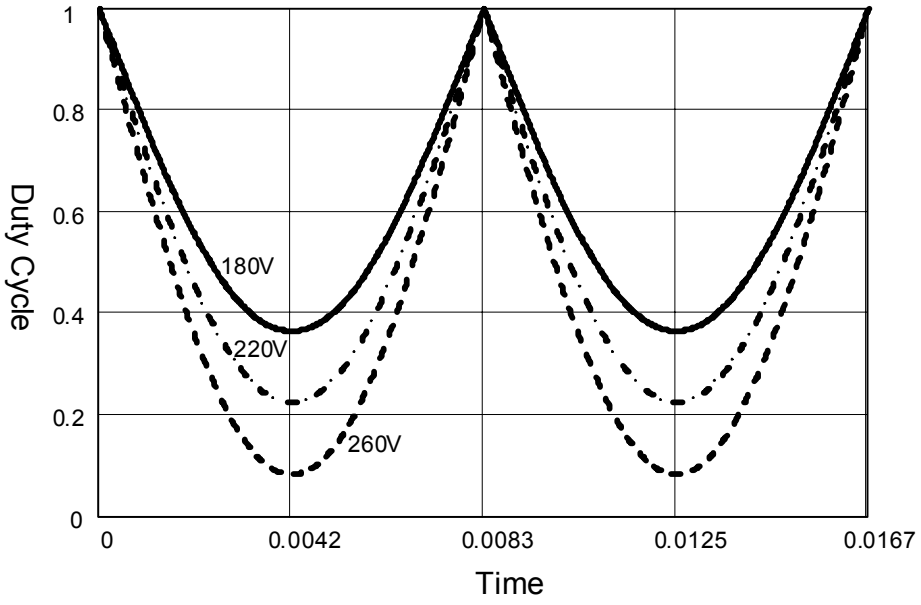


Figure 2-3. PFC duty cycle along half line cycle for different input voltages.

Based on the calculated duty cycle, current ripple can be calculated accordingly.

$$I_{ripple}(t) = \frac{V_o - |v_{in}|}{L_{boost}}(1-d)T_S$$

Here L_{boost} is the PFC inductor value and T_S is the switching cycle. Because the duty cycle changes along the line cycle, the ripple current changes correspondingly. As shown in Figure 2-4, current ripple reaches it maximum value when the input voltage instantaneous value is half of the output voltage. Because the input voltage is half of the output voltage, under this condition, the duty cycle of PFC circuit is 0.5.

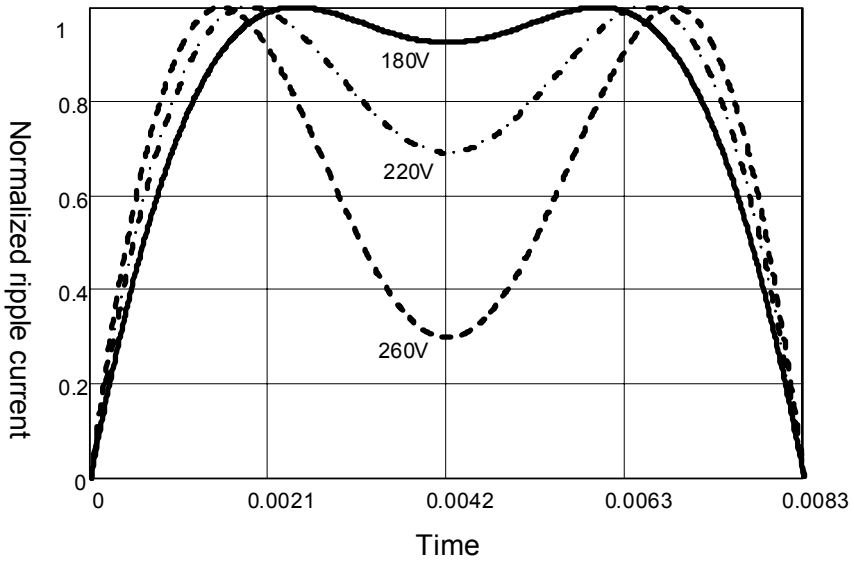


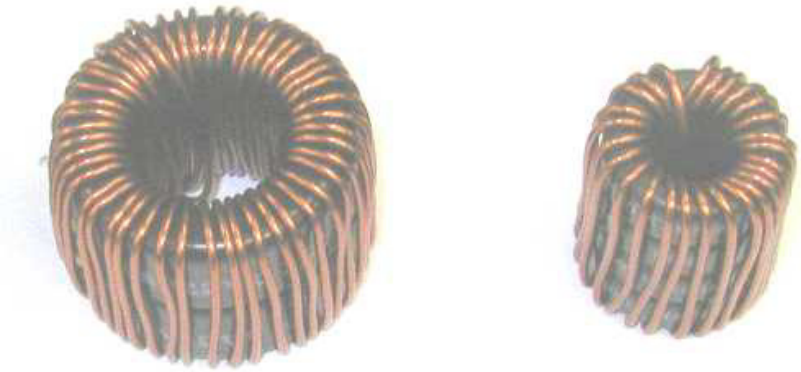
Figure 2-4. Current ripple along the line cycle for different input voltages.

The maximum current ripple is used to design the PFC inductor. This maximum current ripple should be 20 to 30% of the maximum line current. Based on this, PFC inductor value can be calculated as

$$L_{boost}(f) = \frac{1}{2f}\frac{V_o}{2I_{ripple}}$$

From this equation, PFC inductor value is the function of switching frequency, ripple current amplitude and output voltage. For the predetermined output voltage and ripple current amplitude, PFC inductor value is inverse proportional to the switching frequency. The higher the switching frequency, the smaller the boot inductor value is.

As shown in Figure 2-5, for 100 kHz, to keep 30% current ripple, PFC inductor value is required to be 350uH. When the switching frequency is pushed up to 400 kHz, to keep the same amount to current ripple, inductance could be reduced to 90uH, which results in 66% reduction in volume. In Table 2-1, the detailed comparison between these two inductors is summarized.



(a) 100 kHz PFC inductor (b) 400 kHz PFC inductor

Figure 2-5. PFC inductor for different switching frequencies.

Table 2-1. PFC inductor comparison for different switching frequencies.

Switching frequency	Kool Mu Core	Wire	Turns	Dimension (D×L)
100 kHz	77083 X 2	AWG16	49	1.57in X 1.14in
400 kHz	77059 X 4	AWG16	26	0.9in X 1.2in

From the comparison, effectiveness of increasing switching frequency is demonstrated. Although the higher switching frequency can largely increase the core loss density of the PFC inductor, due to less core material, the core loss only increases 4W. Meanwhile, due to the much shorter winding length caused by smaller core size and less turns, copper loss of PFC inductor is largely reduced. The loss comparison between two inductors is summarized in Table 2-2.

Table 2-2. Loss comparison between two PFC inductors.

Switching frequency	Core loss density	Core loss	Winding loss
100 kHz	2.11W/in^3	2.95W	2.51W
400 kHz	14.9W/in^3	7.14W	1.4W

2.3 Switching frequency impacts on EMI filter design

As demonstrated before, PFC inductor and EMI filter size occupies large portion of total converter volume. Although by increasing the switching frequency, PFC inductor size can be largely reduced, it is still questionable that the EMI filter size might be increased at higher switching frequency. Therefore, it is essential to design the EMI filters for different switching frequencies and exam the switching frequency impacts on EMI filter size.

2.3.1 EMI filter design procedure

For telecom and server applications, EMI standard EN55022 Class B is widely used, as shown in Figure 2-6. [B-3][B-4] The standard begins to regulate at 150 kHz. For the EMI noise frequency lower than 150 kHz, there is no regulation requirement. For the noise frequency between 150 kHz and 500 kHz, the limit level decreases from 66dBuV to 56dBuV linearly with the logarithm of the frequency. For EMI noise frequency between 500 kHz and 5 MHz, limit level is 56dBuV. For EMI noise frequency between 5 MHz to 30 MHz, limit level is 60dBuV. Because there is no EMI noise requirement for the noise frequency lower than 150 kHz, the EMI filter design can take the advantage of that.

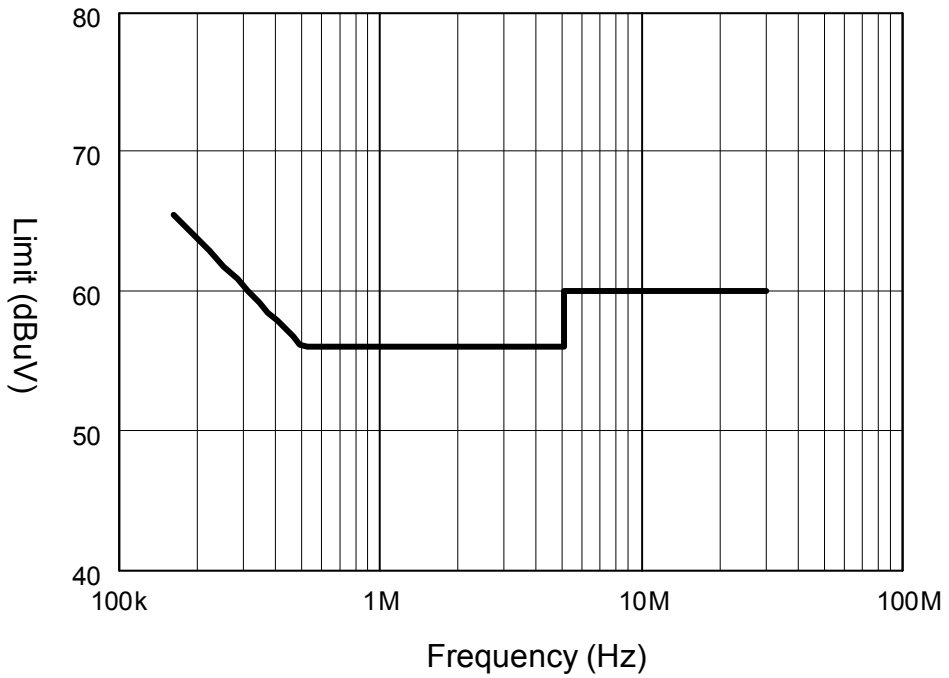


Figure 2-6. EN55022 Class B EMI standard.

To meet the EMI standard requirement, passive EMI filters are widely used [B-5]. Normally two-stage EMI filters are used because they can achieve higher attenuation comparing with single stage EMI filter. A typical two stage EMI filter is demonstrated in Figure 2-7.

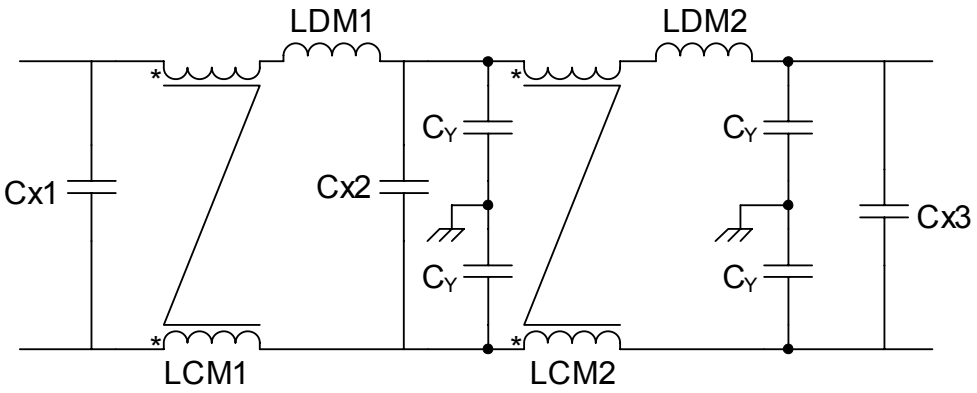


Figure 2-7. Two-stage EMI filter.

The filter is mainly constructed by common mode choke LCM1, LCM2 and corresponding X and Y capacitors. To achieve smaller filter size, leakage inductors of common mode chokes are used as different mode filter inductor LDM1 and LDM2. Because different noise transferring mechanisms, the two-stage EMI filter can be separated into differential mode (DM) filter and common mode (CM) filter.

Equivalent circuit of different mode filter is shown in Figure 2-8 (a). Because it has two inductors and three capacitors, its gain gains characteristic keeps -100dB/dec decreasing slop, which ensures higher attenuation at higher frequencies.

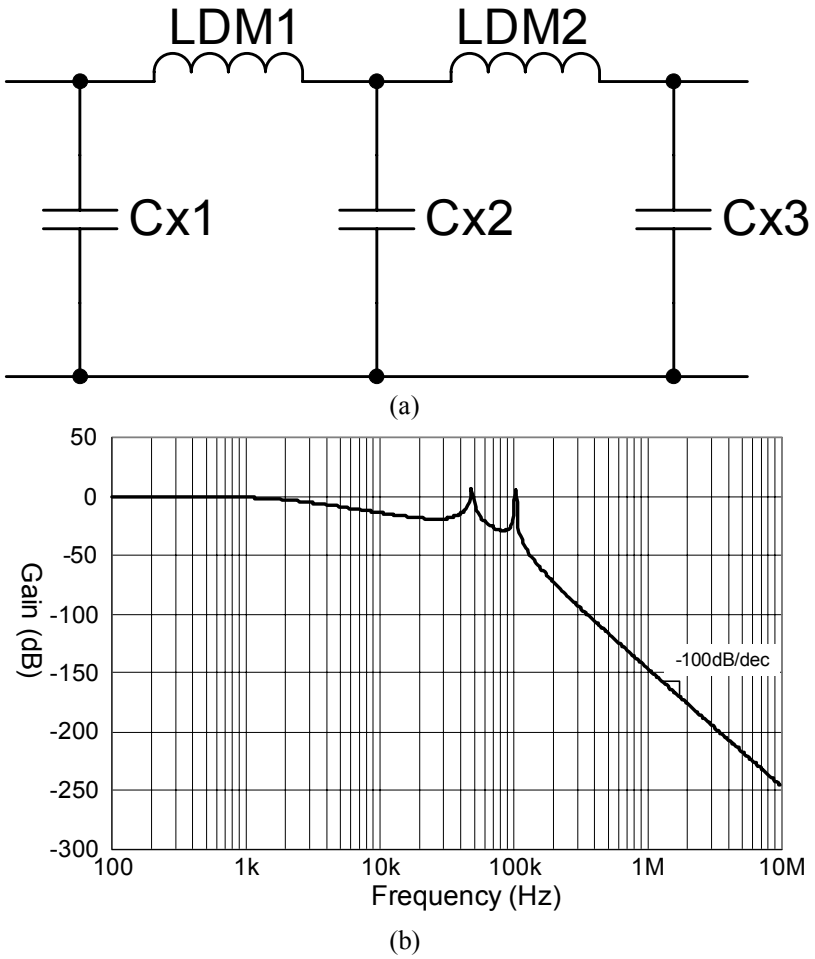


Figure 2-8. Two-stage differential mode filter; (a) Equivalent circuit, (b) Filter attenuation.

The equivalent circuit of the CM filter is shown in Figure 2-9 (a). Due to the two-L and two-C structure, gain characteristic of CM filter has a -80dB/dec decreasing slope, as shown in Figure 2-9 (b), which means higher attenuation can be achieved at high frequency range.

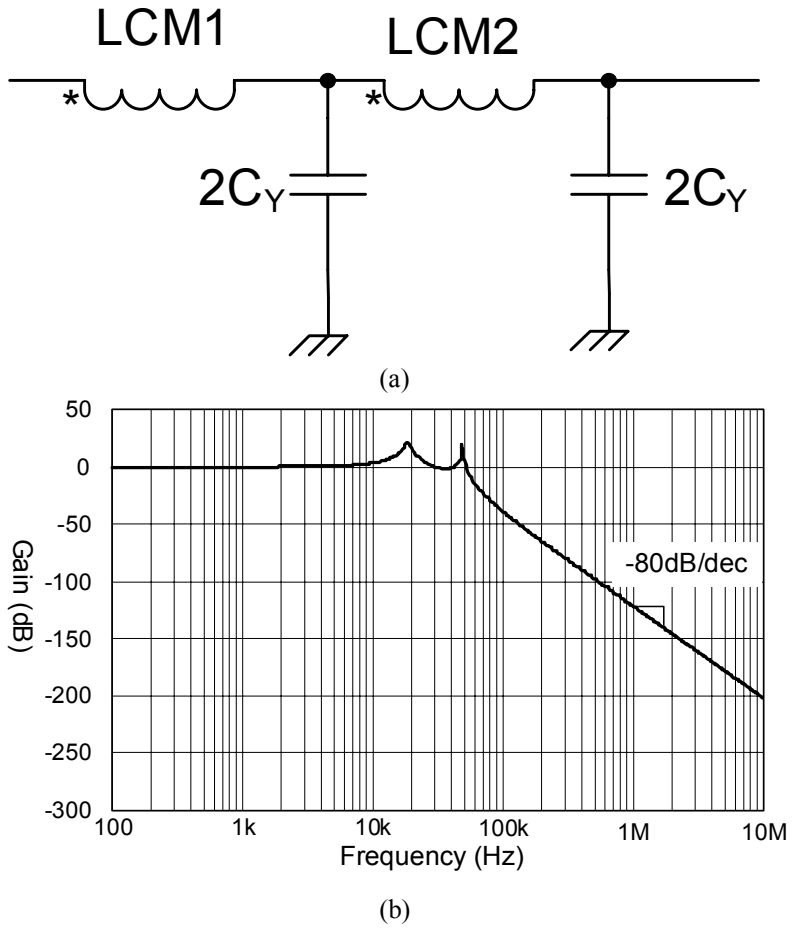


Figure 2-9. Two-stage common mode filter, (a) Equivalent circuit, (b) Filter attenuation.

The design of EMI filter is to achieve desired noise attenuation to make the filtered noise meet EMI standard requirement. Different EMI filter design methods have been proposed by several references. According to the method discussed in [B-6][B-7][B-8], the design of EMI filter can be simplified as three steps.

Firstly, the circuit operates without EMI filter. The base-line CM and DM noises (V_{CM} and V_{DM}) are measured through noise separator. After that, the

measured noises are compared with EMI noise standard to get the noise attenuation requirement curve for different frequencies.

Finally, the corner frequency of CM filter is obtained by drawing a 40dB/dec-slope line to tangent to the required CM attenuation curve. The horizontal intercept of the line and 0dB axis determines the CM filter corner frequency. According to this corner frequency, the filter components can be designed accordingly. Same design process can be used to design the DM filter. This 40dB/dec-slope is based on the assumption of single stage EMI filter. However, for the two-stage EMI filter, it is required to use 80dB/dec-slope for CM filter design and 100dB/dec-slope for DM filter design. Furthermore, the determined the corner frequency is the equivalent corner frequency, as illustrated in Figure 2-10.

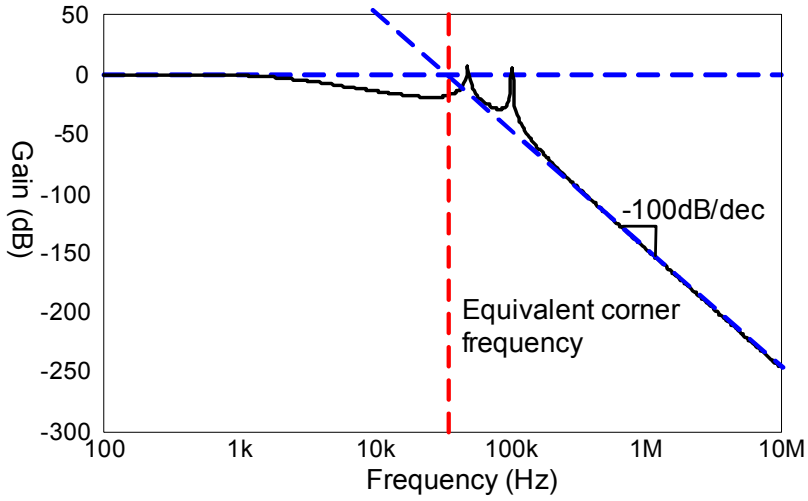


Figure 2-10. Equivalent corner frequency of two stage filter.

Although this equivalent corner frequency could represent infinite numbers of filters with different sizes, because of different filter design method, it is still can be used to evaluate the EMI filter size for the same filter design method. Higher equivalent corner frequency means smaller EMI filter size and higher power density.

Apparently, this design procedure assumes that the attenuation of EMI filter continuous increases with frequency. However, due to circuit parasitics, EMI filter attenuation decreases when the switching frequency is much higher than its corner frequency. Therefore, slightly modification might be required to meet the high frequency EMI specification. However, the EMI filter size is mainly determined by the low frequency noise.

2.3.2 EMI noise prediction of PFC circuit

Based on the described EMI filter design procedure, EMI filter can be designed with the measured CM and DM noise. To exam the switching frequency impacts on EMI filter, it is required to get the EMI noise for different switching frequencies. Since it is impossible to build the converters for all the frequency range, EMI noise of PFC circuit should be predicted by analytical model, which is much more time and cost effective.

During the past years, some research efforts have been executed to build the noise models to predict EMI performance of single switch CCM PFC circuit [B-

9][B-10][B-11][B-12][B-13]. Among different EMI noise prediction methods, the EMI noise is either calculated through time domain simulation or frequency domain calculation. Through simulation tools, EMI performance can be predicted and the effects of parasitic components can be analyzed. Most of the noise models are focus on precisely predicting the EMI performance of PFC circuit for whole conducted EMI frequency range. To accurately calculate the high frequency noise using time domain simulation, small simulation step and long simulation time are required. Thus, it is extremely time consuming and requires long data processing time. To reduce the simulation time, frequency domain simulation is proposed. Moreover, circuit parasitic components are required to be measured or extracted, because most of the circuit parasitic components, such as the trace inductances, will affect EMI noise at high frequency range.

According to the EMI filter design procedure, only low frequency noises are used to calculate EMI filter corner frequency. And those noise frequencies are the harmonics of the switching frequency. Therefore, the complex EMI model for PFC circuit is not necessary. Thus, instead of predicting the EMI performance for the whole conduction noise frequency range, a simplified EMI noised model can be used to predict the EMI noise for the switching frequency harmonics.

For conventional CCM PFC circuit with constant switching frequency and average current mode control, because of turning on and off of MOSFET, large EMI noise is generated. According to the different noise transferring mechanism,

the EMI noise can be separated into differential mode (DM) noise and common mode (CM) noise. DM noise is mainly affected by PFC inductor. And CM noise is determined by the parasitic capacitor between the MOSFET drain to the earth to ground. PFC circuit with parasitic capacitor is demonstrated in Figure 2-11.

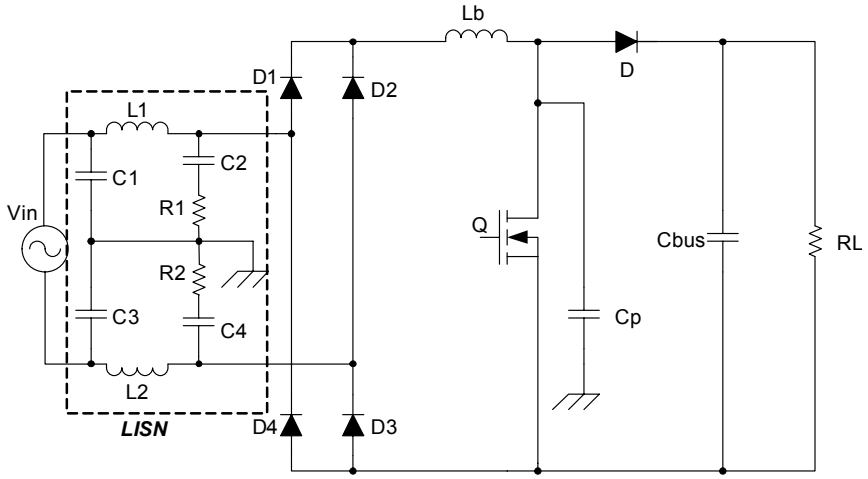


Figure 2-11. PFC circuit with LISN and parasitic capacitor.

In the circuit diagram shown in Figure 2-11, line impedance stabilize network (LISN) is the standard EMI measurement equipment, which can detect the EMI noise through LISN resistors R1 and R2. Because LISN inductors and capacitors construct a high pass filter, most of the EMI noise current goes through LISN resistors. Since the PFC circuit operates with CCM operation mode, input diode bridge can be ignored in the noise path. For the DM current transferring path, as demonstrated in Figure 2-12, includes the PFC inductor, switch circuit, LISN capacitors C2, C4 and LISN resistors R1, R2.

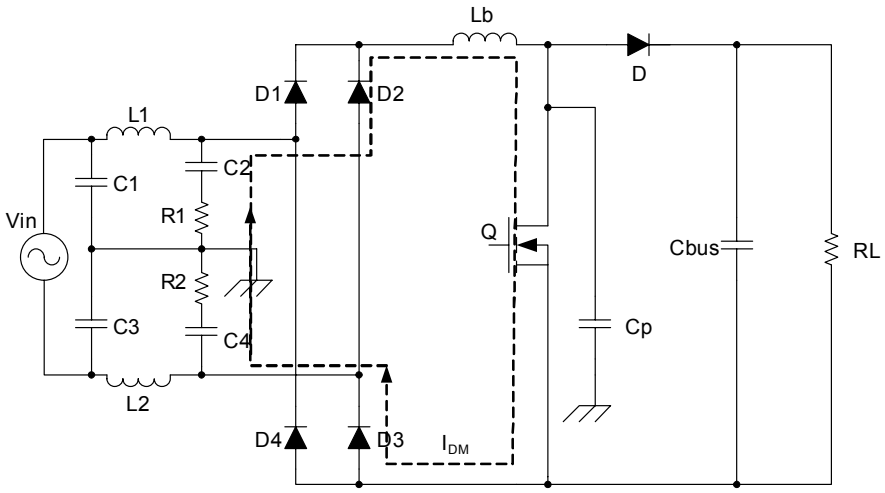


Figure 2-12. DM current transferring path.

As fort the CM current path, it includes the parasitic capacitor Cp, and LISN resistors. Because of large impedance of PFC inductor, most of CM current goes through the low-impedance negative bus. The CM current path is demonstrated in Figure 2-13.

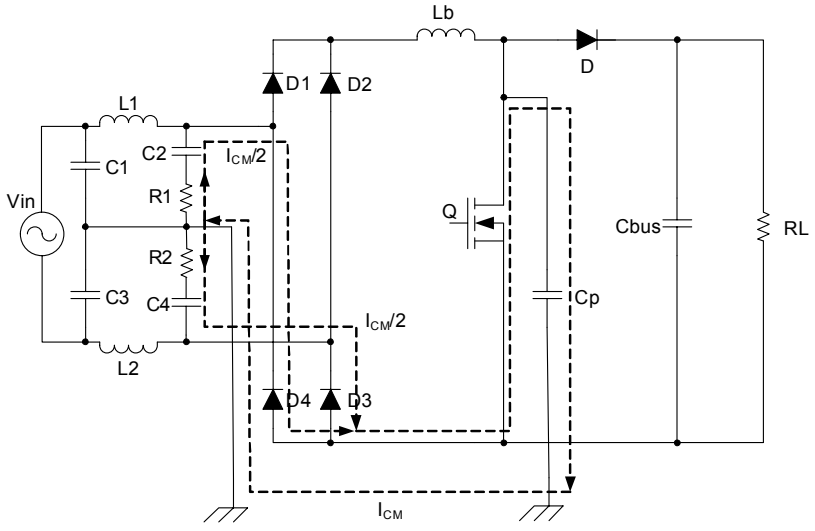
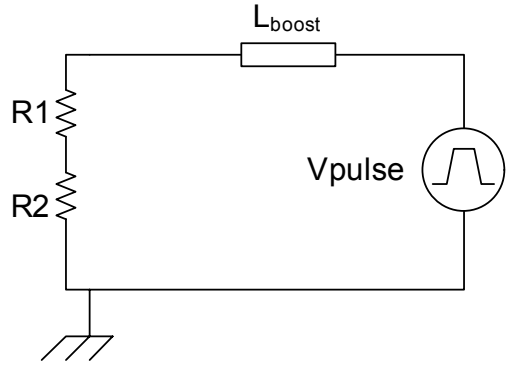


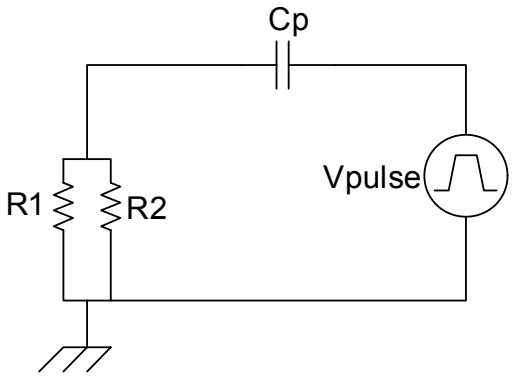
Figure 2-13. CM current transferring path.

Because of the switching of MOSFET, voltage across MOSFET drain to source is a pulse voltage, which pulsates from 0 to output voltage (400V). Its

rising time and falling time is much smaller than the switching cycle and depends on the driving circuit and the switching performance of MOSFET. Therefore, the MOSFET diode and output circuit can be represented by a pulse voltage. This pulse voltage is the noise source for both DM and CM currents. To predict the EMI noise, this pulse voltage source shouldn't have DC component. Meanwhile, for the conduction EMI frequency range 150 kHz to 30 MHz, the impedance of capacitor C2 and C4 are much smaller than 50Ω LISN resistor. Therefore, for the EMI noise transferring path, LISN can be considered as two resistors. By doing these simplifications, the equivalent circuit for calculating DM and CM current can be illustrated by Figure 2-14 (a) and (b), respectively.



(a) Equivalent circuit for DM noise



(b) Equivalent circuit for CM noise

Figure 2-14. Equivalent circuit for EMI noise.

Because PFC circuit has a regulated 400V DC output voltage, its duty cycle is determined by the relationship between input voltage and output voltage, and varies along the line cycle. Spectrum of the voltage source cannot be express by a simple equation. Therefore, Saber simulation is used to get the spectrum of the noise source, as demonstrated in Figure 2-15.

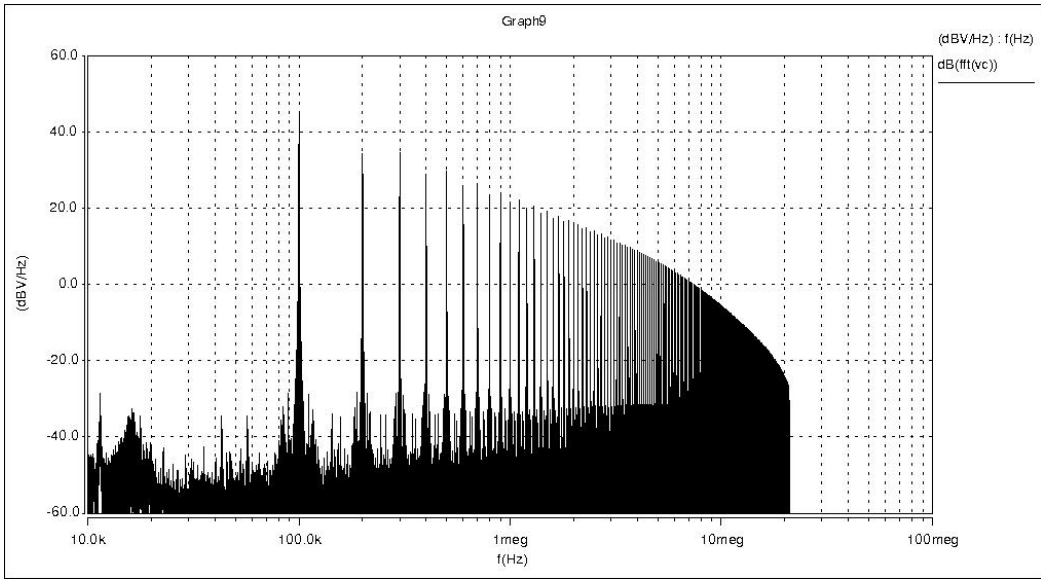


Figure 2-15. Spectrum of voltage source.

From the spectrum, it can be observed that, at switching frequency, the noise source has the amplitude of 45.4dBV. The switching frequency harmonics keeps -20dB/dec slope decreasing. Therefore, the noise source amplitude at harmonics of switching frequency can be derived as

$$V(nf_S) = 45.4 - 20\log(n) \text{ dBV}$$

In this equation, f_S is switching frequency and n is the harmonic order.

From the simulated spectrum, it also can be observed that at high frequency range, the enveloped changes into -40dB/dec, which is caused by the pulse voltage rise and fall time. However, for the EMI filter design, as described before, only the low frequency noise determines EMI filter components values and size. Therefore, the effects of rise and fall time can be ignored for this analysis, and the envelope of the voltage source can be simplified as a -20dB/dec slope, as demonstrated in Figure 2-16.

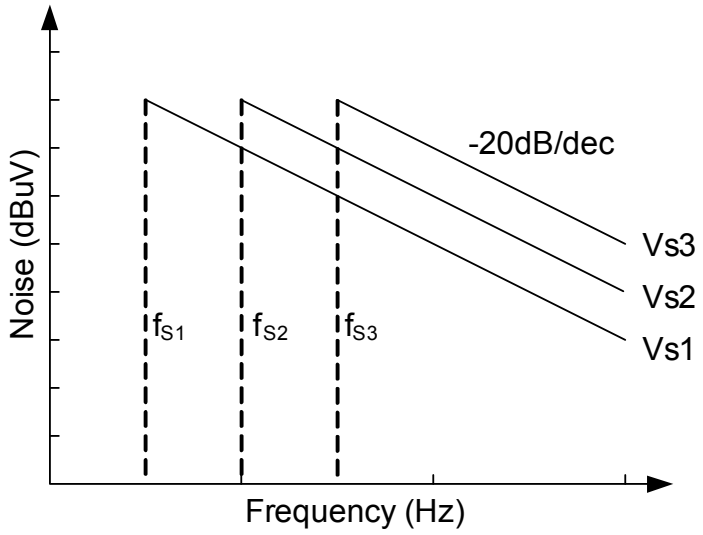


Figure 2-16. Spectrum envelope of PFC noise source.

Moreover, because the spectrum is only determined by the voltage level and duty cycle, when the switching frequency changes, the whole spectrum moves along the frequency axis but keeps the same level.

Based on the principle of superposition, the measured EMI noise on LISN resistors can be calculated used the noise source spectrum and the path impedance.

For DM noise, the path impedance is determined by the PFC inductor and LISN resistor. Because inductor impedance is proportional to the frequency, it has a 20dB/dec slope. For different switching frequencies, to keep the same ripple current, PFC inductor is reverse proportional to the switching frequency. Therefore, the loop impedance decreases with the increasing switching frequency.

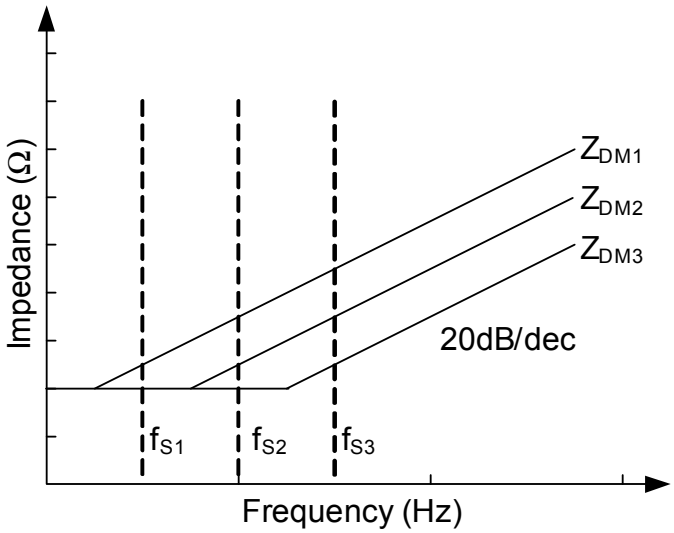


Figure 2-17. DM noise path impedance for different switching frequency.

The voltage across the LISN resistor is determined by the impedance of PFC inductor at switching frequency. Because the noise source spectrum has a -20dB/dec slope envelop and loop impedance has a 20dB/dec slope, the measured DM noise spectrum has a -40dB/dec envelope slope. Thus, DM noise level can be calculated as

$$\begin{aligned} V_{DM}(nf_S) &= V(nf_S) - 20\log(Z_{Lboost}) + 20\log(50) \\ &= 200 - 20\log(2\pi f_S L_{boost}) - 40\log(n) \end{aligned}$$

In this equation, the unit for the amplitude changes into dBuV and same as the standard required. Because the PFC inductor is inverse proportional to the

switching frequency, the switching frequency has no impacts on the amplitude of DM noise. As shown in Figure 2-18, DM noise spectrum envelope moves horizontally with different switching frequency, while keeps the same amplitude.

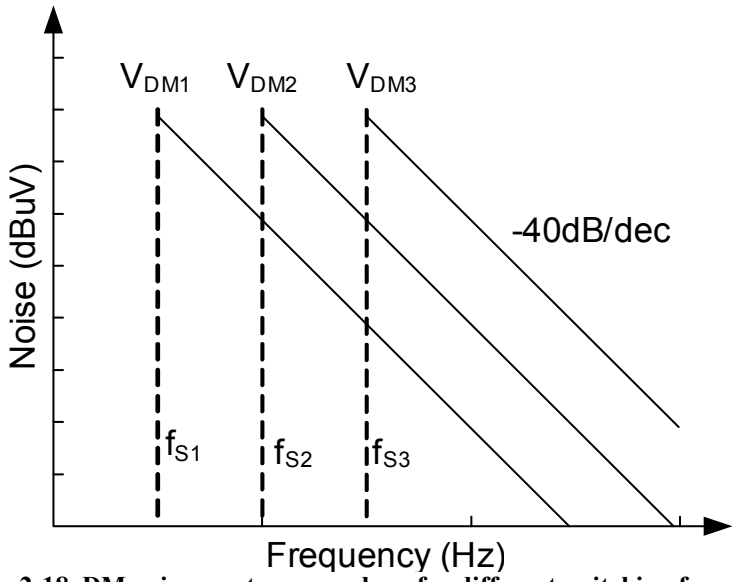


Figure 2-18. DM noise spectrum envelope for different switching frequencies.

For CM noise, the path impedance is determined by the parasitic capacitor between MOSFET drain to earth ground, and LISN resistors. Because the impedance of capacitor is reverse proportional to frequency, it has a -20dB/dec slope. Moreover, this parasitic capacitor is determined by the circuit layout. Therefore, the capacitor keeps similar for different switching frequencies. As shown in Figure 2-19, CM noise path impedance keeps the same for different switching frequencies.

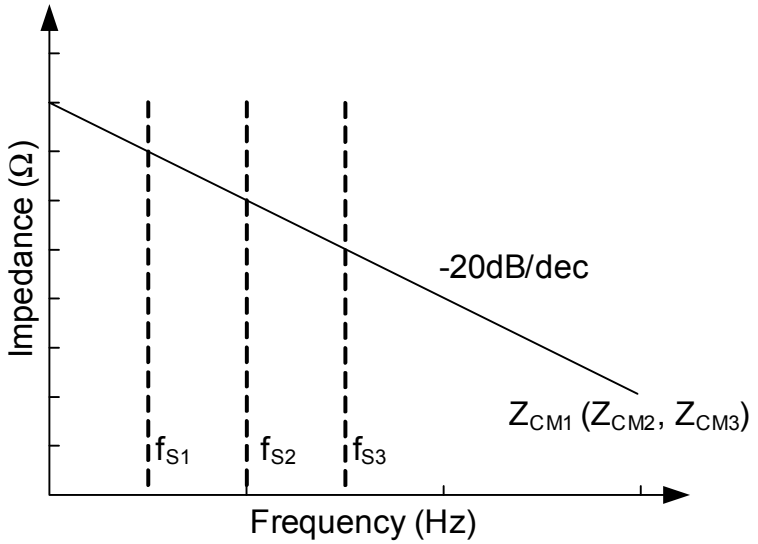


Figure 2-19. CM noise path impedance for different switching frequency.

Together with -20dB/dec slope of noise source spectrum envelope, CM noise should have a flat envelope. Because the CM current is evenly distributed into two LISN resistor, each LISN resistor sees half of CM current. CM noise amplitude can be calculated as

$$V_{CM}(nf_S) = V(nf_S) - 20\log(Z_{Cp}) + 20\log(25) = 193.4 + 20\log(2\pi f_S C_p)$$

In this equation, unite is also changed into dBuV and complied with the standard requirement. From the equation, CM noise envelope is proportional to the switching frequency. Furthermore, for different switching frequency harmonics, they keep the same amplitude.

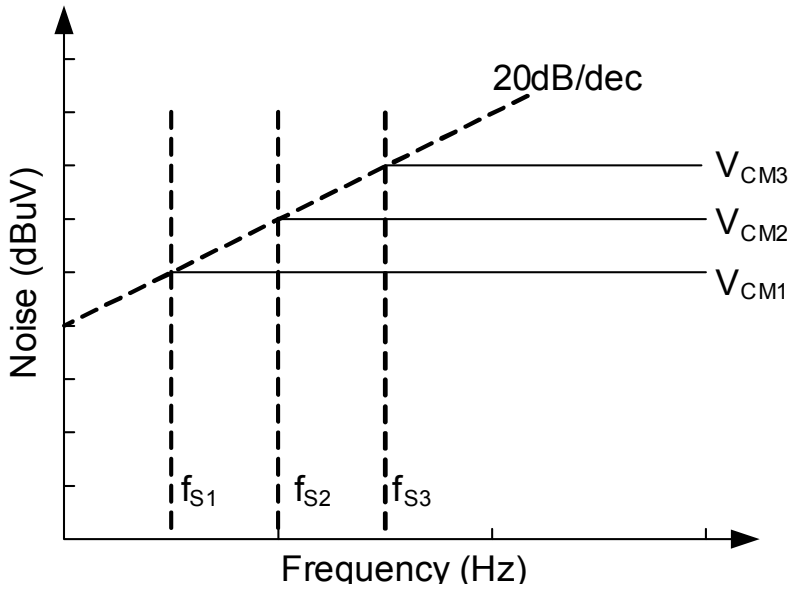


Figure 2-20. CM noise spectrum envelope for different switching frequencies.

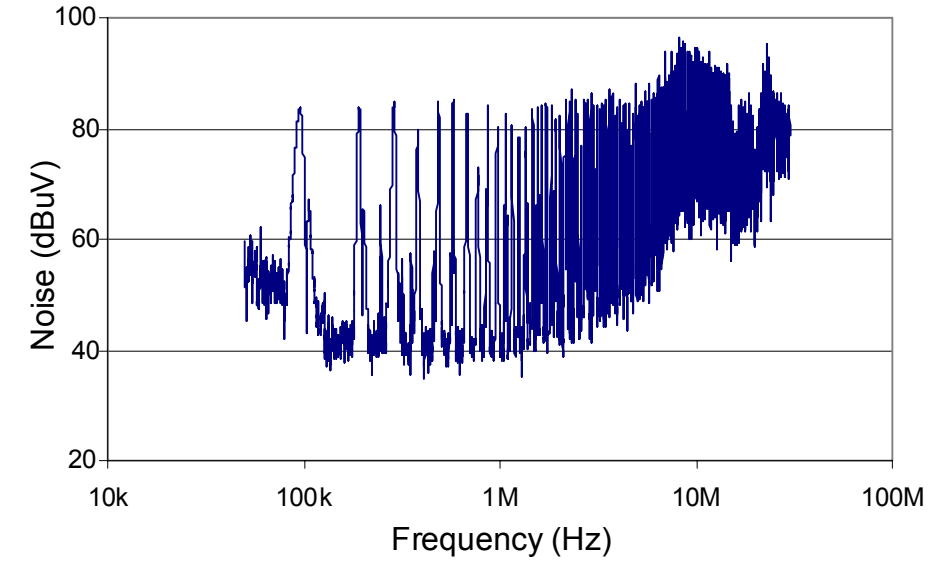
Apparently, these noise spectrum envelops only valid for the low frequency range, or in other words, the harmonics of switching frequency noises. It should not be used for high frequency noise prediction.

To verify the model, a 1kW, 100 kHz switching frequency single switch CCM PFC was built. The test data and predict data are shown in Table 2-3. The differential mode noise model can well predict the noise amplitude. Although there is several dBs error on the prediction noise, considering the design margin for the EMI filter, this simple equation can be used for the differential mode filter design for single switch CCM PFC circuit.

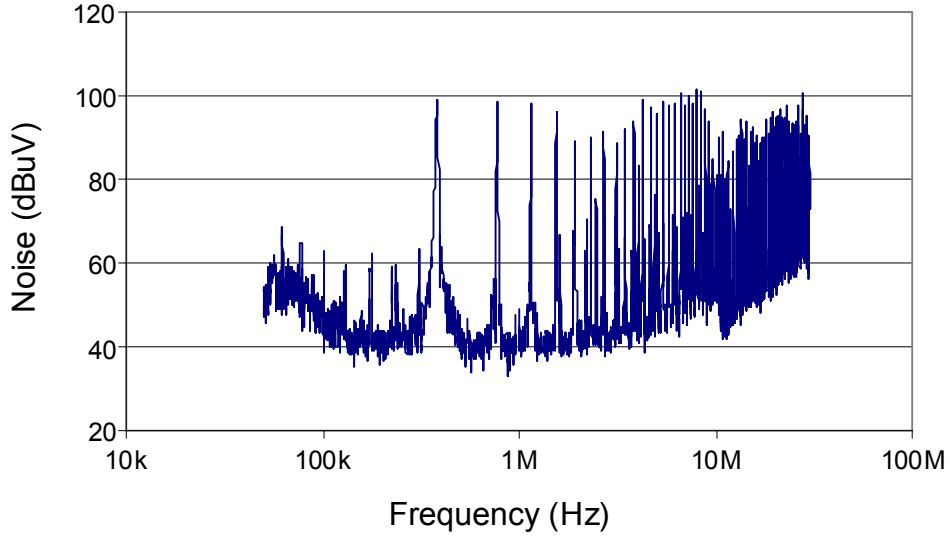
Table 2-3 . EMI model prediction vs. experimental results.

Frequency	100k	200k	300k	400k
Test Noise	149dBuV	127dBuV	131dBuV	121dBuV
Predict Noise	149.5dBuV	137dBuV	130dBuV	125dBuV

To verify the common mode noise model, the PFC circuit common mode noises at different switching frequencies are measured, as shown in Figure 2-21. From experimental results, it can be observed that all the common mode noises have flat envelope, and the amplitude is proportional to the switching frequency.



(a) 100 kHz switching frequency



(b) 400 kHz switching frequency

Figure 2-21. Measured common mode noise.

2.3.3 Filter size evaluation for different switching frequencies

Based on the described EMI filter design procedure, together with the predicted EMI noise for different switching frequencies, EMI filters for PFC with different switching frequencies can be designed accordingly.

CM and DM filters are designed separately. By comparing the predicted EMI noise with EMI standard, attenuation requirement for the EMI filter can be derived. According to the required attenuation and its corresponding frequency, the EMI filter can be designed. CM filter corner frequency is the intersection of 0dB and 80dB/dec-slope line tangent with attenuation requirement. DM filter corner frequency is the intersection of 0dB and 100dB/dec-slope line tangent with attenuation requirement. Because of the sharp slope of CM and DM filter attenuations, the tangent point is always the first switching frequency harmonic that has frequency higher than 150 kHz. Therefore, the EMI filter can be designed based on the noise of this harmonic.

We define the frequency that used to design the EMI filter as the **Worst Frequency**, which is the first noise frequency that is higher than 150 kHz. Because the EMI noise is the harmonics of switching frequency noise, the worst frequency should be the N^{th} switching frequency harmonic. Here N is an integer and should fulfill the equation.

$$(N-1)f_S < 150kHz \le Nf_S$$

Here, f_S is the switching frequency. The worst frequency can be calculated as

$$f_{worst}(f_S) = Nf_S$$

From this equation, when switching frequency is 70 kHz, the worst frequency should be the 3rd harmonic, which is 210 kHz. While for switching frequency is 80 kHz, the worst frequency should be the 2nd harmonic, which is 160 kHz. Therefore a slightly change on the switching frequency could cause big difference on EMI filter design. Relationship between switching frequency and worst frequency is shown in Figure 2-22. From this curve, it can be observed that the worse case frequency has dramatically changes around the frequencies that are fractures of 150 kHz, for the switching frequencies lower than 150 kHz. But when switching frequency is higher than 150 kHz, the worst frequency is always the switching frequency, and there will be no dramatically change.

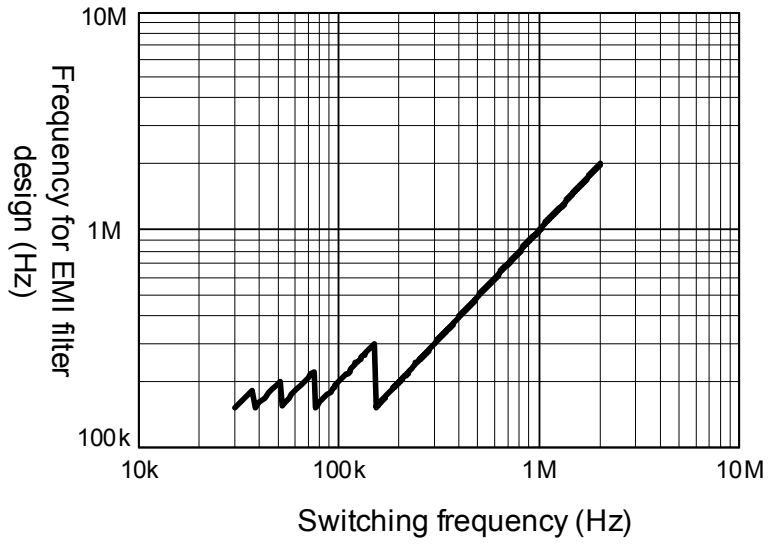


Figure 2-22. Worst frequency vs. switching frequency.

A) Differential mode filter

According to DM noise analysis, DM noise at switching frequency harmonics can be represented as

$$V_{DM}(nf_S) = 200 - 20\log(2\pi f_S L_{boost}) - 40\log(n)$$

Because the PFC inductor is designed based on the percentage current ripple, it is more convenient to calculate DM noise based on the ripple current.

To simplify the analysis, a 1kW PFC with universal input is considered as a design example. Because the PFC circuit derates at 150V AC input, the maximum current happens at 150V AC input. The maximum current is

$$I_{\max} = \sqrt{2}\frac{P_o}{V_{in}} = 9.43A$$

The maximum ripple current is set to be certain percentage of $I_{\max}$. If defining *ripple* as the percentage number, the maximum ripple current can be calculated,

$$I_{ripple} = ripple \times I_{\max}$$

According to the ripple current and switching frequency, DM noise can be represented by the ripple current as

$$V_{DM}(nf_S) = 164 + 20\log(ripple) - 40\log(n)$$

Therefore, DM filter attenuation requirement at worst frequency for different switching frequencies should be the difference between the DM noise and the EMI standard, as shown in the following equation.

$$Att_{DM}(f_{worst}) = \mathrm{V}_{\mathrm{DM}}(f_{worst}) - V_{\mathrm{lim}}(f_{worst}) + 6$$

To leave design margin 6dB attenuation is added. By using the derived equation, DM filter attenuation requirement for different switching frequency can be calculated, as shown in Figure 2-23.

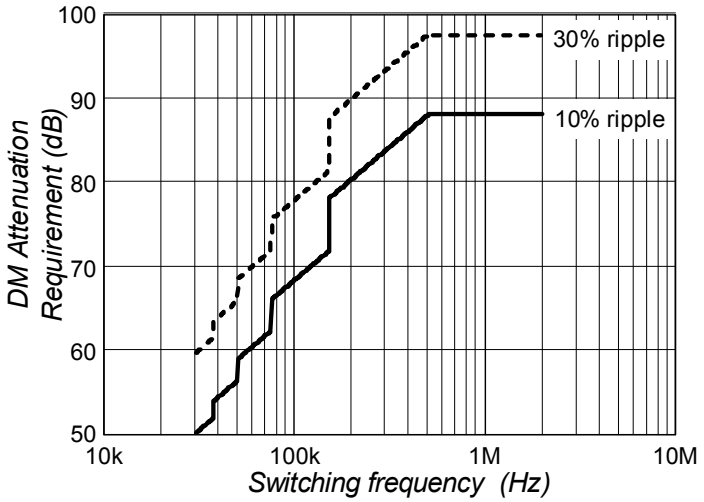


Figure 2-23. DM filter attenuation requirement.

Similar to the worst frequency, the attenuation requirement has dramatically change around switching frequency is equal to 50 kHz, 75 kHz and 150 kHz, etc. For instance, when the switching frequency is 70 kHz, filter design is based on the 3rd harmonic, which is 19dB lower than the switching frequency noise. However, when the switching frequency is 80 kHz, EMI filter design is based on the 2nd harmonic, which is only 12dB lower than the switching frequency noise. Because for different switching frequencies, once keeping the same current ripple, the switching frequency noise keeps the same amplitude. Therefore, attenuation required for 80 kHz switching frequency is much smaller than that for 70 kHz switching frequency.

According to the worst frequency and attenuation requirement, the equivalent corner frequency of DM filter can be calculated. The relationship between the required attenuation and the equivalent corner frequency can be demonstrated by

$$Att_{DM}(f_{worst}) = 100\log\left(\frac{f_{worst}}{f_{C\_DM}}\right)$$

Therefore, the equivalent corner frequency can be calculated as

$$f_{C\_DM} = f_{worst} \times 10^{-\frac{Att_{DM}(f_{worst})}{100}}$$

Based on this equation, the relationship between the required equivalent corner frequency and the switching frequency is shown in Figure 2-24. The curve is a zigzag shape. When the switching frequency is slightly lower than certain frequencies, such as 50 kHz, 75 kHz, and 150 kHz, the equivalent corner frequency of the EMI filter is much higher . This is caused by the combination of worst frequency change and attenuation requirement change. Therefore, a slightly change of the switching frequency could result in largely increase of EMI filter size. Thus, the PFC circuit switching frequency should keep slightly on the left side of those frequencies. Furthermore, when the switching frequency is higher than 450 kHz, the DM filter equivalent corner frequency will keep increasing and higher than those for other switching frequencies.

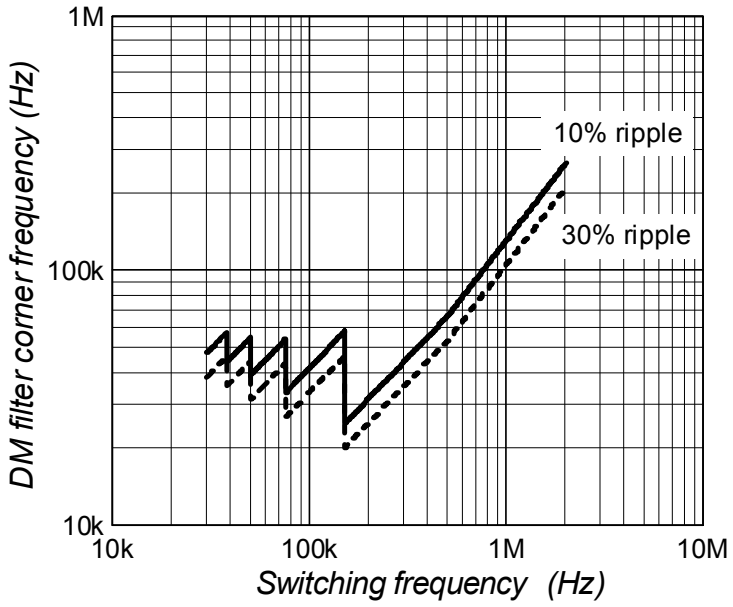


Figure 2-24. Corner frequency of DM filter vs. switching frequency.

B) Common mode filter

Following the same evaluation process, the common mode filter size can also be evaluated. According to previous analysis, CM noise amplitude for PFC circuit should be

$$V_{CM}(nf_S) = 193.4 + 20\log(2\pi f_S C_p)$$

From this equation, it can be observed that CM noise is proportional to the switching frequency and parasitic capacitor. For different switching frequencies, if keeping the similar layout, the parasitic capacitor keeps the same. Although it is difficult to get a specific capacitor value, several C_p values can be used to estimate its effects. Therefore, in the calculation, C_p is chosen as 100pF, 300pF and 500pF. Based on the common mode noise and EMI standard, together with CM noise amplitude, the required attenuation can be calculated as

$$Att_{CM}(f_{worst}) = \mathrm{V}_{\mathrm{CM}}(f_{worst}) - V_{\mathrm{lim}}(f_{worst}) + 6$$

Same as DM filter, 6dB design margin is added. As shown in Figure 2-25, the attenuation requirement for different switching frequency has the similar shape as DM filter. Moreover, larger the parasitic capacitor, higher the attenuation is required for CM noise.

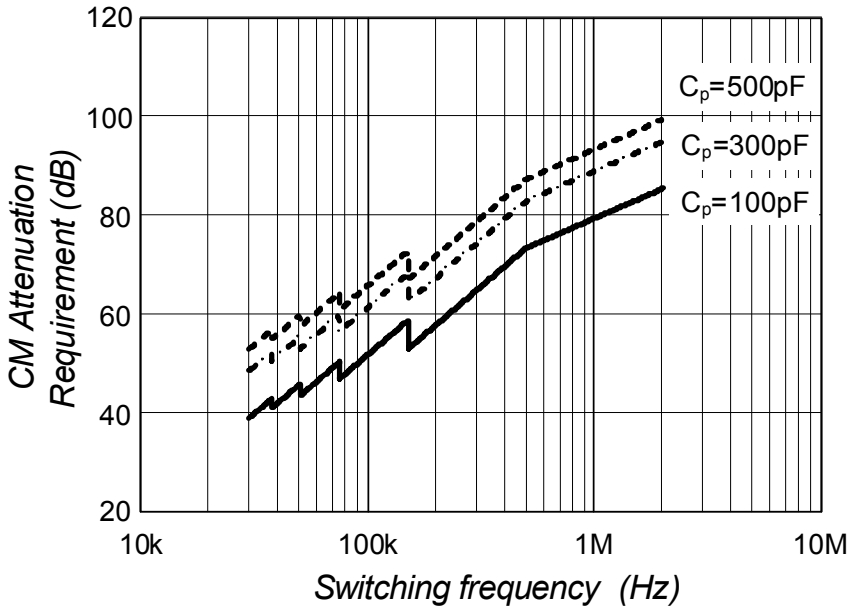


Figure 2-25. CM attenuation requirement.

According to the worst frequency and attenuation requirement, the equivalent corner frequency of CM filter can be calculated. The relationship between required attenuation and the equivalent corner frequency can be demonstrated by

$$Att_{CM}(f_{worst}) = 80\log\left(\frac{f_{worst}}{f_{C\_CM}}\right)$$

Therefore, the equivalent corner frequency can be calculated as

$$f_{C\_CM} = f_{worst} \times 10^{-\frac{Att_{CM}(f_{worst})}{80}}$$

Based on the worst frequency definition, attenuation requirement, together with -80dB/dec filter attenuation slope, the equivalent corner frequency of the CM filter can be derived, as demonstrated in Figure 2-26.

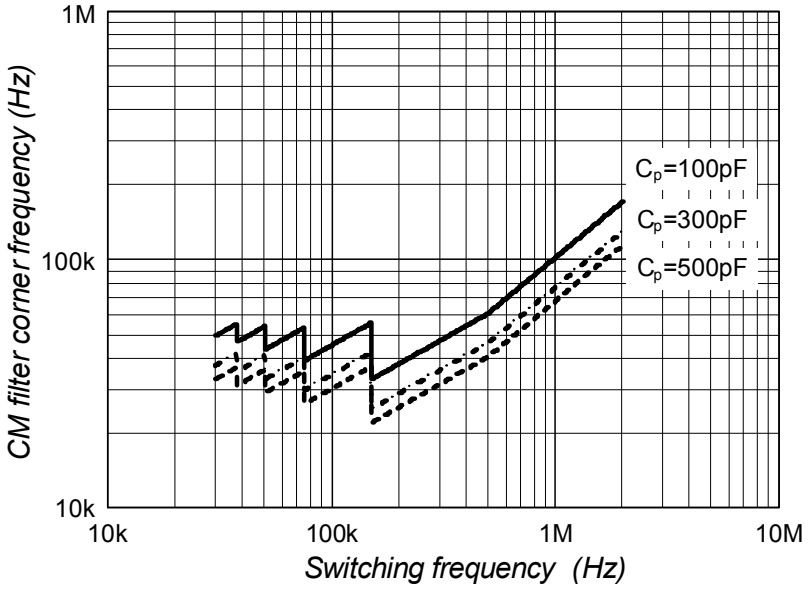


Figure 2-26. CM filter corner frequency vs. switching frequency.

From the derived curves, it can be clearly seen that the corner frequency of CM filter changes with different switching frequency. Similar to corner frequency for DM filter, CM filter corner frequency changes dramatically when the switching frequency is around the fractions of 150 kHz. It is desirable to have the switching frequency slightly lower than these frequencies, so that EMI filter size could be much reduced while maintain similar PFC inductor size. Furthermore, by pushing the switching frequency higher than 400 kHz, CM filter corner frequency begins to be higher than those for lower switching frequencies.

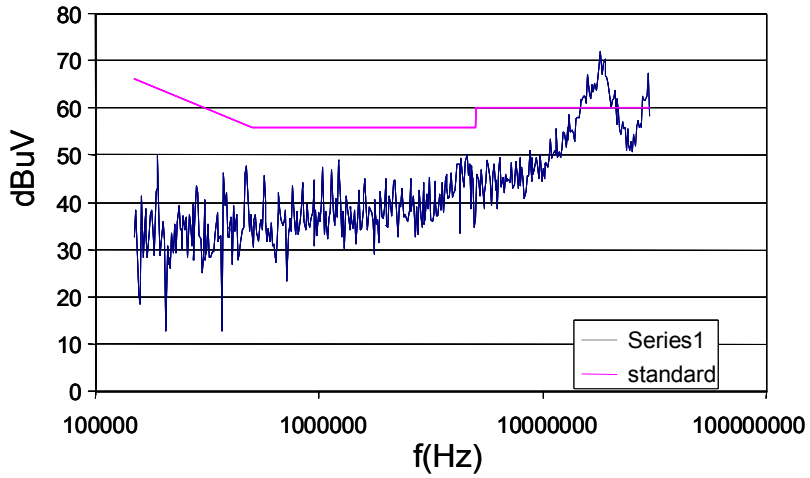
Therefore, to have a smaller EMI filter size, switching frequency of PFC circuit needs to be pushed up to 400 kHz and higher.

In previous analysis, parasitic capacitor Cp is the major concern for CM noise amplitude. By changing different Cp value, the impacts of parasitic capacitor can also be evaluated. From the calculated curves shown in Figure 2-26, with different Cp values, corner frequency curves move up and down while keep the same shape. Thus, the relationship between CM filter corner frequency and switching frequency keeps the same for different parasitic capacitors. Moreover, corner frequency reduces with the increasing of parasitic capacitor. Because larger the parasitic capacitor, higher the CM noise level, more CM filter attenuation is required. For the same CM filter structure, CM filter corner frequency has to be reduced to achieve higher attenuation. From this analysis, it can be conclude that the parasitic capacitor should be kept smaller to achieve smaller EMI filter size.

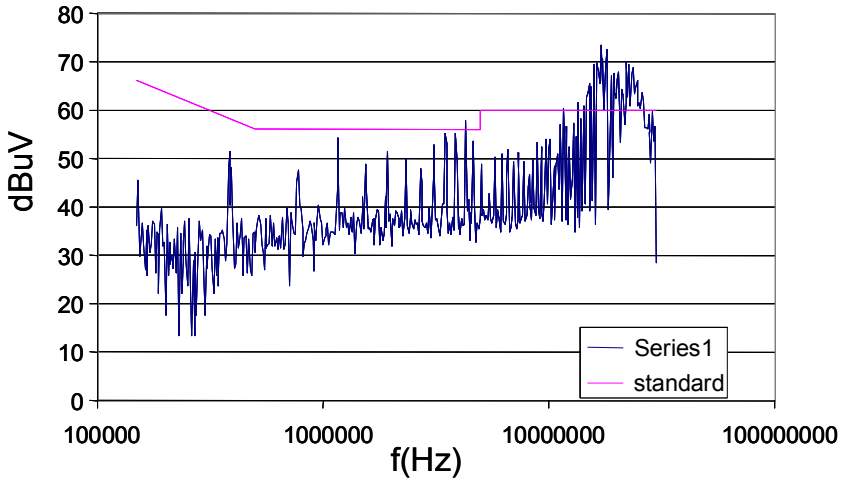
2.3.4 Experimental verification

After the theoretical analysis, two single switch CCM PFC circuits were built, with 100 kHz switching frequency and 400 kHz switching frequency, respectively. Two EMI filters were designed for the converters to meet the EMI standard EN55022 Class B. As shown in Figure 2-27, both of the converters can meet the standard at the low frequency range, which is EMI filter design criteria. The prototypes for two EMI filters are shown in Figure 2-28, 35% volume reduction is achieved by pushing the switching frequency from 100 kHz to 400

kHz, which verifies the theoretical analysis. Because the parasitic effects of the EMI filter have the detrimental effects on the EMI filter performance, especially at the high frequency range, it can't meet the EMI standard at high frequency range. The problem can be solved by using other methods such as grounding and shielding technologies.

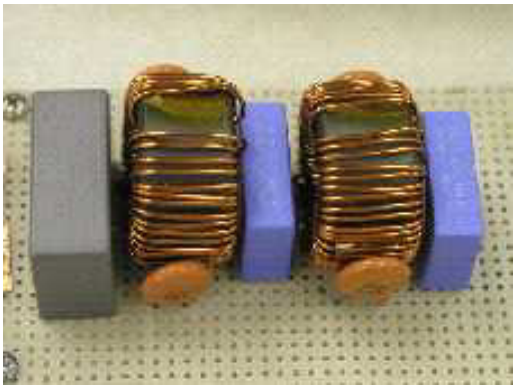


(a) 100 kHz switching frequency

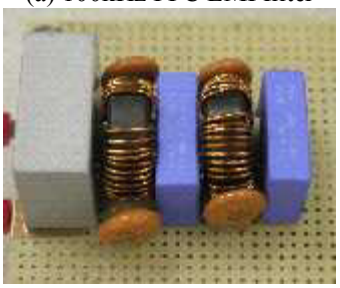


(b) 400 kHz switching frequency

Figure 2-27. EMI noise after filtering for different switching frequencies.



(a) 100kHz PFC EMI filter



(b) 400 kHz PFC EMI filter

Figure 2-28. EMI noise after filtering and EMI filter size comparison.

2.4 Further benefits brought by high switching frequency

So far, it is clear that the switching frequency can shrink EMI filter size and reduce the PFC inductor size through inductor value reduction. However, not only the PFC inductor value is important for PFC circuit, which determines the input current ripple, its impedance also important, especially for the EMI performance at high frequency range [B-14]. Based on the PFC circuit operation principle, DM noise equivalent circuit for PFC circuit is shown in Figure 2-29. From the equivalent circuit, it is quite clear that the EMI noise of the circuit will be largely affected by the characteristic of the PFC inductor. As shown in Figure 2-30, the impedance of the 100 kHz switching frequency PFC inductor and the measured EMI noise are demonstrated.

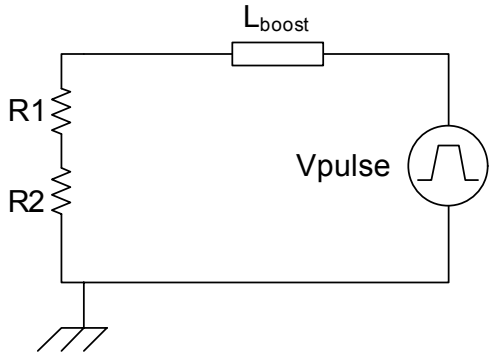
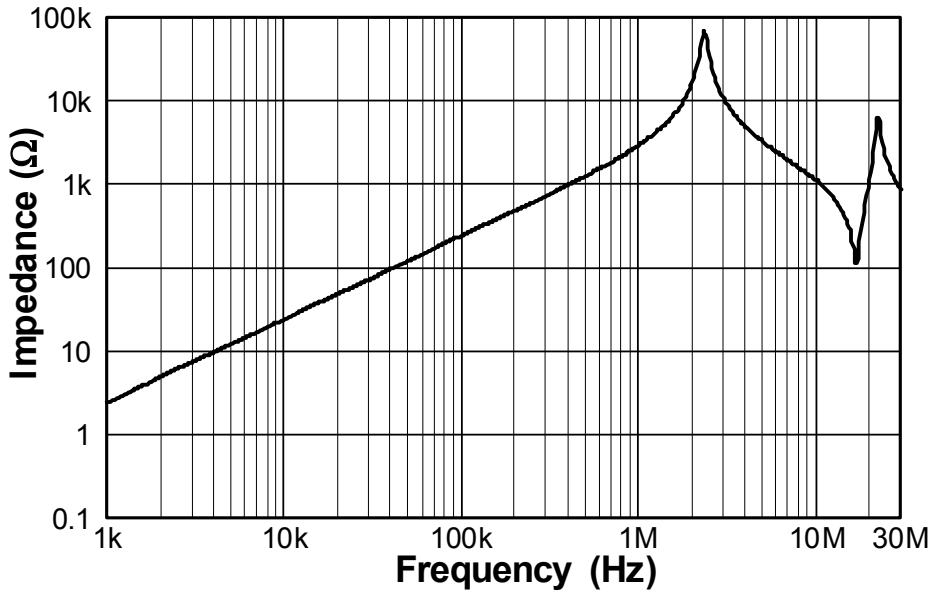
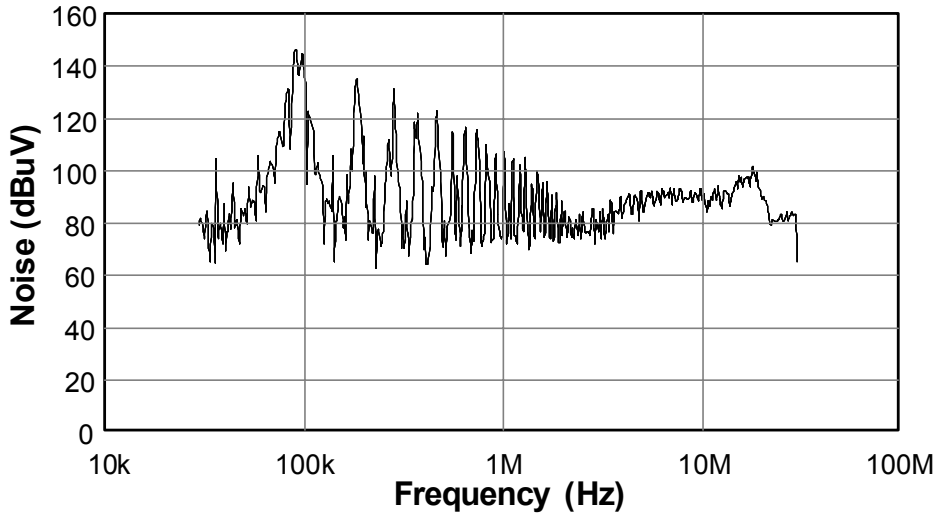


Figure 2-29. Equivalent circuit for DM noise modeling.

It can be clearly seen that there is a noise peak at about 18 MHz. At the corresponding frequency, the Boost inductance impedance reaches its valley value because of the resonance of PFC inductor parasitic components. From this experimental result, by controlling the PFC inductor parasitic, it is possible to reduce the high frequency noise peak for PFC circuit.



(a) PFC inductor impedance



(b) Measured EMI noise

Figure 2-30. 100 kHz switching frequency PFC.

Due to the reduction of PFC inductor value, not only the PFC inductor size, but also the inductor property changes. For the PFC inductors shown in Figure 2-5, their impedances are shown in Figure 2-31. Due to different switching frequency, 400 kHz PFC inductor has much smaller inductor value.

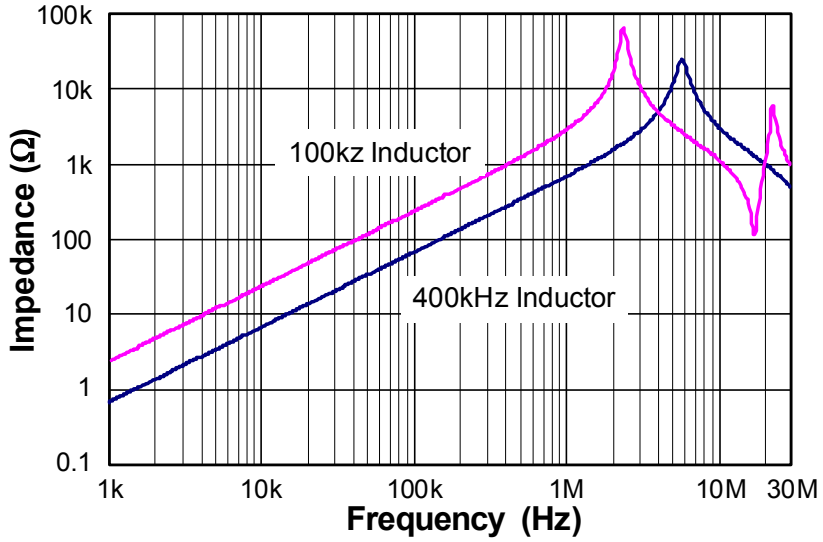


Figure 2-31. Impedances for two PFC inductors for different switching frequencies.

It can be observed that for the PFC inductor working at 100 kHz, there is a resonant frequency at about 18MHz. At this frequency, the impedance of the PFC inductor is small. Therefore, the EMI noise at corresponding frequency is high, which can be seen in Figure 2-32. But for PFC inductor working at 400 kHz switching frequency, from the impedance curve, the resonant valley frequency is pushed higher than 30MHz, which means, at the conducted EMI standard required frequency range, there will be not high EMI noise peak as shown in 100 kHz switching frequency case. The experimental results show that the PFC circuit operating at 400 kHz will not show the high noise peak at high frequency.

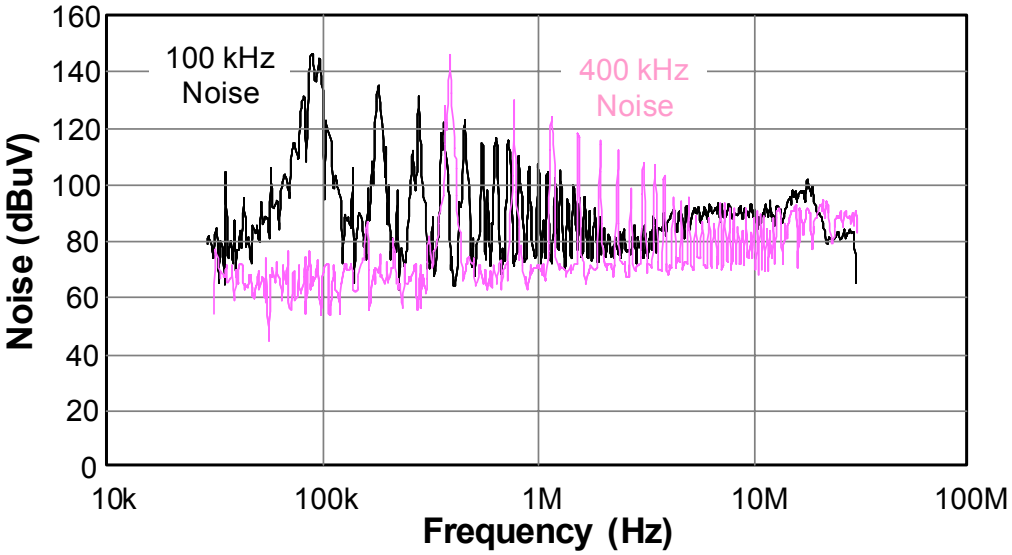


Figure 2-32. EMI noise comparison between two different switching frequencies.

As it is well known, due to circuit parasitics, attenuation of the EMI filter will not keep decreasing with the increasing of the frequency. Normally, EMI filter attenuation will dramatically decrease at the high frequency range. Therefore, it is important to eliminate the high frequency noise peak. From the experimental

results, it can be clear seen that the benefit brought by pushing the switching frequency higher.

2.5 Summary

In this chapter, switching frequency impacts on PFC circuit have been demonstrated through theoretical analysis and experimental results.

Switching frequency impacts on PFC inductor is quite clear. PFC inductor is inverse proportional to the switching frequency. Higher switching frequency results in less inductor value and smaller inductor size. From the experimental demonstration, when switching frequency is pushed from 100 kHz to 400 kHz, PFC inductor size could be reduced by 65%.

However, the switching frequency impacts on EMI filter is not that straightforward. Based on the analysis of DM and CM noise of PFC circuit at different switching frequencies, together with EMI filter design procedure, PFC EMI filters at different switching frequencies are analyzed. The equivalent corner frequency is used to evaluate the EMI filter size. The higher corner frequency means smaller EMI filter size.

From the derived the DM and CM filter corner frequency curves for different switching frequencies, due to the EMI standard begins to regulate at 150 kHz, corner frequency for DM and CM changes dramatically at the switching

frequencies that are fractions of 150 kHz, such as 50 kHz, 75 kHz and 150 kHz, etc. Thus, it is not necessarily to have a smaller EMI filter size with higher switching frequency. Moreover, to have smaller EMI filter size, switching frequency should be chosen as slightly lower than these frequencies. Furthermore, when switching frequency is higher than 400 kHz, EMI filter size will keep decreasing and smaller than those for lower switching frequencies. The experimental results demonstrated that by pushing switching frequency from 100 kHz to 400 kHz, EMI filter size could reduce 35%.

Beside the size reduction on PFC inductor and EMI filter, high switching frequency could bring extra benefit on the EMI noise. For low switching frequency PFC, due to large parasitic on PFC inductor, high noise peak appears at high frequency range. When PFC circuit operates with much higher switching frequency, because of the lower PFC inductor value and less parasitics, high noise peak can be eliminated inside conduction EMI noise frequency range, which was demonstrated by experimental results.

Chapter 3. PFC Topologies Evaluation for High Switching Frequency

3.1 Introduction

For distributed power systems (DPS), high power density, low profile begins to be the standard approach. Since the size of passive components of the converters decrease with the increasing of the switching frequency, to achieve higher power density, converters are operating at increasingly switching frequencies. In chapter 2, based on the analysis on the switching frequency impacts on PFC circuit, PFC converter can achieve power density benefits by pushing the switching frequency higher than 400 kHz.

Although the power density benefits can be realized by using higher switching frequency, it is till questionable if PFC is able to operate at such a high switching frequency. For conventional PFC circuit, as discussed in chapter 2, because of the continuous conducting current, large diode reverse recovery current exists. Therefore, PFC circuit has large switching loss and is not able to operate at high switching frequency. Furthermore, due to the large conduction loss caused by input diode bridge and large MOSFET on-state resistance, PFC efficiency is low, especially at low input line condition. Therefore, to ensure converter thermal handling capability, derating during low input is widely used in commercial products.

When PFC is operating at high switching frequency, major issue is the switching losses generated during switching transient period. Although conduction loss almost keeps the same for different switching frequencies, switching loss increases proportionally to the switching frequency. Thus, to enable the converter operate at higher switching frequency, switching loss must be reduced. In the part years, tremendous efforts have been performed to improve PFC circuit switching loss as well as conduction loss [C-1]~[C-14].

Semiconductor device performance is the major barrier for further improve PFC circuit. Large reverse recovery loss, large conduction loss can both be improved by using better devices. With the development of semiconductor devices, some major breakthroughs show up recently. SiC Schottky diode completely removes the diode reverse recovery current. Super junction MOSFET has much faster switching speed and lower on-state resistance, comparing with conventional MOSFET. All these makes PFC circuit operate with much smaller switching loss and conduction loss [C-11]~[C-14].

Besides semiconductor improvement, all kinds of soft switching technologies, lossless snubber topologies have been developed. By employing different auxiliary circuit, soft switching can be achieved, which results in much smaller loss. However, due to the complexity of the topology and extra loss caused by the auxiliary circuit, they are seldom used n the products [C-1]~[C-10].

Meanwhile, several alternative PFC topologies have been developed and show the benefits of loss reduction, such as the three-level PFC and Dual Boost PFC. For three-level PFC circuit, because the voltage stress on semiconductor devices is half of the output voltage, low voltage rating devices can be used to achieve smaller conduction loss and switching loss. Furthermore, by using range switch, input diode bridge conduction loss can be reduced to half, which can further improve the converter efficiency. For Dual Boost PFC, although it has same switching loss comparing with conventional PFC, because it removes the input diode bridge, less conduction loss enables the circuit operates with higher frequency while maintaining similar efficiency [C-15][C-16][C-17].

In this chapter, based on the loss breakdown of conventional single switch PFC, key components contributing to low efficiency are identified. Through the theoretical analysis and experimental results, different efficiency improvement methods have been evaluated, which include new semiconductor devices, three-level PFC with range switch and Dual Boost PFC. All these solutions show the potential of enabling PFC circuit operate with high switching frequency and maintain high efficiency.

3.2 High frequency opportunity of Conventional PFC

For front-end AC/DC converters, due to the regulation of power factor and input current harmonics, power factor correction (PFC) stage is the standard approach. Among different PFC topologies, the single switch CCM PFC (conventional PFC) is the most widely used topology because of its simplicity and smaller EMI filter size. The circuit topology is shown in Figure 3-1.

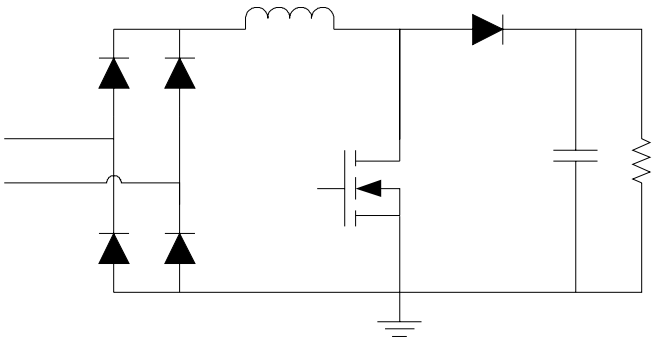


Figure 3-1. Single Switch CCM PFC.

The circuit is constructed by an uncontrolled diode-bridge rectifier and a Boost DC/DC stage. By adjusting Boost converter duty cycle, input current shape can be controlled and meets the current harmonic standard (EN61000-3-2) requirement. Meanwhile, due to input and output power balancing, output voltage can also be regulated. Although the converter can achieve power factor correction with simple structure, due to the continuous current conduction mode (CCM), Boost diode is forced turning off by MOSFET turning on. Large switching loss is generated because of series reverse recovery current. Furthermore, because the switching devices need to handle the full output voltage 400V, high voltage rating

MOSFET and diode are used. Comparing with low voltage rating devices, high on-state resistance and worse switching performance damages the circuit performance and reduces efficiency.

Both the switching loss and conduction loss are getting sever when the input line drops to the low input line, especially the minimum voltage of 90V AC. A 1kW single switch CCM PFC with 100 kHz switching frequency is built to evaluate the converter performance. With conventional MOSFET IRFP460A and fast recovery diode RHRP860, the converter efficiency for different input line is measured and summarized Figure 3-2.

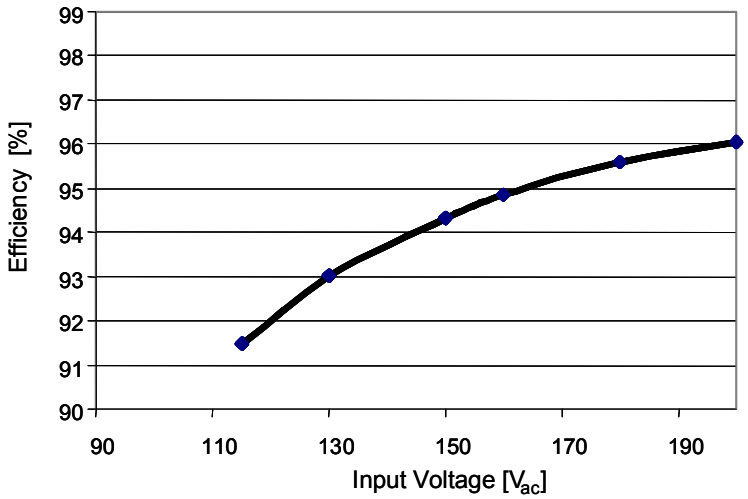


Figure 3-2. Efficiency for 1kW single switch PFC with 100 kHz switching frequency.

The efficiency of the PFC circuit drops below 91% when the input line is 110V. Due to thermal runway, the measurement couldn't be finished at 90V input. However, if following the trends of efficiency changing, converter efficiency will be much lower than 90% when the input line is 90V. However, at high input line, the circuit can maintain a much higher efficiency as 96%. Since

the converter efficiency drops dramatically with the decreasing of input line, it is necessary the breakdown the loss to reveal the key components for loss reduction. The converter loss breakdown for different input line is shown in Figure 3-3.

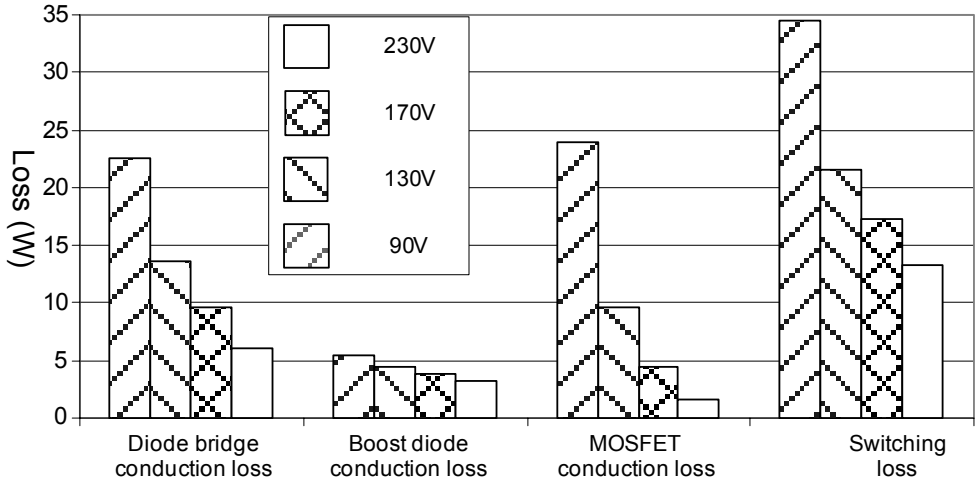
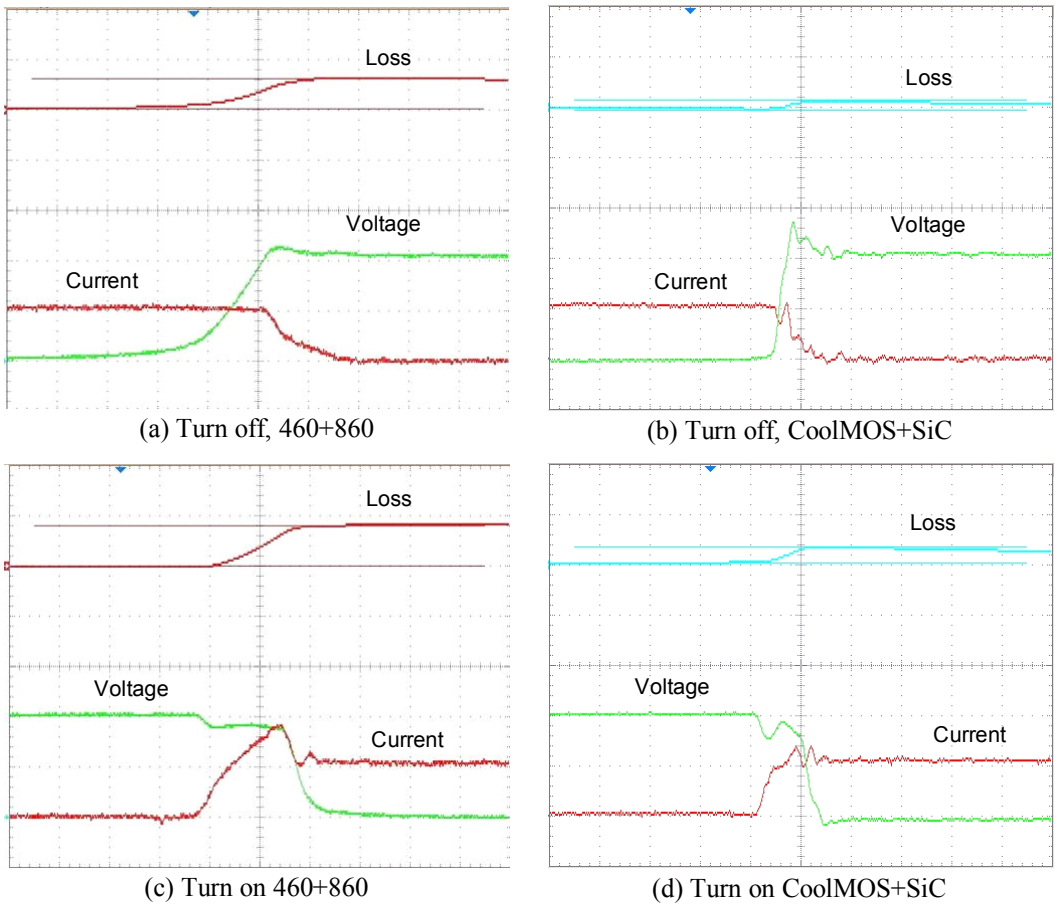


Figure 3-3. Loss breakdown for 100 kHz, 1kW PFC with IRFP460A and RHRP860.

From the loss breakdown, switching loss, conduction loss of MOSFET and Diode Bridge are the main contributors. Especially MOSFET conduction loss, it increases more than 8 times, when input voltage drops form 230V to 90V.

To allow PFC circuit operating at higher frequency, switching loss must be reduced, by either using better performance devices, or other circuit topologies. Recently developed super junction MOSFET (CoolMOS^{TM}) and SiC Schottky diode, greatly improve the switching performance of MOSFET and diode. The switching waveforms using conventional MOSFET IRFP460A and Si-based fast recovery diode RHRP860, comparing with CoolMOS^{TM} SPW20N60C3 and SiC Schottky diode SPD06S60, are summarized in Figure 3-4.



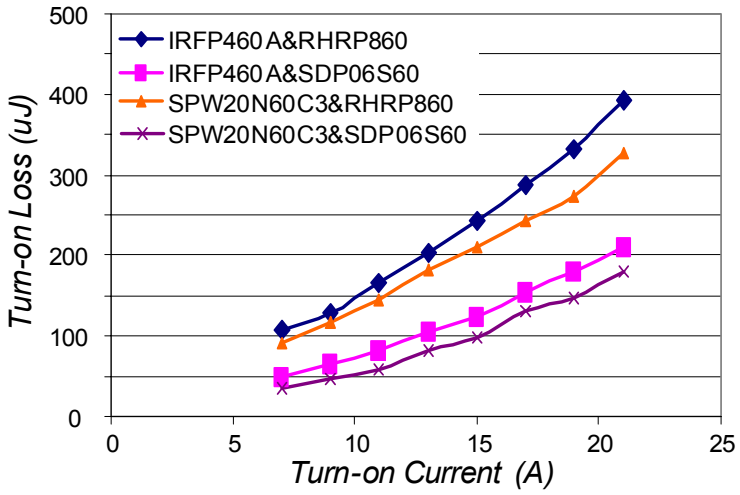
(a) Turn off, 460+860 (b) Turn off, CoolMOS+SiC

(c) Turn on 460+860 (d) Turn on CoolMOS+SiC

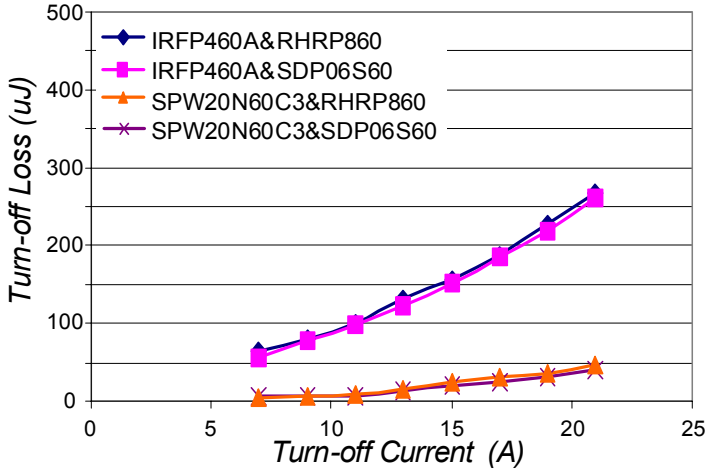
Figure 3-4. Switching Waveform comparison (20nS/div, 200V/div, 20A/div, 400uJ/div).

From the experimental results, it can be clearly seen that the switching time is much reduced. Therefore, the switching loss caused by voltage and current overlapping is much improved. Moreover, from turn-on waveforms of conventional devices, large reverse recovery current can be observed, which is caused by the hard turn-off of Si-based fast recovery diode. However, the CoolMOS^{TM} and SiC diode combination shows that the reverse recovery current is entirely removed by the SiC Schottky diode. Thus, much smaller turn-on loss is expected on MOSFET.

By changing the switching current, switching loss at different load conditions can be explored. The measured data are summarized in Figure 3-5. For different load conditions, by using CoolMOS™ and SiC diode, 60% turn-on loss reduction and 80% turn-off loss reduction can be achieved.



(a) Turn-on loss



(b) Turn-off loss

Figure 3-5. Switching loss comparison for different device combinations.

From device performance evaluation, it can be observed that switching loss is greatly improved by using these new devices. Therefore, PFC circuit efficiency is expected to be much improved. Efficiency comparison of 100 kHz 1kW

conventional PFC with different devices are summarized in Figure 3-6, PFC efficiency can be improved to 92.5% at 90V input, which is much higher comparing with conventional devices. In this set of curves, only the combination of CoolMOS™ and SiC diode is able to operate with full power without thermal run-away.

Moreover, the device technology keeps improving, and recently developed newest version of CoolMOS™ can achieve 99mΩ on state resistance and better switching performance, which can further improve PFC circuit efficiency. As shown in Figure 3-6, by using newest devices, low line efficiency can be increased to 95.5%.

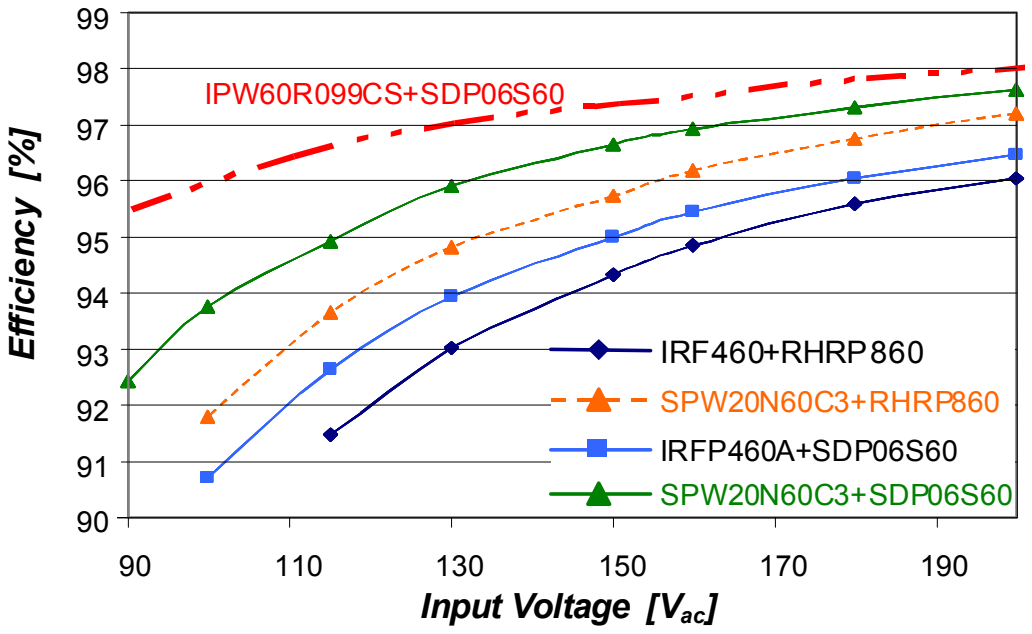
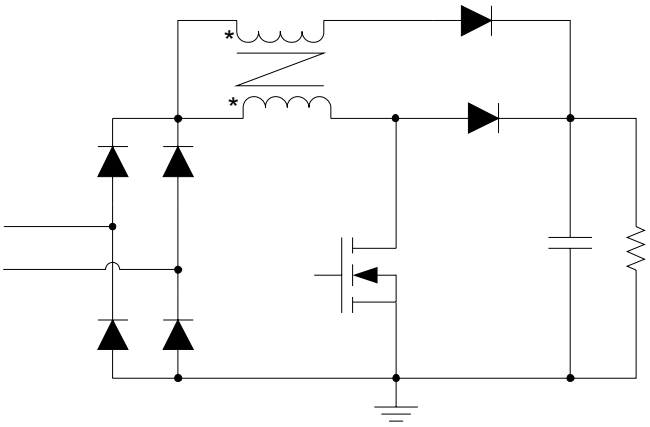


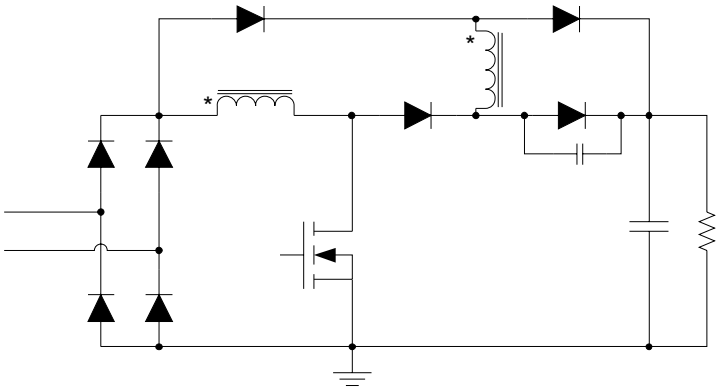
Figure 3-6. 100 kHz 1kW PFC efficiency using different devices.

Because switching loss is much reduced by using these new devices, the switching frequency of PFC circuit is allowed to be much higher comparing with

using conventional devices. In this way, the benefits of EMI filter and PFC inductor size reduction can be realized. To verify the high switching frequency capability, a 400 kHz 1kW PFC using CoolMOS^{TM} (SPW20N60C3) and SiC diode (SDP06S60) was built. Meanwhile, two 1 kW PFC circuits with different lossless snubbers operating at 100 kHz using conventional devices (IRFP460A and RHRP860) are set as the benchmarks, because these circuit can well control the switching loss on conventional PFC circuit and achieve high efficiency. The circuit diagrams are shown in Figure 3-7. More detailed discussion about these two topologies could be found in Reference [C-9] and [C-10].



(a) Lossless snubber using current steering



(b) Lossless snubber with improved current steering

Figure 3-7. PFC circuit with different lossless snubbers.

From the experimental results shown in Figure 3-8, 400 kHz PFC can achieve higher efficiency comparing with PFC circuit using conventional devices. Therefore, the power density of PFC circuit can be much improved. As shown in Figure 3-9, by pushing the switching frequency up to 400 kHz, 35% size reduction on EMI filter and 65% size reduction on Boost inductor can be achieved.

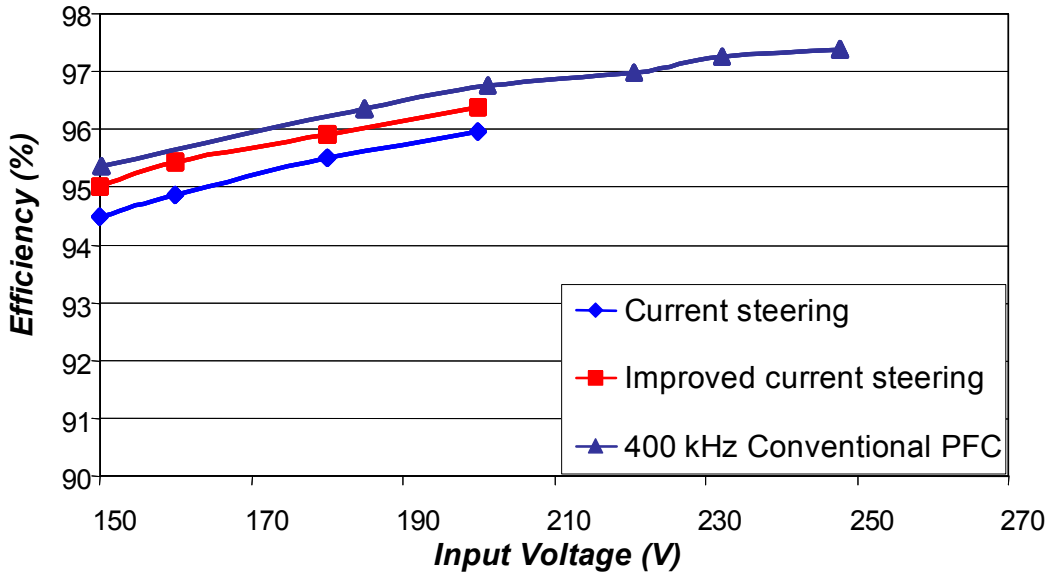
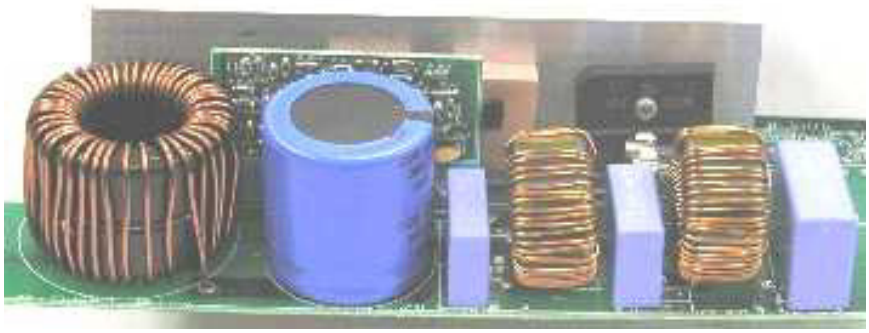


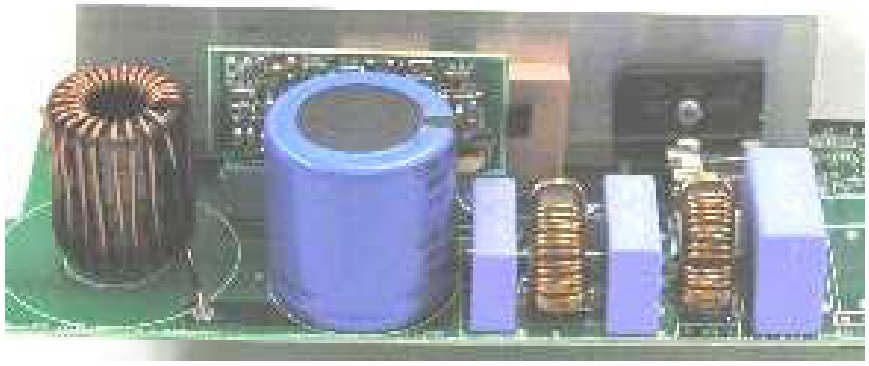
Figure 3-8. Efficiency of high frequency PFC.

Although PFC circuit switching loss can be greatly reduced by using these new devices, from loss breakdown results, the conduction loss on the MOSFET and input diode bridge is also server issue for the PFC circuit especially for low input line voltage. It is also desirable to reduce the converter conduction loss and improve efficiency. Since power density of power converter is eventually determined by thermal handling capability. By reducing the conduction loss, it

will allow PFC circuit operate at higher switching frequency while reduce the Boost inductor and EMI filter size.



(a) 100 kHz PFC



(b) 400 kHz PFC

Figure 3-9. Hardware comparison of PFC circuit with different switching frequencies.

Because PFC circuit operates at continuous conduction mode, anytime, there are three semiconductors in the conduction path: two diodes from Diode Bridge, MOSFET or diode in Boost stage. Meanwhile, the forward voltage drop on the diode is about 1V for different conditions. Therefore, severe conduction loss is generated at low input line. From the loss break down, it can be clear seen that input diode bridge contributes more than 20W loss at 90V input line. Instead of using conventional PFC topology, three-level PFC with range switch and Dual

Boost PFC are able to remove one semiconductor from conduction path and improve efficiency. Besides, by using three-level structure, three-level PFC can use low voltage rating devices as the switching components, together with its interleaved switching control, converter efficiency can be further improve for all the input lines.

In the following section, these two topologies are evaluated through theoretical analysis and experiments.

3.3 PFC topologies evaluation for high switching frequency

3.3.1 Three-level PFC

For conventional PFC circuit, due to the simple Boost converter structure, the MOSFET and diode have to have the voltage rating higher than the output voltage. Normally 500V MOSFET and 600V fast recovery diode are used as the switching devices. However, these devices have high conduction loss, as well as the large switching loss due to the high voltage ratings. Instead of using simple Boost structure, three-level Boost converter can be used to enable of using lower voltage rating devices. The circuit topology is shown in Figure 3-10, three-level Boost structure is used to replace the simple Boost converter [C-18].

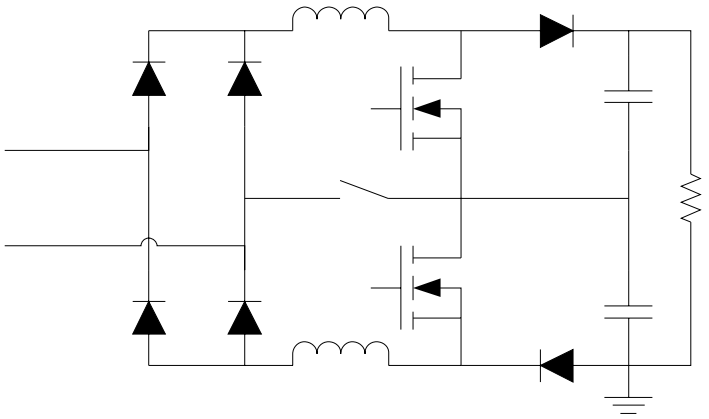


Figure 3-10. Three level PFC with range switch.

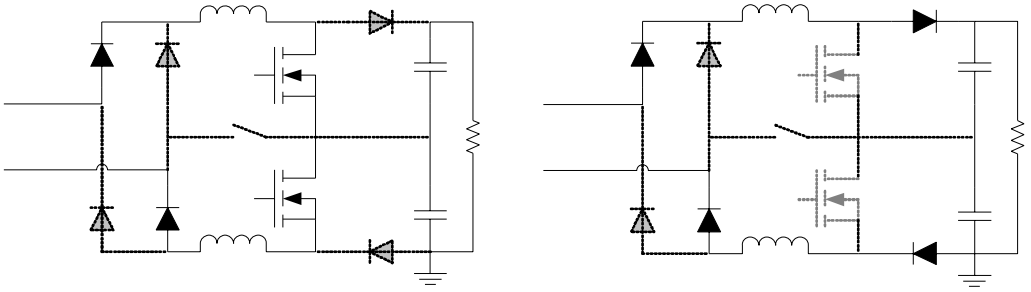
Keeping the same output voltage at 400V, instead of using 500V devices, 300V devices can be used, which means much better conduction and switching performance. Moreover, a range switch is used to generate the voltage doubler structure. By using the voltage doubler, converter low line efficiency can be dramatically improved. Because of the range switch, operation principles of the converter can be differentiated as the high input line and low input line.

A. High input line operation

When the input voltage is high line, from 180V to 260V AC, the range switch is turned off. At this input line, two different control methods can be used to achieve power factor correction.

Two-level control method is a simple control method. Both of the switches are turned on and off at exactly the same time. The equivalent circuits for switches on and off are shown in Figure 3-11. When the switches are turned on, the Boost

inductor is charge through two MOSFET. When switches are turn off, the Boost inductor is discharged though the whole output voltage.



(a) Equivalent circuit when switch on (b) Equivalent circuit when switch off

Figure 3-11. Two-level control method for three-level PFC.

In this operation mode, the inductor is charged by the input voltage and discharged by the different between the input voltage and output voltage. Comparing with the control of conventional PFC circuit, the only modification is to change the driver from driving one device into driving two devices. Thus the converter control design can be the same as the conventional PFC and achieved same amount of current ripple with same Boost inductor value.

The relationship between ripple current and Boost inductor value can be derived as

$$i_{ripple} = \frac{|v_{in}|}{L} dT_S = \frac{T_S}{L}\left(|v_{in}| - \frac{v_{in}^{\ 2}}{V_o}\right)$$

The ripple current changes along the line cycle, and can be represented as Figure 3-12. Ripple current reaches its maximum value when input voltage instantaneous value is 200V.

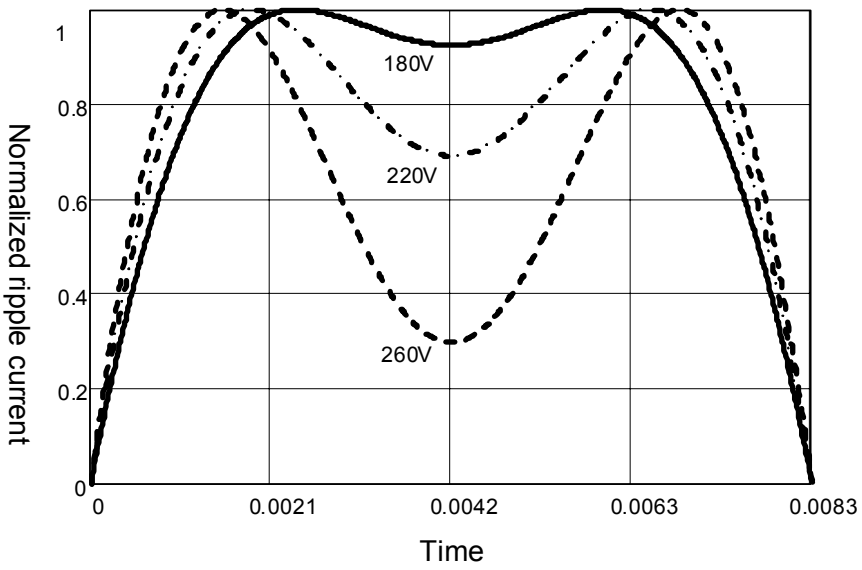


Figure 3-12. Inductor ripple current for different input line with simple control method.

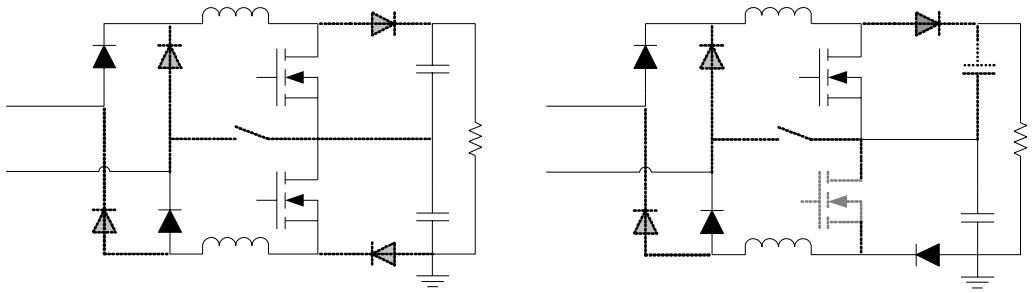
However, by modifying the operation mode, three-level control method can largely reduce the volt-second on Boost inductor. Therefore the switching frequency can be reduced or inductor value can be reduced to achieve same amount of current ripple. However, three-level control method is much more complex comparing with two-level control. Three-level control method can be explained as following.

When input voltage instantaneous value is less than half of the output voltage, Boost inductor is charged through both of the MOSFET and discharge through half of the output voltage, as shown in Figure 3-13 (a) and (b). When the instantaneous input voltage is higher than half of the output voltage, the inductor is charged through one of the output capacitors, and discharged through the whole output voltage, as shown in Figure 3-13 (c) and (d). The operation principle can be summarized in Table 3-1.

Table 3-1. Different control method for three-level PFC at high input line.

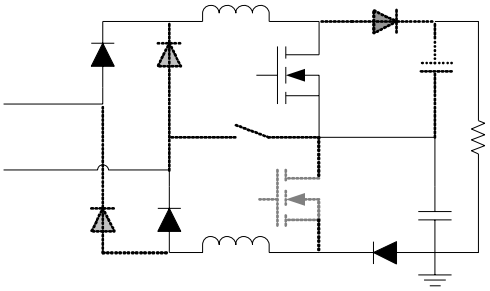
Instantaneous input voltage	Inductor voltage	
	Charging inductor	Discharging inductor
Less than Vo/2	v_{in}	$\frac{V_o}{2} - v_{in}$
More than Vo/2	$v_{in} - \frac{V_o}{2}$	$V_o - v_{in}$

The equivalent circuit for three-level converter operates at high input line is shown in Figure 3-13. By adjusting the duty cycle of the two MOSFETs, the two different operation modes can be changed automatically.

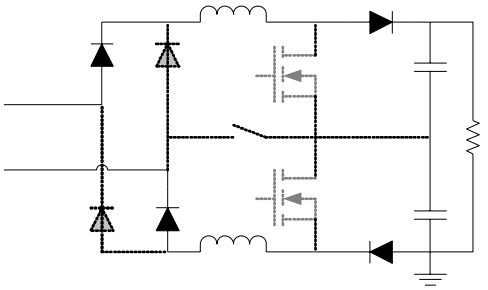


(a) Charging inductor ($v_{in} < V_o / 2$)

(b) Discharging inductor ($v_{in} < V_o / 2$)



(c) Charging inductor ($v_{in} > V_o / 2$)



(d) Discharging inductor ($v_{in} > V_o / 2$)

Figure 3-13. Equivalent circuits for three-level PFC.

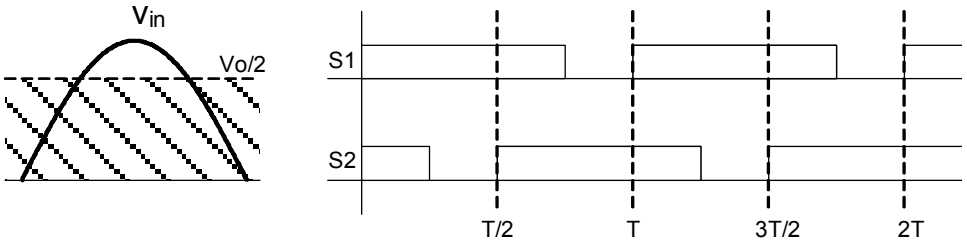
When instantaneous input voltage is less than Vo/2, Boost inductor charges through two MOSFETs and discharged by half of the output voltage. Thus, when instantaneous input voltage is less than 200V, the duty cycle should be

$$d = 1 - \frac{v_{in}}{V_o}$$

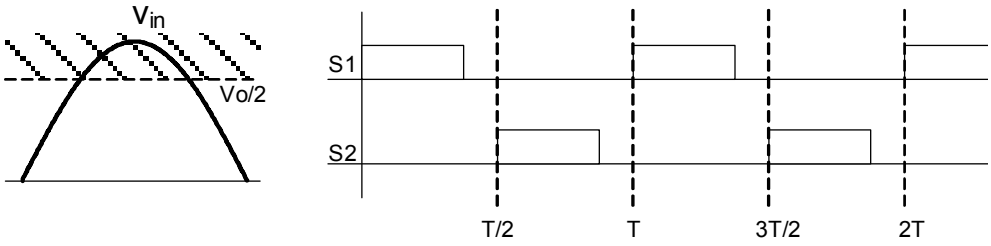
When input voltage instantaneous value is higher than 200V, Boost inductor is charged by half of the output voltage and discharged by the whole output voltage. Thus, when instantaneous input voltage is higher than 200V, the duty cycle should be

$$d = 1 - \frac{v_{in}}{V_o}$$

Therefore, for different instantaneous input voltage values, the control law keeps the same, which means these two operation modes can be automatically switched. The PWM signal for the two MOSFET can be summarized in Figure 3-14. For different input voltage instantaneous voltages, the duty cycle of two switches changes accordingly.



(a) Instantaneous input voltage less than 200V



(b) Instantaneous input voltage higher than 200V

Figure 3-14. Gate signals for two MOSFETs.

After calculating the duty cycle, the inductor current ripple can be estimated. The equations for estimating the inductor ripple for different time instance are

$$i_{ripple} = |v_{in}|(1 - \frac{|v_{in}|}{V_o}) \qquad \text{if} \qquad |v_{in}| \le \frac{V_o}{2}$$

$$i_{ripple} = (|v_{in}| - \frac{V_o}{2})(1 - \frac{|v_{in}|}{V_o}) \qquad \text{if} \qquad |v_{in}| > \frac{V_o}{2}$$

The inductor current also normalized with the same current as we did in Figure 3-12. Comparing with Figure 3-12, the inductor ripple current is 4 times smaller. Thus, we can use 4 times smaller inductor or reduce switching frequency to one fourth to achieve same amount current ripple, which will improve the converter efficiency.

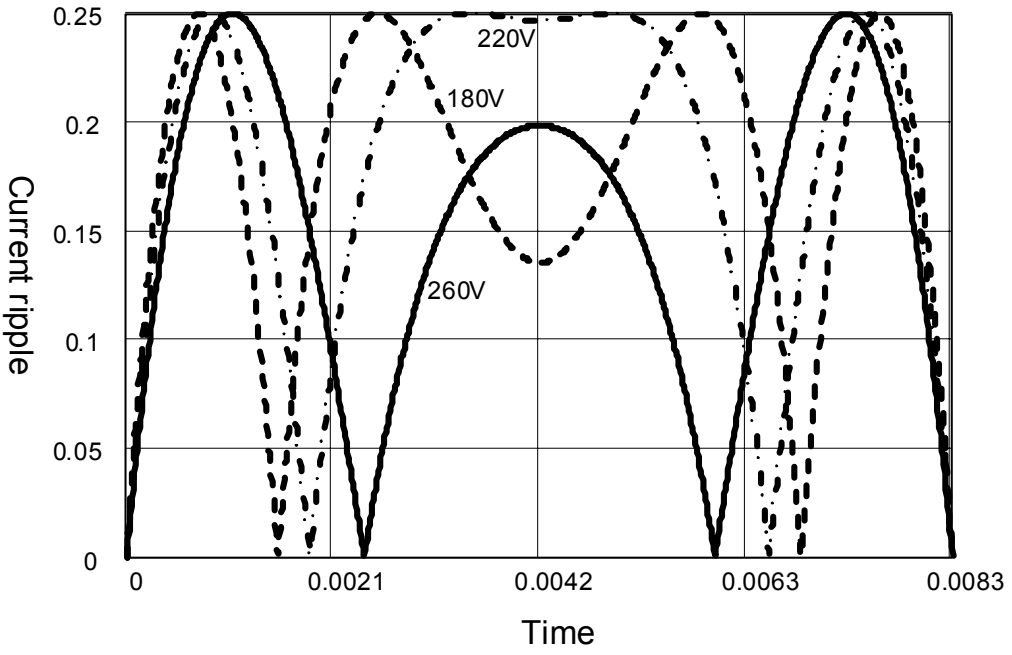
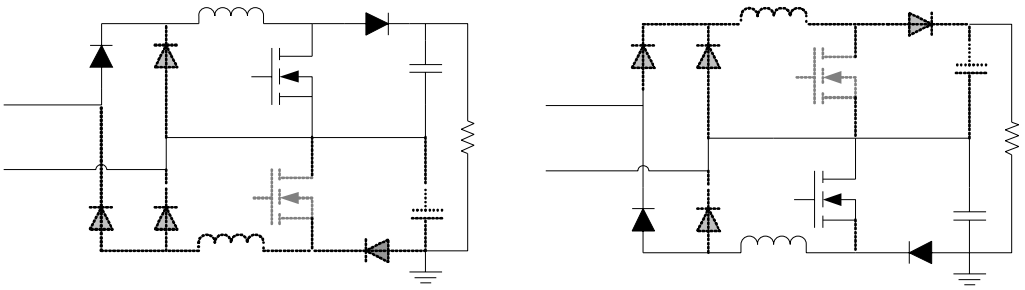


Figure 3-15. Inductor ripple current for three-level PFC with other control method.

B. Operation under low input line

By definition, low input line means the input line voltage RMS value is between 90V to 130V. For the three-level PFC with range switching, at low input line the range switch is turned on. Therefore, for each half line cycle, the circuit operates as a single switch PFC, as shown in Figure 3-16. Boost inductor is charged by the input voltage and discharged by half of the output voltage. Besides, comparing with conventional PFC, there is only one diode of input diode bridge is conducting. Thus, conduction loss on one diode is removed, which means the efficiency improvement.



(a) Positive half line cycle (b) Negative half line cycle

Figure 3-16. Equivalent circuit for three-level PFC with range switch at low input line.

Moreover, in the conduction path, there is only one 300V MOSFET or 300V fast recovery diode, and conduction loss can be further reduced comparing with high voltage rating devices. The different between the conventional PFC and three-level PFC under low line condition are summarized in Table 3-2.

Table 3-2. Three-level PFC at low input line with range switch on.

	Inductor voltage	
	Charging	Discharging
Conventional PFC	v_{in}	$V_o - v_{in}$
Three-level PFC	v_{in}	$\frac{V_o}{2} - v_{in}$

Thus, according to the volt-second balance on Boost inductor, we can derive

$$d = 1 - \frac{2|v_{in}|}{V_o}$$

Therefore, the Boost inductor ripple current can be calculated accordingly.

$$i_{ripple} = \frac{T_S}{L/2}|v_{in}|\left(1 - \frac{2|v_{in}|}{V_o}\right)$$

Considering three-level PFC splits the Boost inductor into two, each one has half of the original inductor. The inductor current ripple comparison is shown in Figure 3-17. Because three-level PFC reduces the volt-second applied to the Boost inductor, although three-level PFC operates with half of the Boost inductor, the ripple current only increase by 5%.

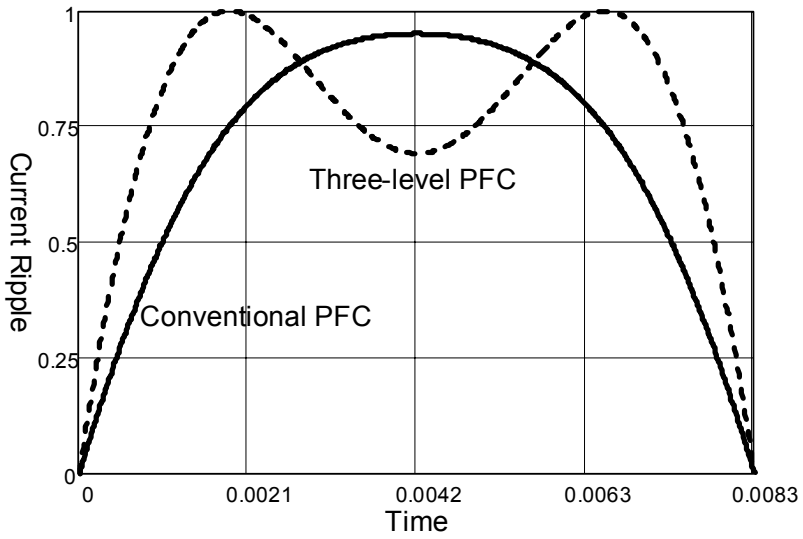


Figure 3-17. Comparison between conventional PFC and three=level PFC at 110V input.

Based on the operation mode analysis of the three-level converter at different input line conditions, the converter loss can be breakdown and compared with conventional PFC circuit. Because of the three-level structure, voltage stresses on the switching devices are only half of the output voltage. Thus, 300V rating high performance MOSFET and diode can be used. In the analysis, 300V MOSFET APT30M85BVR from Advanced Power was chosen as switching device, which has an on-state resistance as 85mΩ. Meanwhile, 300V fast recovery diode APT30D30B from Advanced Power was chosen as the rectifier. Converter loss breakdowns at different input line conditions are shown in Figure 3-18. Comparing with the loss breakdown of conventional PFC circuit, as shown in Figure 3-3, by using three-level PFC with range switch, converter conduction loss can be dramatically reduced, from both the diode-bridge and MOSFET. Further more, because of the low voltage rating devices and equivalent low output voltage, switching loss is reduced as well.

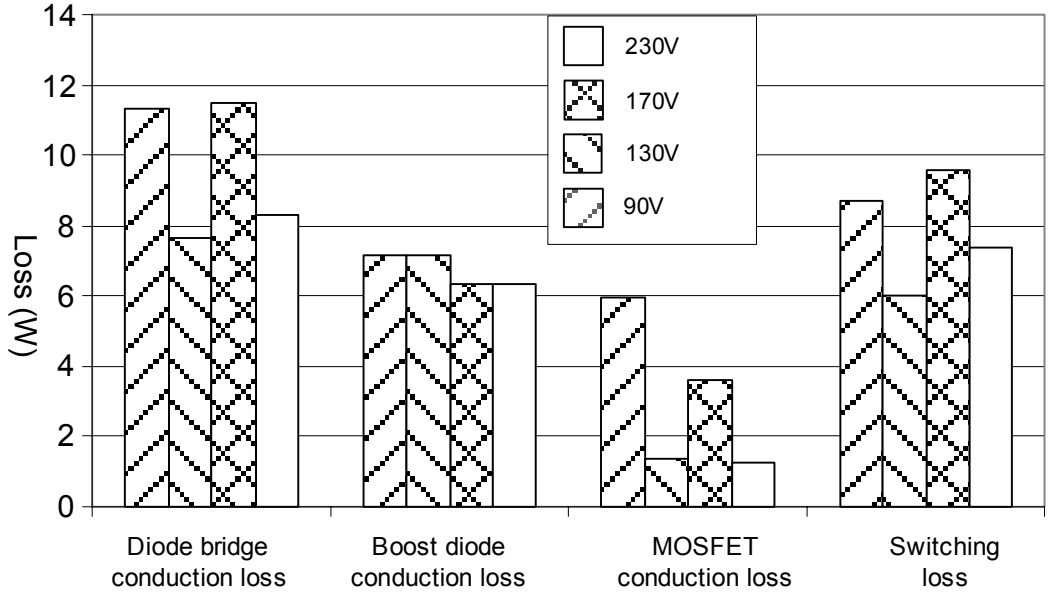


Figure 3-18. Loss Break down of three-level PFC.

C. Implementation of Three-Level PFC with Range Switch

To verify the benefits of three-level PFC, a 1kW 100 kHz PFC with range switching was built. The experimental waveforms are shown in Figure 3-19 and Figure 3-20

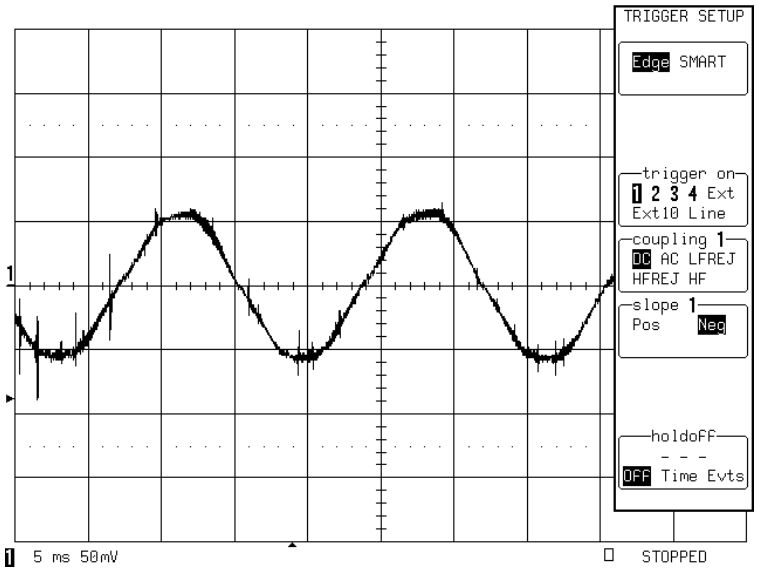


Figure 3-19. Input current for three-level PFC at 110V input (10A/div, 5mS/div).

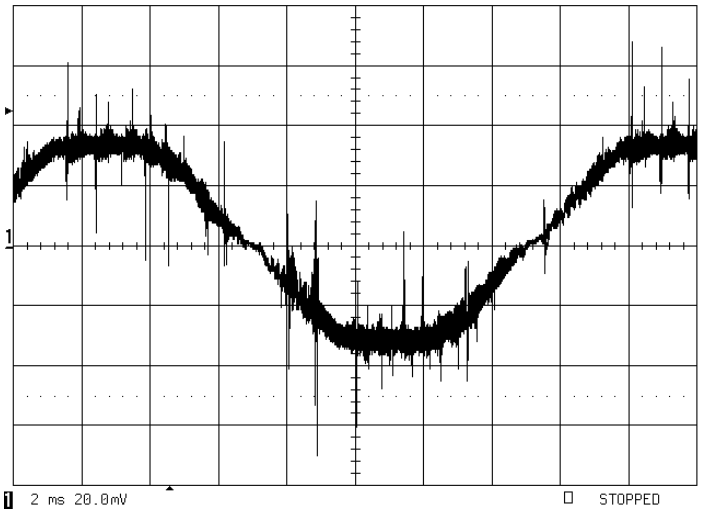


Figure 3-20. Input current for three-level PFC at high input line (4A/div, 2mS/div).

The efficiency of three-level PFC at different line voltages is shown in Figure 3-21. At low input line, due to the reduction of conduction loss and switching loss, the efficiency is much high comparing with conventional PFC and it can reach 94.5% at 90V input.

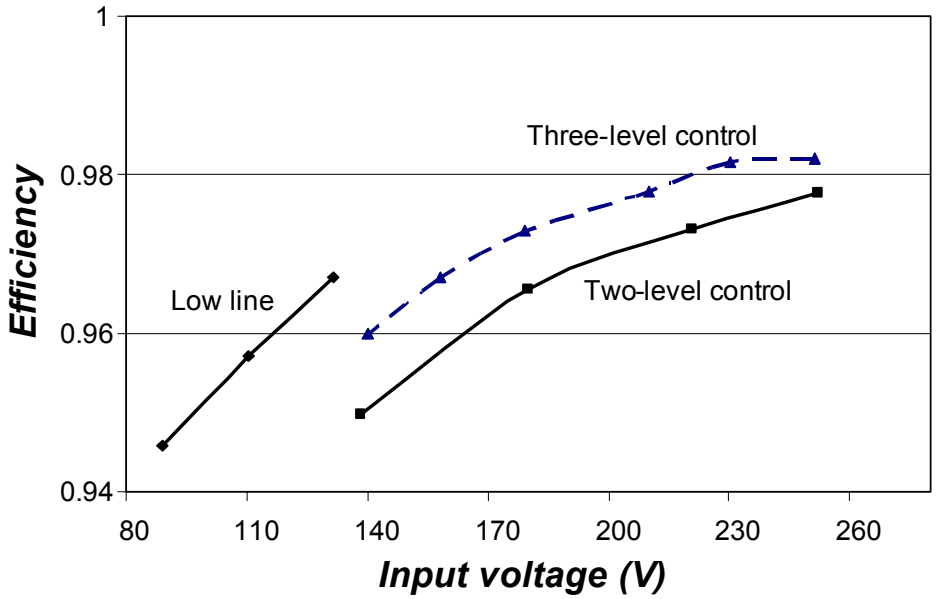


Figure 3-21. Efficiency for three-level PFC with range switch.

3.3.2 Dual Boost PFC (Bridgeless PFC)

Comparing with conventional PFC circuit, three-level PFC can dramatically improve the efficiency, especially under low input line condition. However, due to the complex control method ad implementation of range switch, it hasn't been adopted for industry implementations [C-19][C-20]. Instead of using three-level PFC, bridgeless PFC is able to improve the converter efficiency without complex control method, which makes it attractive for industries [C-21][C-22].

Without input diode bridge, bridgeless PFC generates less conduction loss comparing with conventional PFC. Bridgeless PFC circuit diagram is shown in Figure 3-22. PFC inductor is split into two and located at AC side to construct the Boost structure. Equivalent circuit of positive half line cycle is show in Figure 3-23. In the positive half line cycle, MOSFET S1 and Boost diode D1, together with the PFC inductor construct a Boost DC/DC converter. Meanwhile, MOSFET S2 is conducting through its body diode and it operates as a simple diode. Therefore, turning on or off S2 will not change the circuit operation mode. Therefore, both of the MOSFETs can be driven by the same signal. The input current is then controlled by the duty cycle of MOSFET S1 and following the input voltage shape to achieve power factor correction. During the negative half line cycle, circuit operates as the same way. But the Boost converter switch changes into S2 and S1 works as a diode. Thus, in each half line cycle, one of the MOSFET operates as active switch and the other one operates as a simple diode.

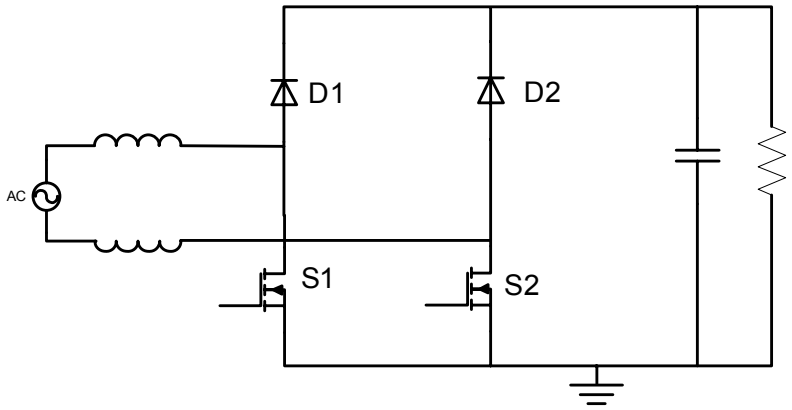


Figure 3-22. Bridgeless PFC circuit.

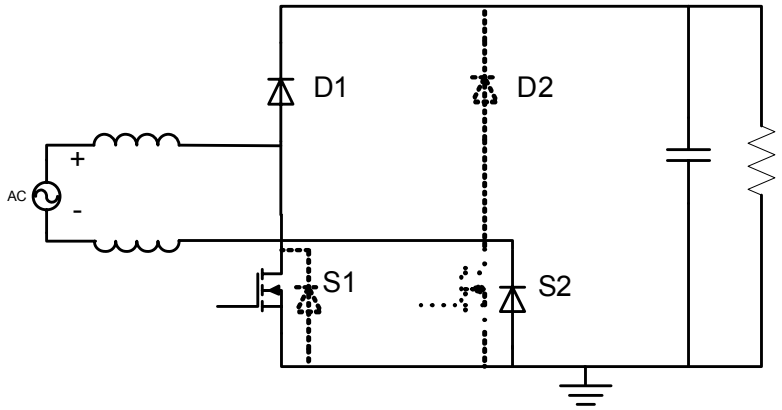


Figure 3-23. Equivalent circuit of bridgeless PFC.

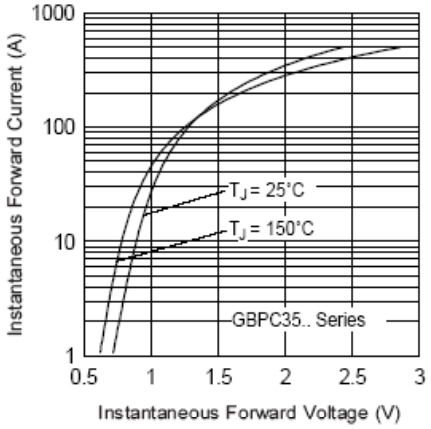
The difference between bridgeless PFC and conventional PFC is summarized in Table 3-3. Comparing the conduction paths of these two circuits, at every time instance, bridgeless PFC inductor current only goes through two semiconductor devices, but inductor current goes through three semiconductor devices for the conventional PFC circuit. Therefore, conduction loss is much reduced in bridgeless PFC. Furthermore, comparing with conventional PFC, bridgeless PFC also reduces the total components count.

Since both the circuits operating as Boost DC/DC converters, switching performance of two circuits keep the same, which results in similar switching loss. As shown in Table 3-3, the bridgeless PFC uses one MOSFET body diode to replace the two slow diodes of the conventional PFC. Thus, efficiency improvement by using bridgeless PFC relies on the conduction loss difference between the two slow diodes and the body diode of one MOSFET.

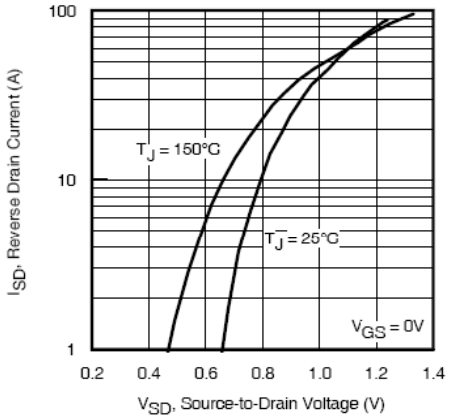
Table 3-3. Differences between conventional PFC and bridgeless PFC.

	Slow diode	Fast Diode	MOSFET	Conduction Path On/(Off)
Conventional PFC	4	1	1	2 slow diode, 1MOSFET/ (2 slow diode, 1 fast diode)
Bridgeless PFC	0	2	2	1 body diode, 1 MOSFET/ (1 MOSFET body diode, 1diode)

To estimate the efficiency improvement by using bridgeless PFC circuit, loss comparison is performed based on theoretical analysis. The switch of choice is a super junction MOSFET rated at 22A, 600V from International Rectifier and the diode bridge is chosen as GBPC2506W, rated at 25A, 600V, which is also from International Rectifier. The forward voltage drops of Diode Bridge and MOSFET body diode are shown in Figure 3-24.



(a) Forward voltage drop of GBPC2506W



(b) Forward voltage drop of MOSFET

Figure 3-24. Forward voltage drop comparison.

Curve fitting method is used to generate the conduction loss model of these devices. Based on the inductor current instantaneous value, conduction losses generated by two Diode Bridge diodes and one MOSFET body diode at 90V input are calculated for different output power levels, as shown in Figure 3-25.

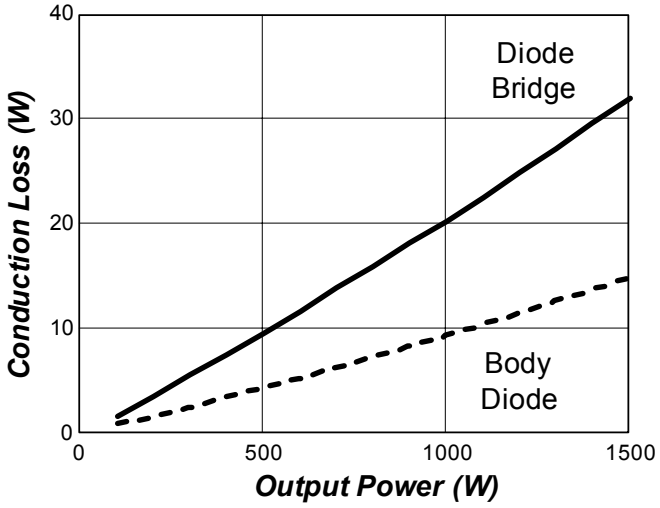


Figure 3-25. Diode conduction loss comparison.

The loss reduction is getting large when the output power level is increased. However, for all the power level range, the ratio between the loss reduction and the output power is almost constant. Thus, bridgeless PFC can improve the total

efficiency at different power levels by around 1%, at 90V AC input. When the input voltage increases, the loss reduction gets less. As shown in Figure 3-26, the loss reduction is maximized when input voltage is 90V. Because diode forward voltage drop is almost constant for all the load conditions, its effect becomes more pronounced when input voltage is lower.

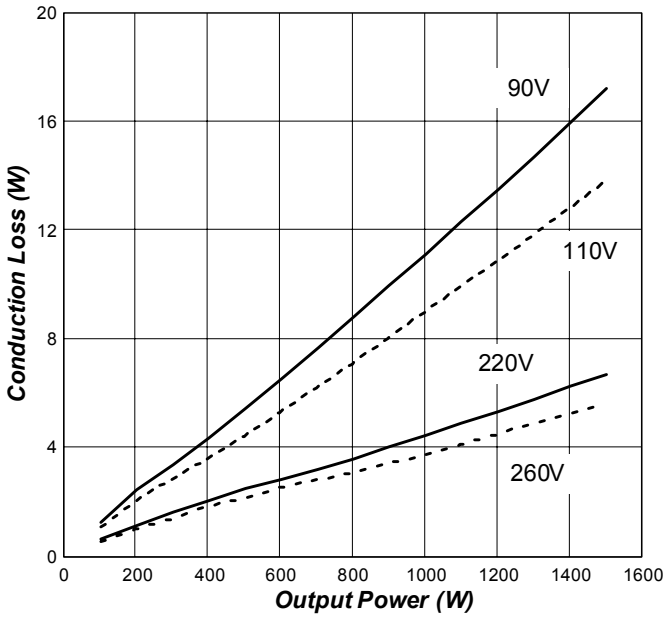


Figure 3-26. Power loss improvement at different input voltages.

Besides loss reduction by removing one diode, considering small MOSFET on state resistance, turning on the MOSFET might further reduce conduction loss by using synchronous rectifier. Based on the current conduction mechanism of MOSFET, current automatically chooses between MOSFET channel and body diode channel according to the lower voltage drop. Therefore, single MOSFET conduction loss can be estimated with or without synchronous rectified turned on. The calculation results are shown in Figure 3-27.

The power losses of these two cases are very similar. Although the synchronous rectifier has slight loss reduction at low power level, the different is neglectable. Considering the complexity of synchronous rectifier control, it shouldn't be implemented using today's device.

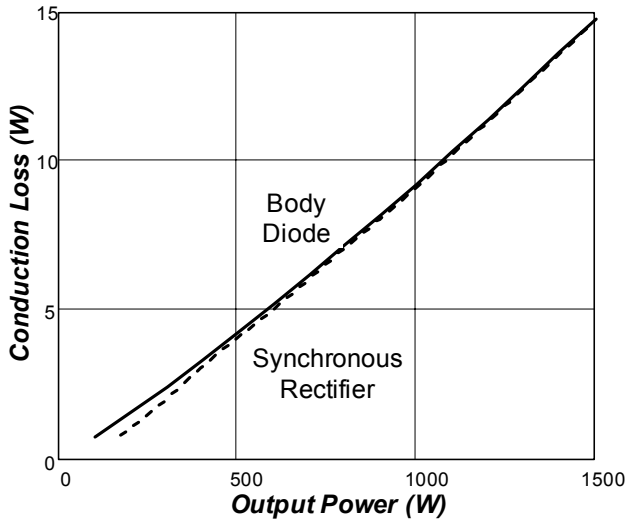


Figure 3-27. MOSFET loss comparison between the body diode and synchronous rectifier at 25°C.

So far, according to the loss analysis, the capability of conduction loss reduction of using bridgeless PFC has been demonstrated. However, without input Diode Bridge, Boost inductor located on the AC side, there is no direct connection between circuit output and input. Thus, bridgeless circuit has several issues, including input voltage sensing, inductor current sensing and large common mode EMI noise.

The voltage sensing and current sensing issues are related to the control of bridgeless PFC circuit. For the conventional PFC circuit, different control

methods have been developed, such as the average current mode control, peak current mode control, and one cycle control.

The average current mode control is the most popular control method because of its high performance and easy to understand: the controller multiplies input voltage signal with the voltage loop output voltage, and divided by the square of input voltage feed forward signal, to generate the current reference, while the current loop controls the inductor average current to follow the current reference. The control diagram is shown in Figure 3-28.

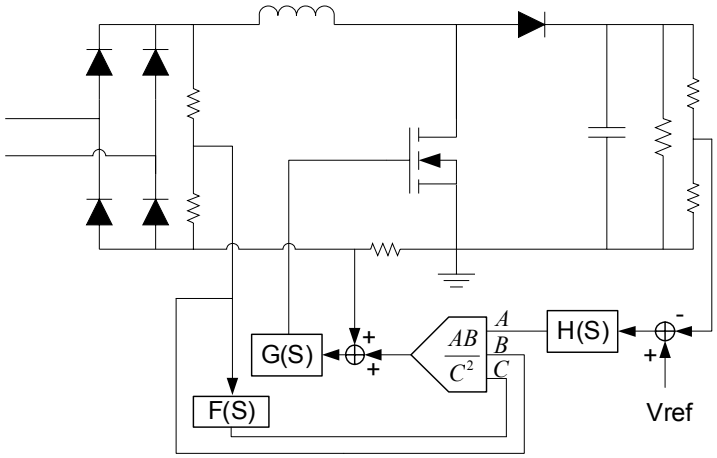
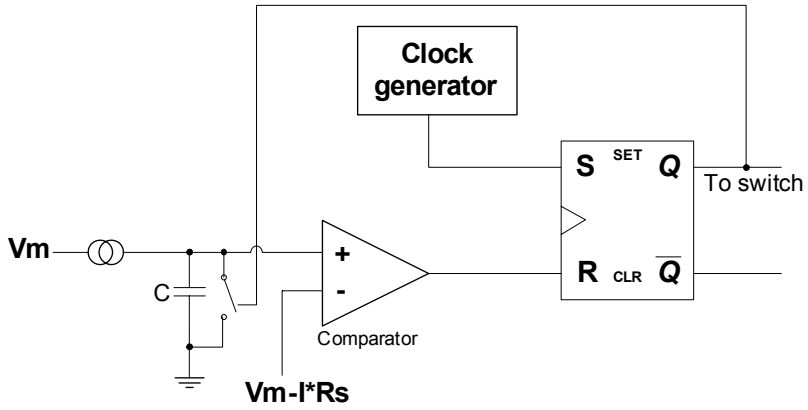


Figure 3-28. Average current control for PFC circuit.

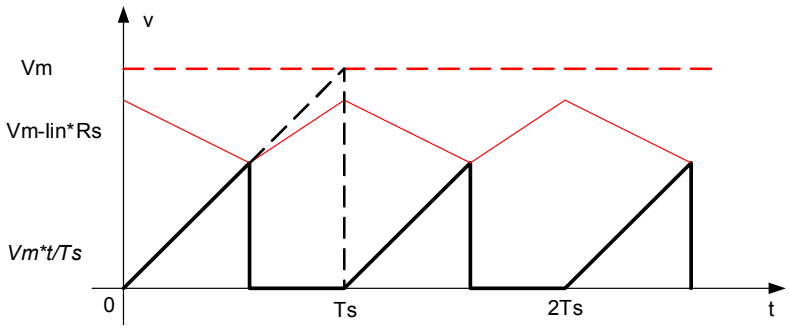
As for the One Cycle Control, the controller uses the voltage loop output voltage and inductor peak current to calculate the duty cycle of each switching cycle [C-23][C-24][C-25]. Control block and key control waveforms are shown in Figure 3-29. Here Vm is the voltage loop compensator output, which is the same as average current mode control. Because of the low bandwidth of voltage loop, this voltage can be considered as DC voltage. This voltage is then

transferred into a current source and charges the capacitor C. In each switching cycle, capacitor C is charged from zero to Vm and then reset to zero at the end of the cycle. The capacitor voltage is then compared with $V_m - I * R_S$ signal. Here R_S is the current sensing gain. From the control waveforms, it can be observed that, at current peak value

$$V_m D = V_m - I \cdot R_S$$



(a) Control diagram



(b) Key waveforems

Figure 3-29. One cycle control.

From this equation, we can derive

$$I \cdot R_S = V_m (1 - D)$$

According to the relationship between input and output voltage of PFC circuit, the duty cycle should meet the equation

$$V_{in} = V_o(1-D)$$

Because V_o is a DC voltage and V_{in} is a sinusoidal voltage, $V_m(1-D)$ in turn should be a sinusoidal voltage. Thus, the inductor peak current follows the sinusoidal shape and in phase with input voltage, which means the power factor correction function can be achieved. From the principles of one cycle control, it doesn't require input voltage sensing. Furthermore, it is a peak current mode control. Thus, switch current can be used.

By using one cycle control, the duty cycle meets the requirement of the Boost circuit input and output voltage relationship, the inductor current peak current automatically follows the input voltage shape. Thus, the power factor correction function can be achieved. From the principles of one cycle control, it doesn't require input voltage sensing. Furthermore, it is a peak current mode control. Thus, switch current can be used.

A. Input voltage sensing

For conventional PFC, input voltage sensing is simple. Because of the existence of the rectifier bridge, the rectified input voltage can be directly sensed by using the voltage divider, as shown in Figure 3-30.

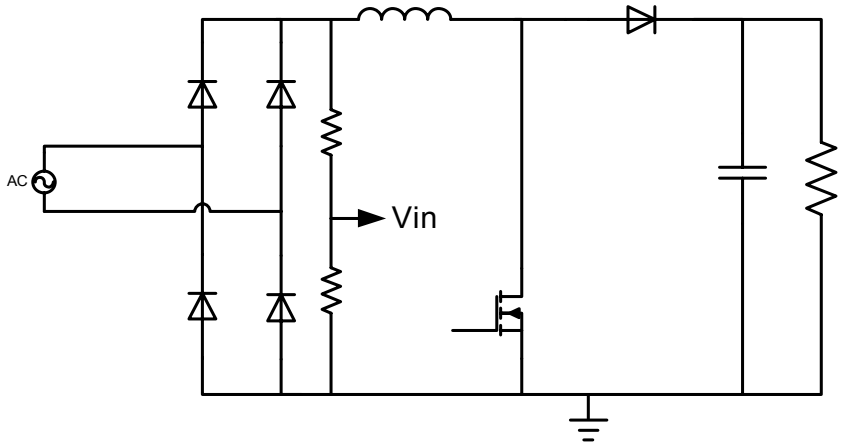
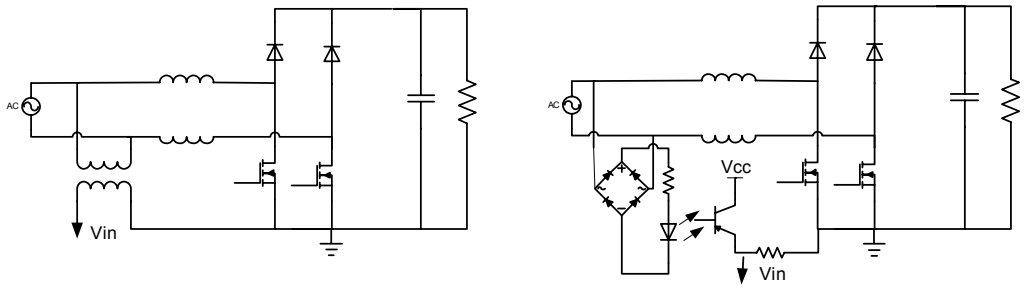


Figure 3-30. Input voltage sensing for conventional PFC.

For the bridgeless PFC, there is no rectifier bridge and no place to use the voltage divider to sense the input voltage. A line frequency transformer is a simple solution for the voltage sensing, as shown in Figure 3-31 (a). Due to the larger size of low frequency transformer and the cost issue, it is generally unacceptable for an efficient design. The optical coupler is also a good candidate for voltage sensing, because it can easily achieve isolation, as shown in Figure 3-31 (b). To achieve lower distortion of the voltage sensing, higher linearity optical coupler with wide operating range needs to be used, which is not practical and much more complex comparing with the conventional voltage divider sensing.



(a) Line frequency transformer (b) Optical coupler

Figure 3-31. Voltage sensing for bridgeless PFC.

For the average current mode control, the inductor current reference is generated based on the sensed input voltage: the input voltage sensing is necessary and will cause higher cost or larger converter size. When One Cycle Control is used, all the necessary information is generated from peak inductor current and the voltage loop output, which makes input voltage sensing unnecessary. For the conventional PFC circuit, the voltage sensing is simple, which makes the benefit of using One Cycle control less obvious. The complex input voltage sensing of bridgeless PFC makes the One Cycle control a more attractive control method.

B. Current sensing

For conventional PFC, inductor current sensing is quite simple, too. Simply putting a shunt resistor at the return path of inductor current, inductor current can be sensed and with the common ground of the control, as shown in Figure 3-32. There is no isolation requirement for the current sensing.

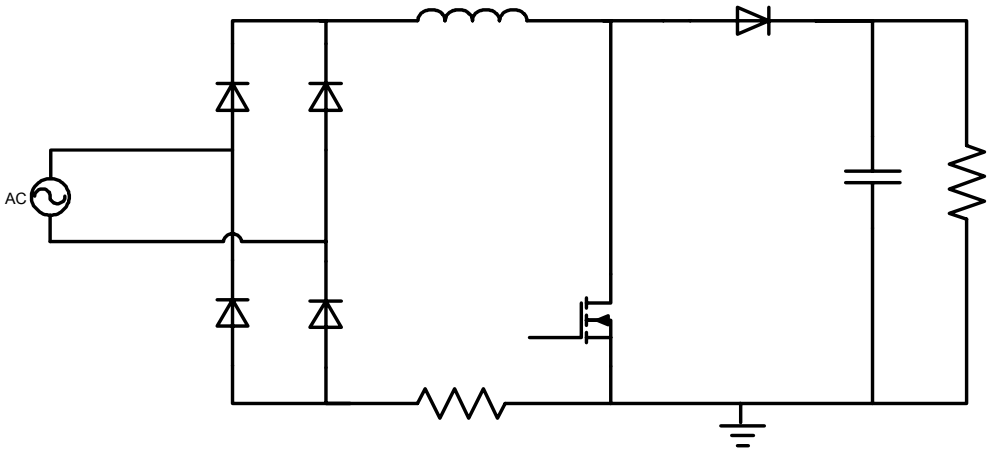
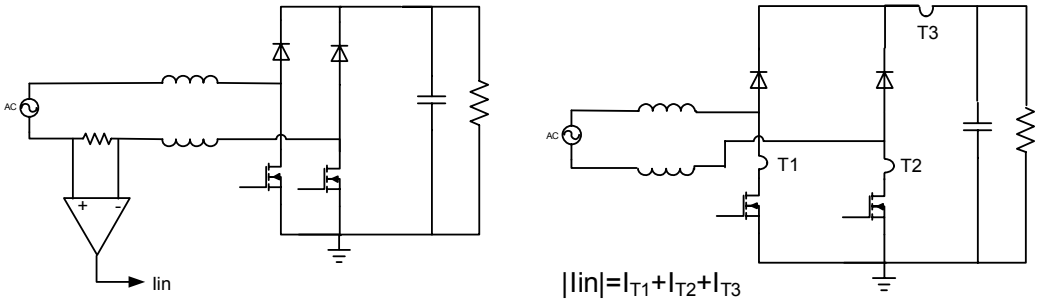


Figure 3-32. Current sensing for conventional PFC.

For bridgeless PFC, inductor return path doesn't share the same ground as the output. Therefore an isolated sensing method has to be used. Same as voltage sensing, a 60Hz current transformer will give a straightforward solution. In general a low frequency transformer will introduce a non negligible phase delay on the current signal, causing a degradation of the power factor.

Another isolation method is to use the differential mode amplifier, as shown in Figure 3-33 (a). Because the PFC circuit switches at high switching frequency and high output voltage, the high common mode voltage will cause extra noise in sensed current signal. Since the current sensing voltage is desired to be low to minimize the power loss, power factor may be hurt because of the current sensing noise. Besides, the differential amplifier cost is much higher comparing with the shunt resistor solution.

Alternatively, the inductor current can be reconstructed by the switch and diode current. Due to the different conduction path of the inductor current a total of three current transformers are required for the current sensing. Figure 3-33 (b) shows the position of the required current transformers. The input current I_{IN} can be reconstructed as the sum of the three sensed currents.



(a) Differential mode amplifier (b) Current transformer

Figure 3-33. Current sensing for bridgeless PFC.

For average current mode control, inductor average current is required for the current loop. Therefore, the current sensing needs to sense the inductor current. But for One Cycle Control only the inductor peak current is required for the control. Therefore, the current sensing can be simplified. By using two current transformers in series with the switches, the inductor peak current can be easily sensed through switch current. At the same time the use of current transformer can further reduce the power loss caused by shunt resistor.

Same as the voltage sensing, the simple current method for the conventional PFC circuit makes the One Cycle Control less attractive. For bridgeless PFC, the complexity of current sensing makes One Cycle Control the most attractive control method.

C. Common Mode EMI Noise

EMI noise issues rely on the power stage structure [C-26][C-27][C-28]. For conventional PFC, the output voltage ground is always connected with the input line, through the rectifier bridge. Therefore, the only parasitic capacitor

contributes to the common mode noise is the parasitic capacitance between the MOSFET drain to the earth ground, as shown in Figure 3-34.

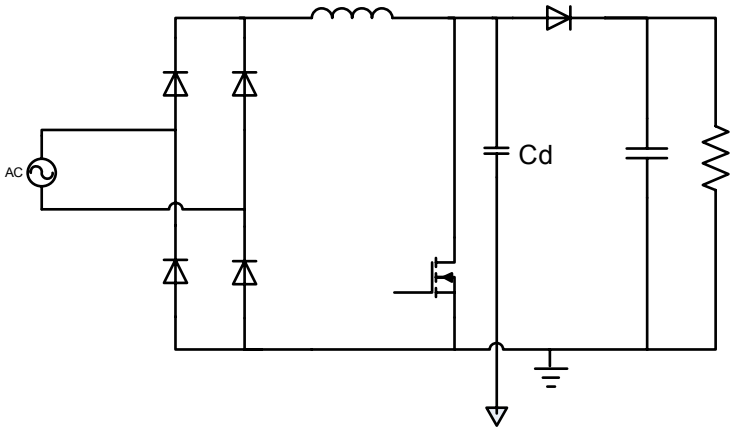


Figure 3-34. Parasitic capacitor contributes to common mode noise for conventional PFC.

For the bridgeless PFC the output voltage is always floating in regard of the input AC line. Thus, not only the parasitic capacitance between the MOSFET drains to the earth ground Cd1 and Cd2, but also all the parasitic capacitances between the output terminals to the earth ground Cn and Cp contribute to the common mode noise, as shown in Figure 3-35. The simulation results are shown in Figure 3-36. All the voltages across parasitic capacitors are fluctuating, which means large common mode current will be generated and cause large common mode noise.

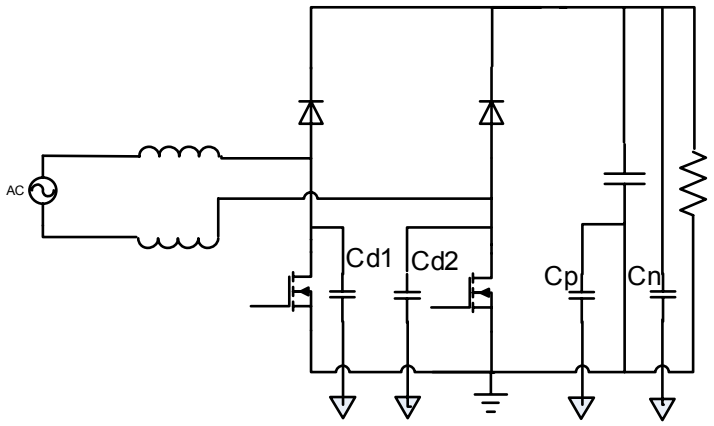


Figure 3-35. Parasitic capacitances contribute to common mode noise for bridgeless PFC.

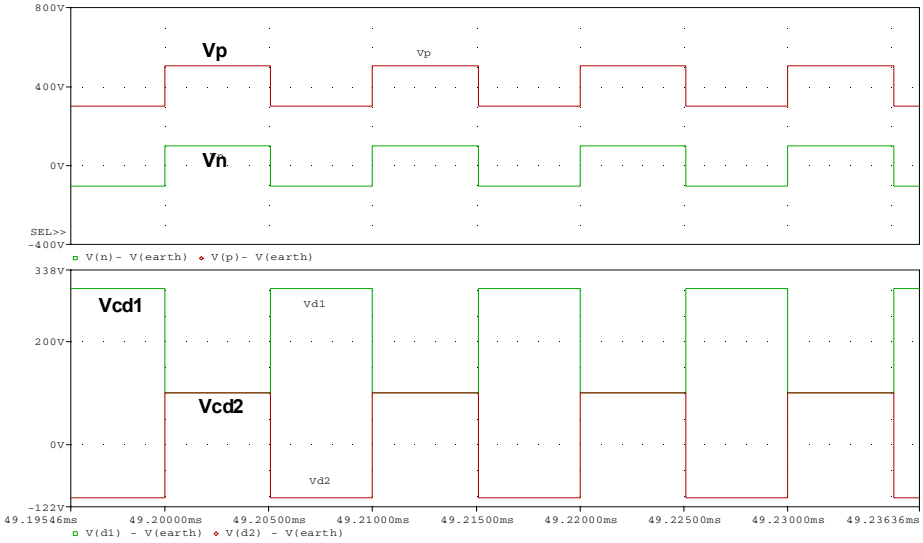


Figure 3-36. Voltage on the parasitic capacitor of bridgeless PFC.

dv/dt on the parasitic capacitors between the MOSFET drains to the earth ground Vcd1 and Vcd2 are reverse polarity. By carefully designing the parasitic capacitances, noise cancellation can be achieved.

As the dv/dt of the parasitic capacitances between the output terminals to the earth ground, Vp and Vn, are the same polarities, there is no way to achieve noise cancellation.

Considering these capacitors not only include the output of the PFC stage parasitics but also the input terminals of loads, the common mode noise can be much worse comparing with the conventional PFC circuit. As shown in Figure 3-37, measured EMI noise for bridgeless PFC is way higher than the EMI standard requirement, even with EMI filter.

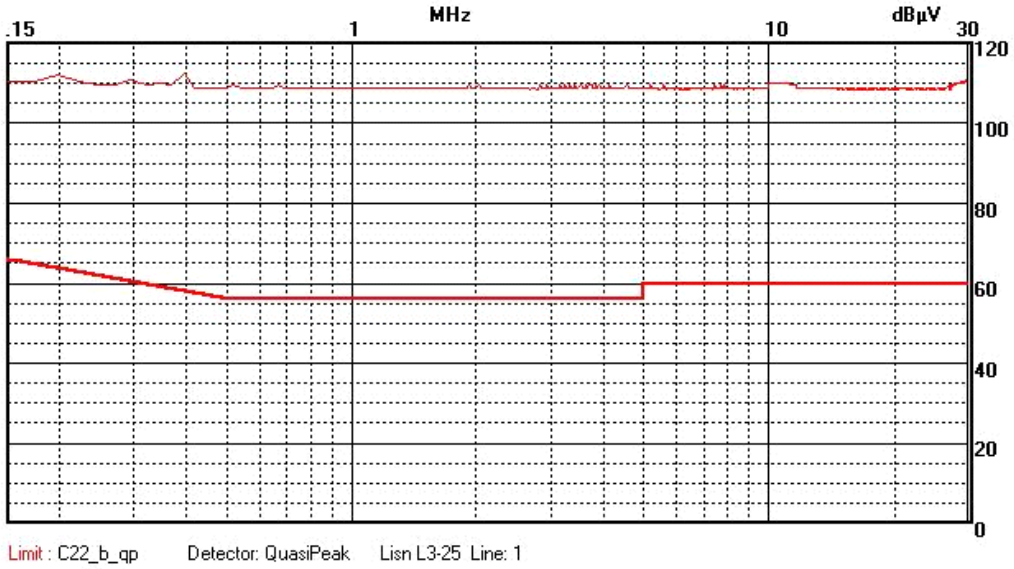


Figure 3-37. EMI noise for bridgeless PFC without EMI reduction circuit.

To solve the EMI noise issue, a new EMI noise reduction circuit for the bridgeless PFC circuit is introduced. The circuit schematic is shown in Figure 3-38. Comparing with original bridgeless PFC circuit, the proposed circuit adds two capacitors to create a high frequency path between output voltage to input AC line. In this way, the output voltage no longer fluctuates respecting to input line. Therefore, CM noise again is determined by the parasitic capacitor between MOSFET drain and the earth ground. Thus, the EMI performance of bridgeless

PFC with proposed EMI noise reduction circuit can achieve similar performance comparing with conventional PFC circuit.

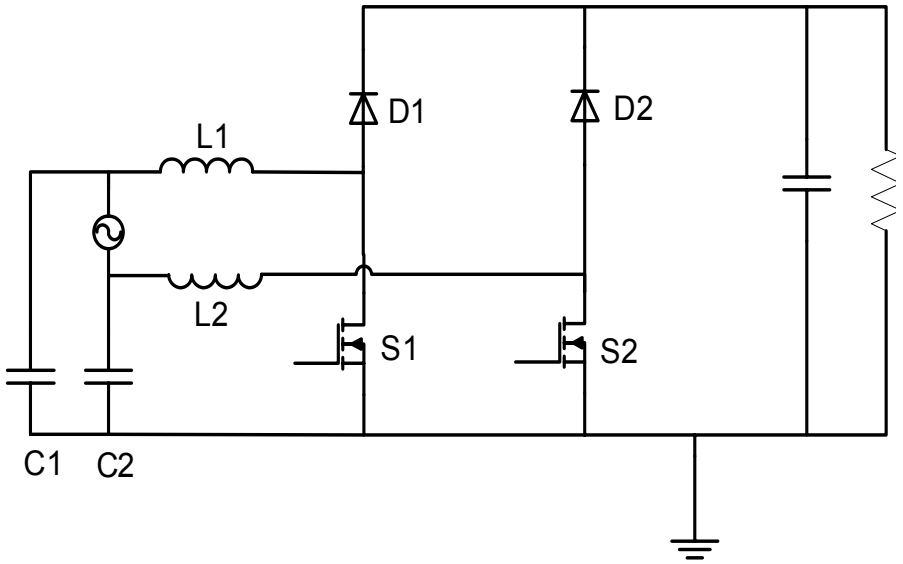


Figure 3-38. An improved EMI performance bridgeless PFC circuit.

D. Experimental verification

Based on the analysis above, the bridgeless PFC circuit can both simplify the circuit topology and improve the efficiency, while the One Cycle Control is the most attractive control method for the bridgeless PFC circuit.

One 500W, 100 kHz switching frequency, universal line input bridgeless PFC circuit is designed and implemented with One Cycle Control, using IR1150S controller. Super Junction MOSFET 600V 22A and 600V 4A SiC diode, both from International Rectifier, are used in the prototype. Besides, the conventional PFC circuit using same devices and conventional average current mode control was built to serve as the benchmark.

The input voltage and current waveforms are shown in Figure 3-39. The input current perfectly follows the input voltage. Thus the power factor correction function is achieved by using one cycle controller. The efficiency comparison between these two circuits at 90V input line is shown in Figure 3-40. For the whole power range, efficiency improvement is around 1%, which is quite coincident with the theoretical analysis.

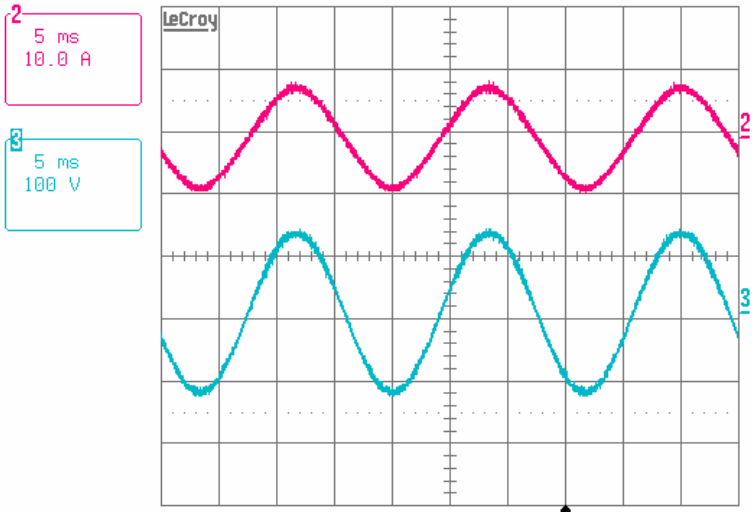


Figure 3-39. Input voltage and current waveforms of the bridgeless PFC.

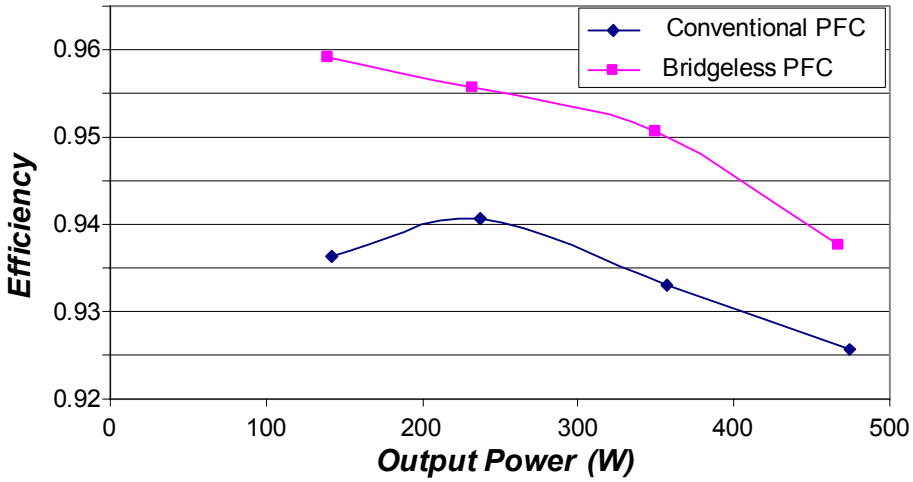


Figure 3-40. Efficiency comparison between conventional PFC and bridgeless PFC.

The power factor at full output power and different input line is shown in Figure 3-41. Comparing with average current mode control, high power factor can also be achieved by using the One Cycle Control for the whole input line range.

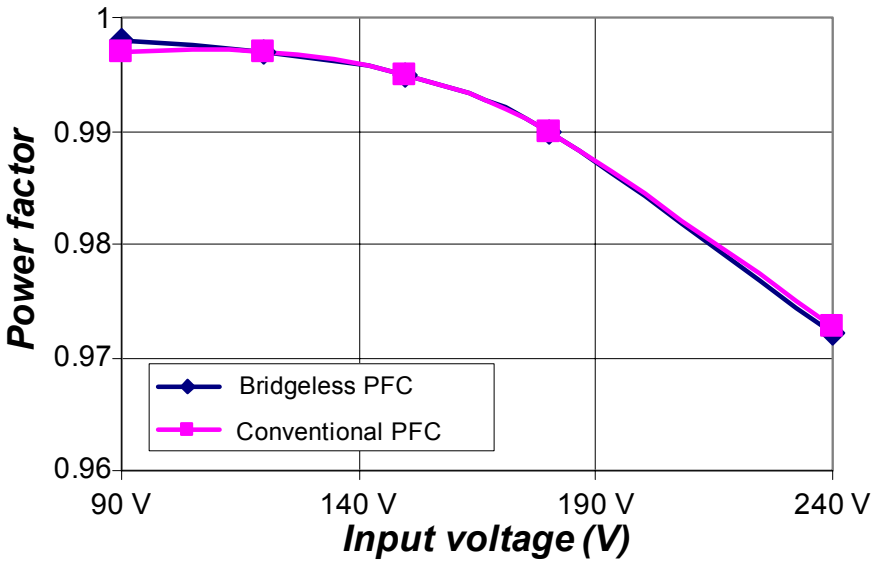


Figure 3-41. PF comparison at different input line.

EMI performances of the bridgeless PFC and the conventional PFC circuit are compared, and the results are shown in Figure 3-42 though Figure 3-44. From the experimental results, EMI noise of bridgeless PFC with the proposed EMI noise reduction circuit is similar to the conventional PFC circuit noise at low frequency range. Although the noise is slightly higher at the high frequency range, the EMI noise of the bridgeless PFC circuit is controllable.

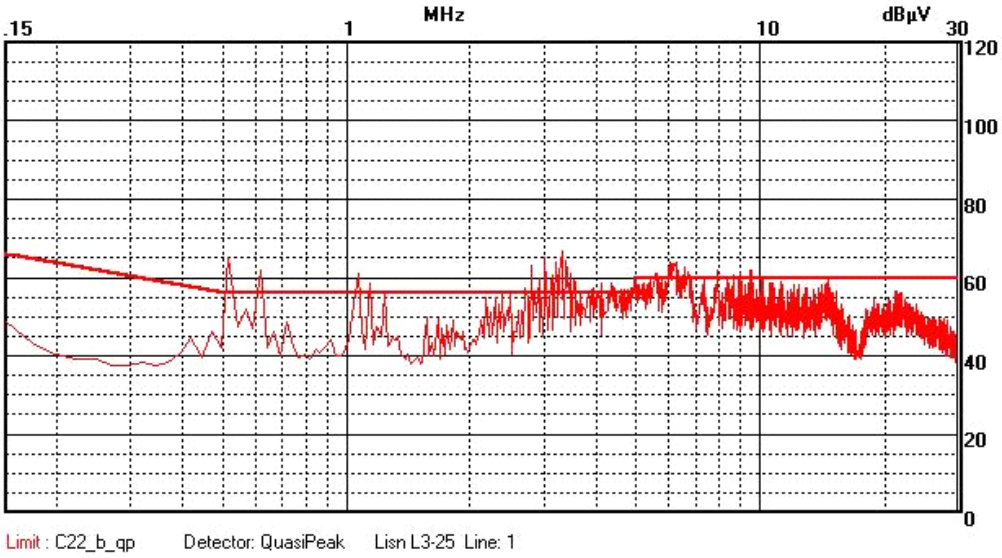


Figure 3-42. EMI noise of the conventional PFC.

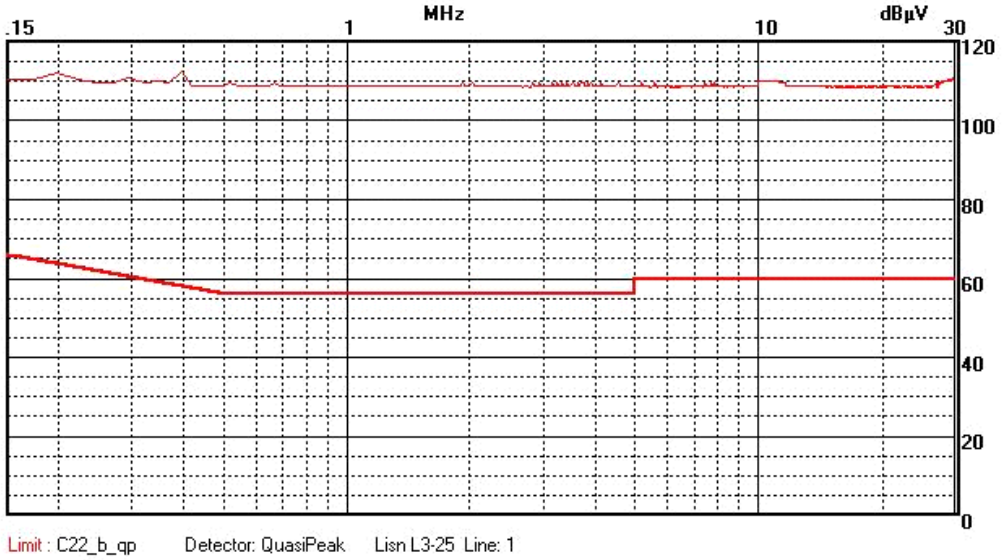


Figure 3-43. EMI noise for bridgeless PFC without EMI reduction circuit.

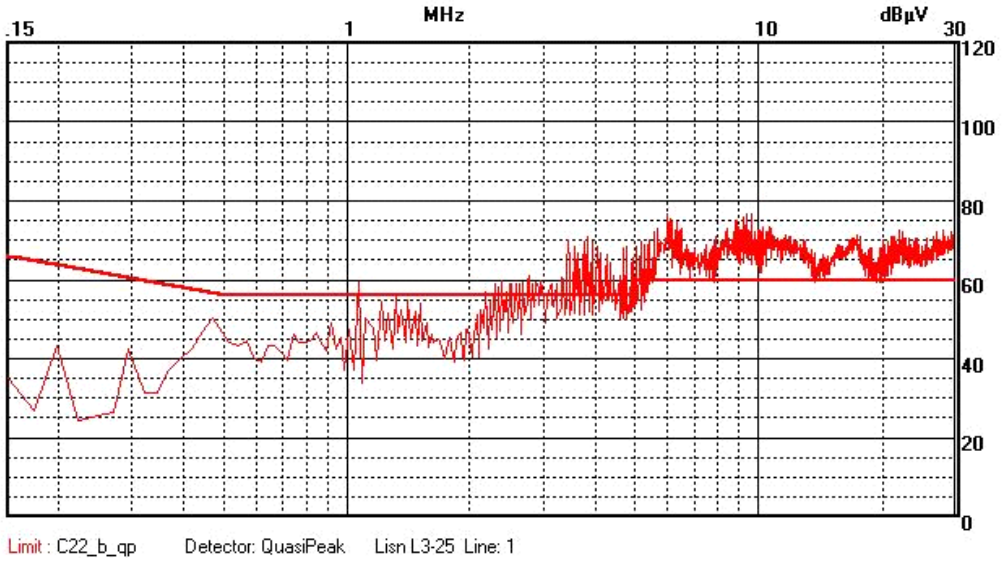


Figure 3-44. EMI noise of bridgeless PFC with noise reduction circuit.

3.4 Summary

In this chapter, different techniques for achieving high switching frequency PFC have been investigated.

As demonstrated in chapter 2, by pushing PFC switching frequency higher than 400 KHz, Boost inductor and EMI filter sizes keep decreasing. Therefore, PFC circuit is desirable to operate at switching higher than 400 kHz to achieve high power density.

For conventional PFC circuit using conventional devices, high switching loss and conduction loss exist. Thus, the circuit is not able to operate with high switching frequency. The newly developed CoolMOS^{TM} and SiC Schottky diode dramatically improve the switching performance and totally remove reverse recovery current. By using these devices, conventional PFC efficiency can be

improved to around 93% at 90V input. Furthermore, these devices enable the circuit operate at 400 kHz switching frequency and maintain 95% efficiency at 150V input.

By modifying PFC circuit topology, further efficiency improvement can be achieved. Three-level converter allows PFC circuit using 300V rating devices, together with three-level control, efficiency can be pushed up to 96% at 150V input by using conventional devices. Furthermore, by using the range switch, both the diode bridge and MOSFET conduction loss can be largely reduces, which results in 94.5% efficiency at 90V input.

Bridgeless PFC circuit removes the input diode bridge and reduces conduction loss. The bridgeless PFC topology removes the input rectifier conduction losses and is able to achieve higher efficiency. Based on the theoretical analysis, 1% efficiency improvement is expected from the circuit at 90V input. The efficiency improvement comes at the cost of increased complexity for input voltage and current sensing. At the same time additional EMI issues are present.

The One Cycle Control does not require input line sensing and can operate in peak current mode, providing a simple and high performance solution and overcoming the limitation of bridgeless topology with conventional control. The EMI issues can be also overcome by using a modified version of the bridgeless topology.

The experimental results show the simplicity of the One Cycle Control and high power factor, meanwhile, verify that the bridgeless PFC can improve 1% efficiency comparing with the conventional PFC circuit, at 90V AC input.

Although the bridgeless PFC circuit exhibits slightly higher EMI levels, the noise is controllable and similar to the conventional PFC circuit EMI.

By using different techniques, PFC efficiency can be largely improved, which allows the PFC circuit operate at high switching frequency and achieve high power density. However, due to holdup time require, large bus capacitor is used in PFC circuit to provide the energy during holdup time, which becomes the bottleneck for further power density improvement. In chapter 4, this issue is further addressed.

Chapter 4. High Frequency LLC Resonant Converter

4.1 Introduction

With the development of power conversion technology, power density becomes the major challenge for front-end AC/DC converters. Although increasing switching frequency can dramatically reduce the passive component size, its effectiveness is limited by the converter efficiency and thermal management. In present industry implementations, due to the low efficiency PWM type topologies, DC/DC stage switching frequency is limited to 100 kHz range. Therefore, passive components take large portion of converter volume. As shown in Figure 4-1, DC/DC stage transformer and inductor take more than 30% for total converter space.

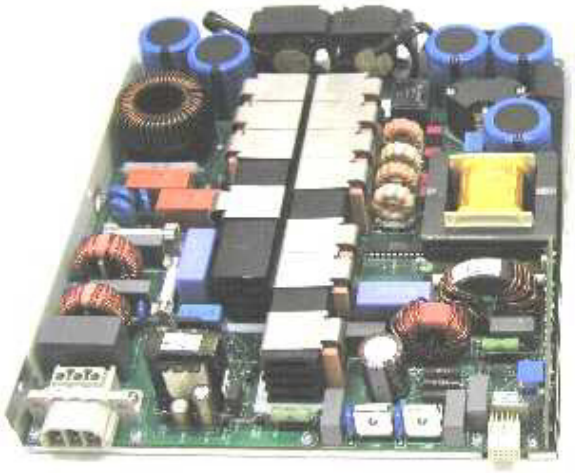


Figure 4-1. 1200W front-end AC/DC converter.

Beside large passive component size, bulky holdup time capacitor becomes the bottleneck for further power density improvement. As shown in Figure 4-1, to

meet the holdup time requirement, bulky capacitors have to be used to provide the energy during the holdup time. For the 12000W design five 200uF electrolytic capacitors are used.

Holdup time requirement can be explained in Figure 4-2. When the input line exists, PFC stages converters the input AC line into a regulated DC voltage and DC/DC stages changes it into the required output voltage, such as 48V or 12V. Once input line is lost, it is required the converter to keep the regulated output voltage for more than 20mS. During the holdup time, PFC output voltage keeps decreasing and DC/DC keeps regulating the output voltage, until the minimum input voltage the DC/DC converter is reached. After that, DC/DC stage shuts down and output voltage begins to drop.

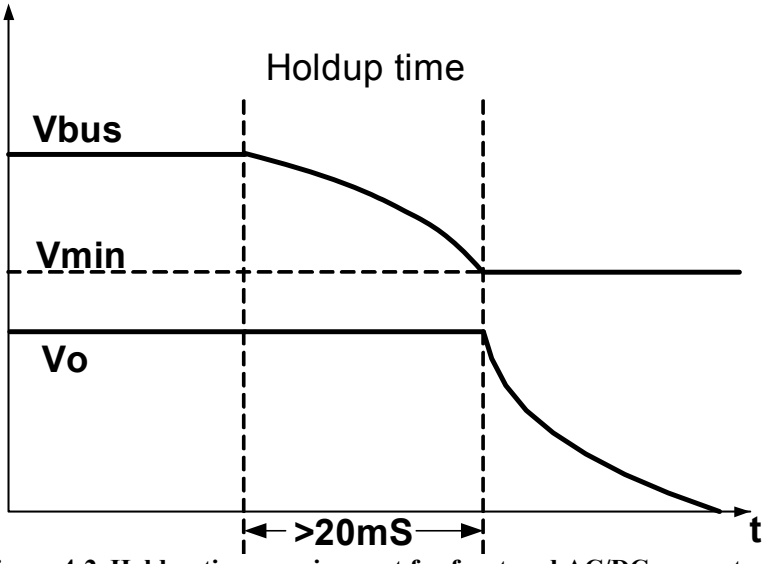


Figure 4-2. Holdup time requirement for front-end AC/DC converters.

Due to the loss of input line, energy transferred to load comes from PFC stage output capacitor, which is also known as holdup time capacitor. During holdup

time, the energy that transferred to the load, as well as dissipated in the DC/DC power conversion stage, is

$$E = \frac{1}{2} C\left(V_{bus}{}^2 - V_{\min}{}^2\right)$$

For PFC stage, the output voltage is always set to 400V to ensure its capability of operates at highest input line. Therefore, to provide the required energy during holdup time, both large C with large $V_{\min}$ and small C with small $V_{\min}$ can meet the requirement. The relationship between the holdup time capacitor requirement and the minimum DC/DC stage input voltage for front-end AC/DC converter at different power levels is illustrated in Figure 4-3. It can be seen that the holdup time capacitor requirement decreases with reducing DC/DC minimum input voltage. Therefore, wide input range DC/DC converter is desired for the front-end AC/DC converters.

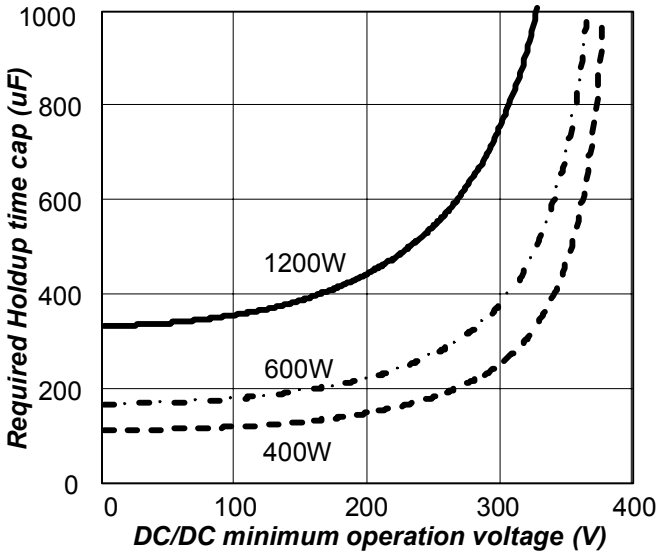


Figure 4-3. Holdup time capacitor vs. minimum DC/DC stage input voltage.

For conventional PWM converters, it is difficult to achieve both high efficiency and wide operation range simultaneously [D-1]. For instance, the asymmetrical half bridge converter, circuit is desired to operate with 50% duty cycle and achieve maximum efficiency [D-2]. However, to ensure wide operation range, during normal operation, duty cycle has to be reduced to realize regulation capability. Thus, circuit normal operation condition has to be compromised to achieve wide operation range. As demonstrated in Figure 4-4, 1 kW, 48V output asymmetrical half bridge (AHB) is able to achieve 94.5% optimal efficiency at 200 kHz switching frequency when it is dedicatedly designed for 400V input and operates with 50% duty cycle. However, to achieve wide operation range from 300V to 400V, duty cycle at 400V input has to be reduced to 30%, which dramatically reduce the converter efficiency. As demonstrated in Figure 4-4, converter efficiency reduces to 92% when the wide operation range is realized.

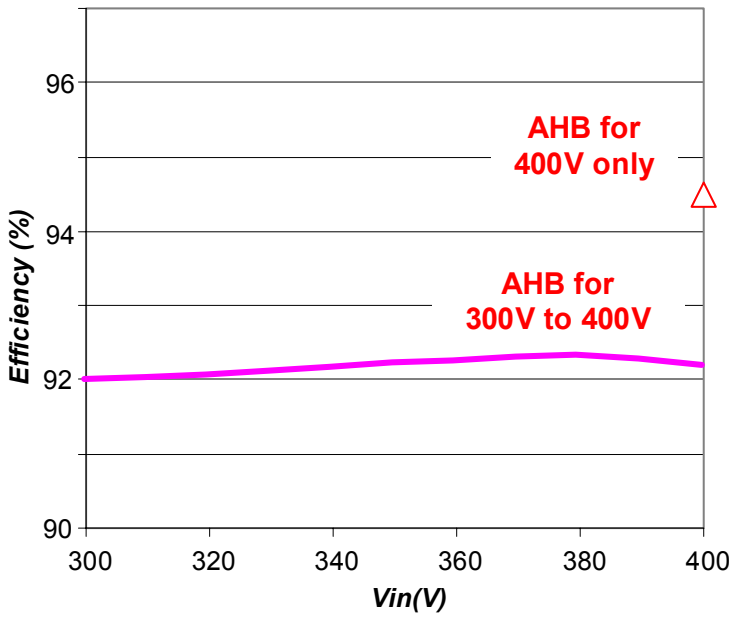


Figure 4-4. Asymmetrical half bridge efficiency.

To allow DC/DC stage accomplishing both wide operation range and high efficiency, different research efforts have been implemented.

By using range winding concept, transformer turns-ratio can be changed during holdup time, as shown in Figure 4-5. In this way, regulation during holdup time can be achieved by using different transformer turns-ratio, instead of compromising the duty cycle [D-3].

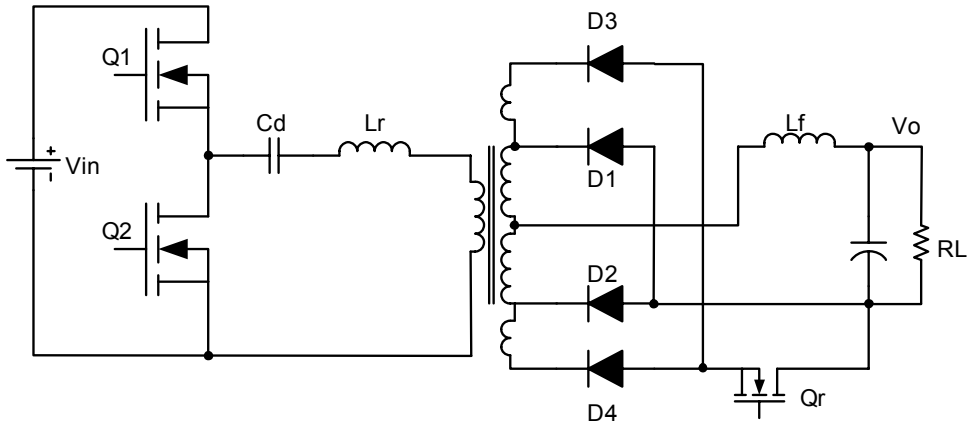


Figure 4-5. Holdup extension by range winding concept.

Holdup extension circuit is an alternative solution, as shown in Figure 4-6. Instead of modifying DC/DC stage topology, adding an extra stage Boost converter can dramatically reduce the duty cycle range of DC/DC stage, so that better efficiency can be achieved. At normal operation, holdup time extension circuit is bypassed by the parallel diode. During holdup time, the extension circuit begins to work and boost the voltage from holdup time capacitor and maintain DC/DC stage input voltage. Therefore, DC/DC stage sees a relatively stable voltage. Thus, DC/DC stage can be designed without considering wide operation

range. Furthermore, under normal operation condition, the extension circuit doesn't work, and all the load current goes through the bypass diode. In this way, very little loss is generated by the extension circuit and circuit is able to maintain high efficiency [D-4][D-5].

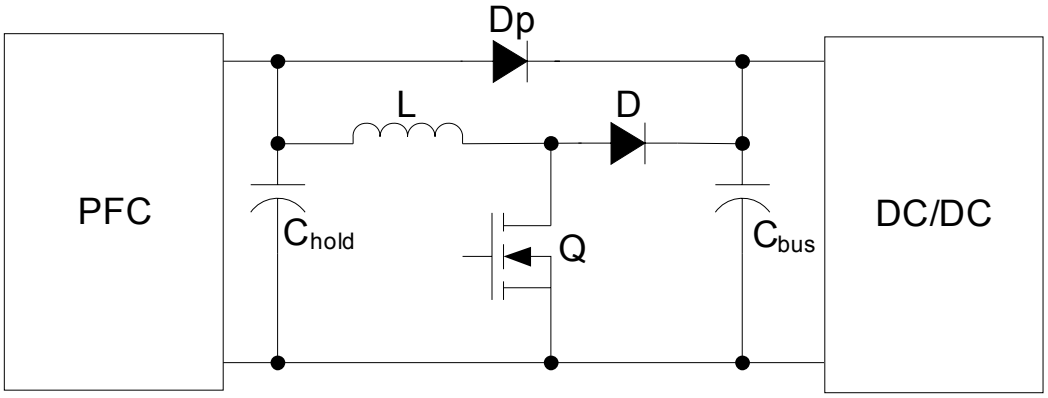


Figure 4-6. Holdup extension circuit.

Although these solutions could results in good circuit performance in the aspects of efficiency, due to the complex circuit structure, together with the concern of stability issues during transient period, these solutions are difficult to be adopted by industry.

Instead of using auxiliary circuit, certain circuit topologies are able to achieve wide operation range without sacrificing normal operation condition efficiency. Among these topologies, LLC resonant converter becomes the most attractive solution due to its smaller switching loss, which enables it operates to very high switching frequency [D-6][D-7]. The LLC resonant converter topology is shown in Figure 4-7. By utilizing the transformer magnetizing inductor, LLC converter modifies the gain characteristic of series resonant converter (SRC).

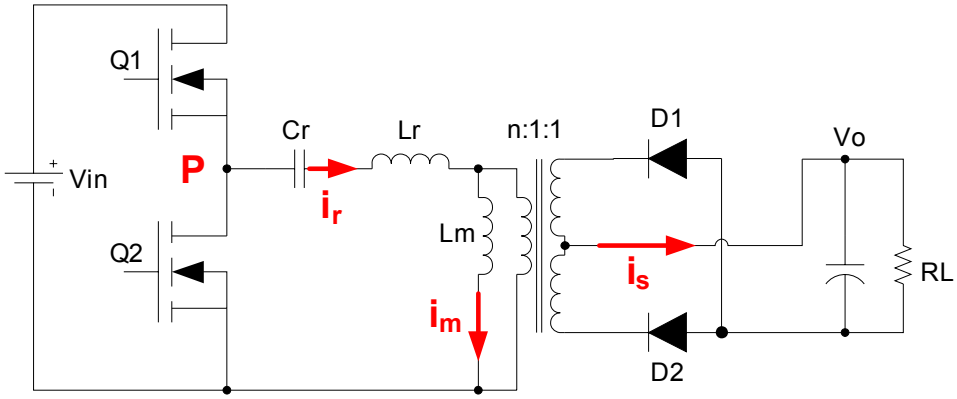


Figure 4-7. LLC Resonant Converter.

LLC resonant converter can achieve both Buck mode and Boost mode operation. When input AC line exists, its input is generated by PFC stage. At this condition, converter operates at its resonant frequency to minimize the conduction loss and switching loss. During holdup time, its input voltage keeps decreasing, and switching frequency is reduced to realize Boost mode and keeping output voltage regulation.

Thus, LLC resonant operate at resonant frequency and achieves maximum efficiency for most of the time. While during holdup time, circuit operates far away from the resonant frequency, and circuit has lower efficiency, this condition only lasts for 20mS and will not cause thermal issue for the converter design.

The other benefit of using LLC resonant converter is its small switching loss. For PWM converters, large ZVS range is achieved by increasing switching turn-off current, which results in large turn-off loss. However in LLC resonant converter, magnetizing inductor current is used to realize ZVS and ZVS can be achieved for all the load conditions with small turnoff current. Therefore, zero

turn-on loss and small turn-off loss can be achieved. Furthermore, secondary side diode of LLC resonant converter turns off with low di/dt. Thus, small reverse recovery loss can be achieved on secondary side. Combining smaller switching loss on both primary and secondary side, LLC resonant converter efficiency is not sensitive to the switching loss and the circuit is able to achieve high switching frequency operation.

In this chapter, firstly, LLC resonant converter is analyzed based on the normal operation and holdup time operation. Secondly, LLC resonant converter design procedure has been developed to achieve high efficiency at normal operation and desirable operation range to minimize the holdup time capacitor. Furthermore, LLC resonant converter has been implemented using 1 MHz switching frequency to demonstrate the high frequency operation capability and verify the design process.

4.2 Operation principles of LLC Resonant Converter

Comparing with series resonant converter, LLC resonant largely reduces the magnetizing inductance. In this way, the magnetizing inductor can be used to realize soft switching for primary side switches. Furthermore, the magnetizing inductor participates into the resonance and modifies voltage gain characteristic. As shown in Figure 4-8, converter gain can be higher or lower than 1. For these

gain curves, switching frequency is normalized with the resonant frequency, which is determined by the series resonant tank and can be represented as

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$$

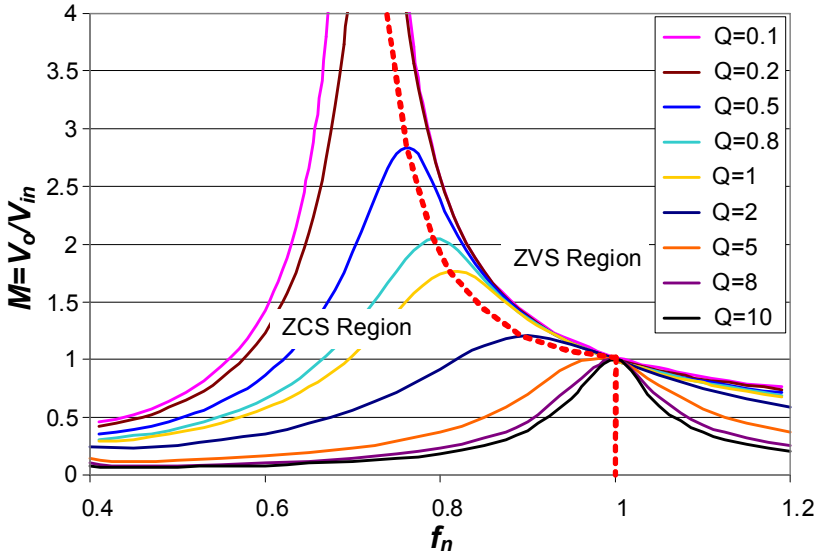


Figure 4-8. Gain characteristic for LLC resonant converter.

Due to different operation mode of LLC resonant converter, its operation principles are quite complex. According to its switching frequency, LLC operation modes can be separated into above, below and equal to the resonant frequency [D-8][D-9][D-10][D-11][D-12].

4.2.1 Switching frequency equal to resonant frequency

For conventional resonant converters, such as SRC and PRC, it is desired to make the converter operate at resonant frequency to maximize the circuit efficiency. However, when these circuits operate on the left hand side of resonant frequency, circuits work with zero current switching. To ensure ZVS operation,

enough design margins has to be considered during design stage. Thus, circuit would not be able to operate at optimal operation point.

For LLC resonant converter, ZVS switching can be achieved for the switching frequency either higher or lower than the resonant frequency. Thus, there is no requirement for design margin and circuit is able to operate with resonant frequency and achieve optimal efficiency.

For the circuit diagram shown in Figure 4-7, operation principle at resonant frequency can be demonstrated in Figure 4-9.The Equivalent circuit of the circuit at different time instance can be summarized in Figure 4-10.

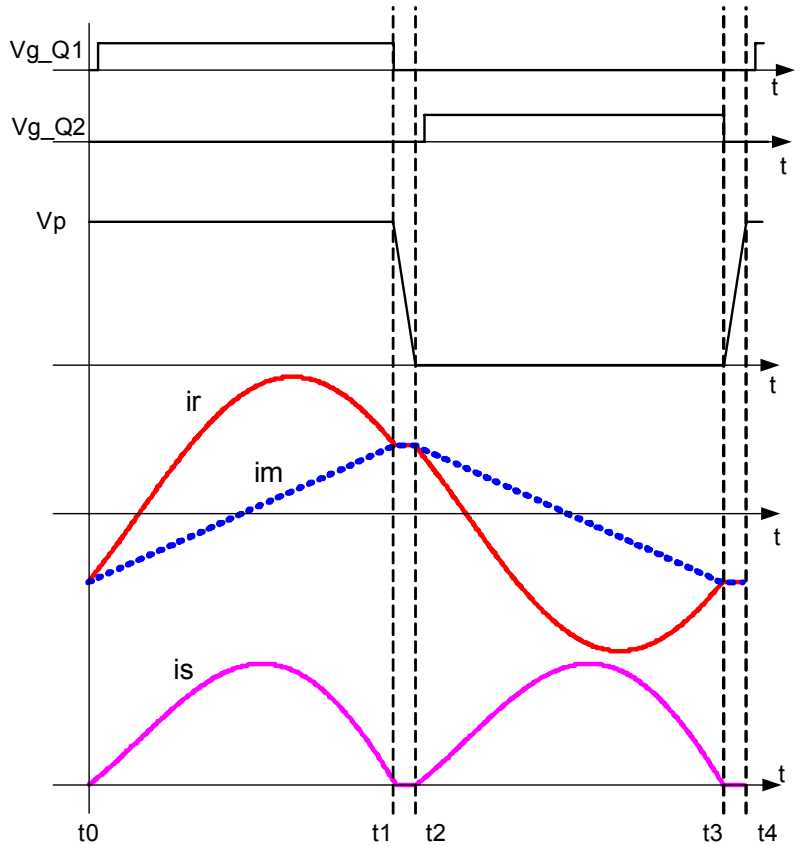


Figure 4-9. LLC resonant converter operates at resonant frequency.

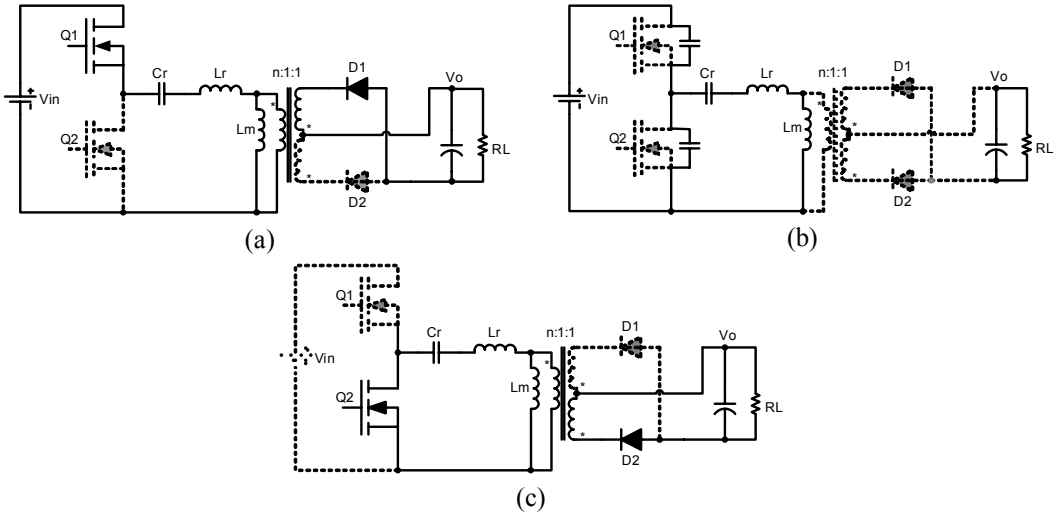


Figure 4-10. Equivalent circuit for LLC circuit at resonant frequency (a) Equivalent circuit from t0 to t1, (b) Equivalent circuit from t1 to t2, (c) Equivalent circuit from t2 to t3.

Between time t0 and t1, switch Q1 is conducting. In this period, resonant tank current is larger than the magnetizing inductor current. According to the polarity of the transformer, secondary diode D1 is conducting. Therefore, voltage applied to the transformer magnetizing inductance is the output voltage reflected to transformer primary side. Thus, magnetizing current linearly increases. During this period, the different between the input voltage and output voltage is applied to the resonant tank, and resonant tank current is a sinusoidal waveform. At time t1, resonant tank current reaches magnetizing current and Q1 turns off. Between time t1 and t2, the equivalent is shown as Figure 4-10 (b). Secondary diodes are off, because the resonant tank current is the same as magnetizing current and there is no current transferred to load. Due to the junction capacitors of Q1 and Q2, magnetizing current discharges the capacitors and help to achieve ZVS turn on of Q2. Between t1 and t2, both Q1 and Q2 are off. This period is always known as

dead-time, which is used to allow enough time to achieve ZVS, as well as prevent shoot through of two switches.

At time t2, Q2 turn on with zero voltage switching. Between time t2 and t3, the different between the resonant tank current and the magnetizing inductor current is transferred to load. After t3, Q2 is turn off and circuit operates into another half cycle.

At resonant frequency, LLC resonant converter is able to achieve ZVS turn on for the primary side switches. Meanwhile, the switching turn-off current is maximum transformer magnetizing inductor current. By choosing a suitable magnetizing inductor, small turn-off loss can be realized. Moreover, secondary diodes turn off with low di/dt, which means smaller reverse recovery loss. Therefore, at resonant frequency, optimal performance of LLC resonant converter is expected.

At resonant frequency, the series resonant tank impedance is equal to zero. Therefore, the input and output voltages are virtually connected together. Thus, the voltage gain at resonant frequency is equal to 1.

4.2.2 Switching frequency higher than resonant frequency

When LLC resonant converter operates with switching frequency higher than resonant frequency, the circuit operates as a SRC circuit. The equivalent circuit and key waveforms are shown in Figure 4-11 and Figure 4-12, respectively.

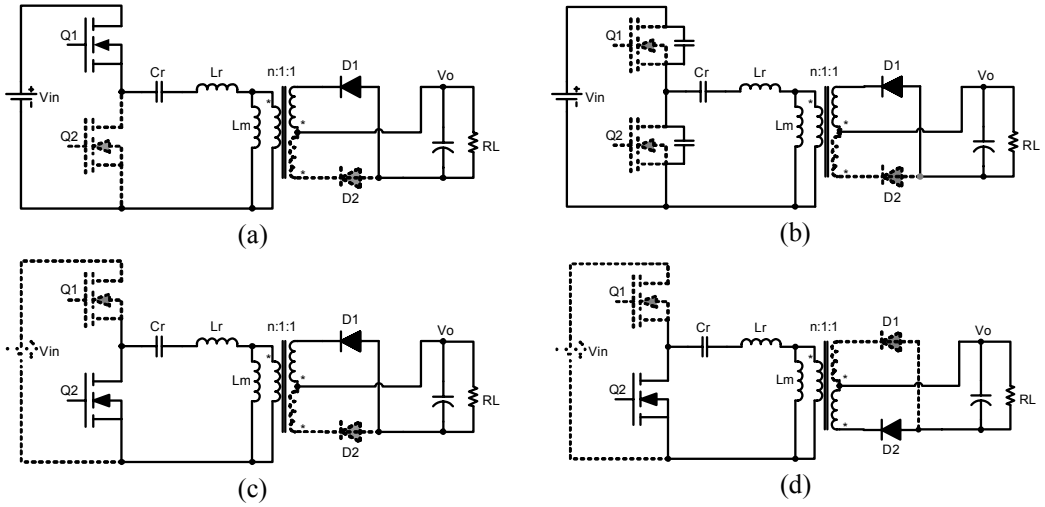


Figure 4-11. Equivalent circuits for LLC switching frequency higher than resonant frequency.

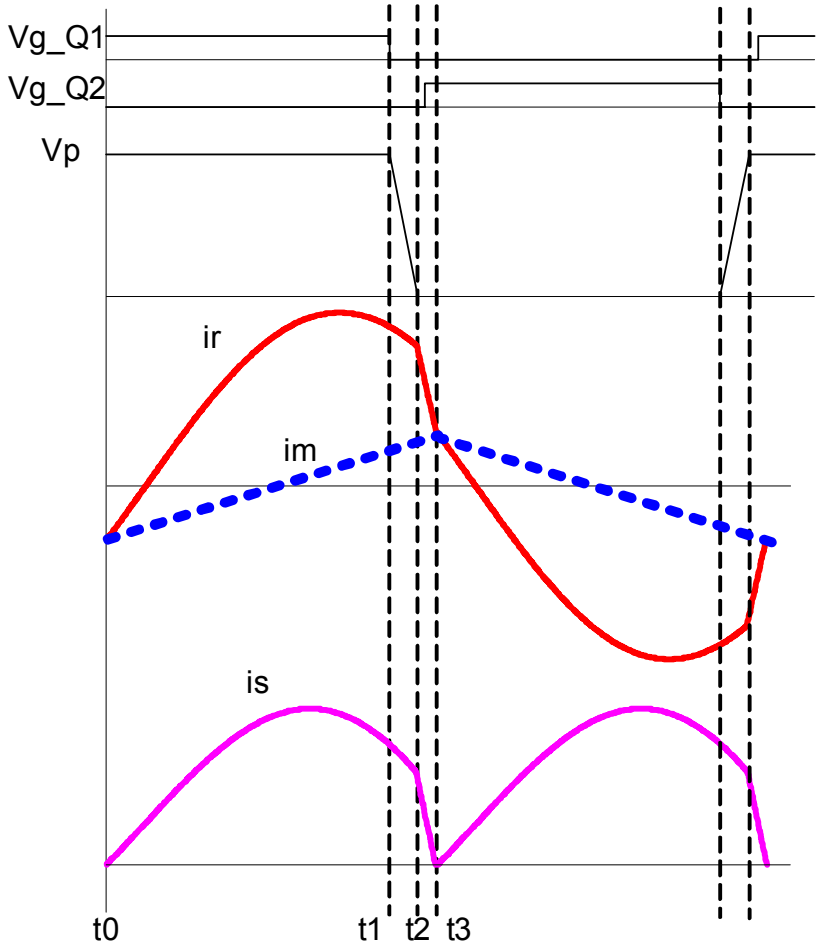


Figure 4-12. LLC resonant converter with switching frequency higher than resonant frequency.

Between time t0 and t1, switch Q1 is conducting and the circuit is transferring energy to load through diode D1. At time t1, Q1 is turned off. Because the switching frequency is higher than resonant frequency, the resonant tank current is higher than the magnetizing current. Between time t1 and t2, both Q1 and Q2 are off, the resonant tank current is charging and discharging the junction capacitors of primary side switches. At time t2, voltage on junction capacitor of switch Q2 is discharged to zero, and Q2 turns on with zero voltage switching. After t2, due to switch Q2 conduction, resonant tank current decreases quickly. At time t3, resonant tank current is equal to magnetizing current and diode D1 turns off. After t3, diode D2 turns on and begins to transfer energy to load.

In this operation mode, ZVS switching on primary side switches can be guaranteed due to the large turn off current. However, the large turn off current generates excessive turn off loss on primary side switches. Moreover, secondary side diode turns off with large di/dt, as shown in Figure 4-12 between t2 to t3, which can cause large reverse recovery on the diodes. Furthermore, the high di/dt turn off of the diode causes extra voltage stress on the diode, which makes the circuit less reliable.

4.2.3 Switching frequency lower than resonant frequency

When the switching frequency of LLC resonant converter is lower than resonant frequency, magnetizing inductor participate in the circuit operation,

which modifies the converter voltage gain characteristics. The equivalent circuit and key waveforms are shown in Figure 4-13 and Figure 4-14, respectively.

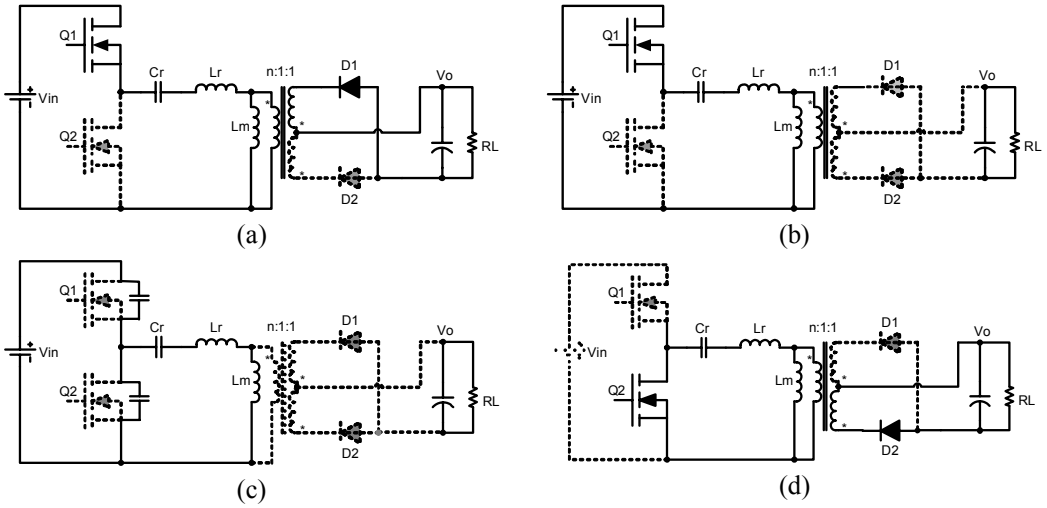


Figure 4-13. Equivalent circuit with switching frequency lower than resonant frequency.

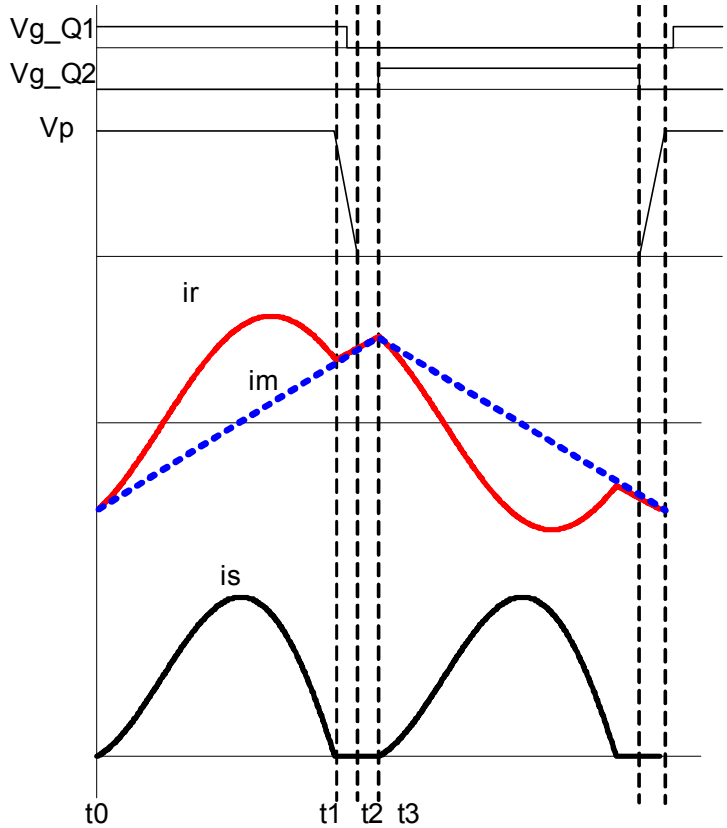


Figure 4-14. LLC resonant converter with switching frequency lower than resonant frequency.

Between time t0 and t1, switching Q1 and diode D1 are conducting, and converter deliveries energy to load. At time t2, resonant tank current resonates back and equals to magnetizing current. After that, magnetizing inductor begins to participate in the resonant. Since resonant current is equal to magnetizing inductor current, diode D1 is turned off. Between time t2 and t3, magnetizing inductor transfers its stored energy to the resonant capacitor. Therefore, in this operation mode, the converter is able to boost gain up. After t3, Q1 turns off, and resonant tank transfers to the body diode of Q2. Thus Q2 achieves ZVS turn on. And then circuit enters the other half cycle.

From previous analysis, it can be seen that LLC resonant converter is able to achieve gain larger, smaller or equal to 1. When the circuit operates at resonant frequency, the converter voltage gain is equal to one, and circuit operates optimally.

4.3 Performance Analysis of LLC resonant converter

4.3.1 Loss analysis on the operation at resonant frequency

By choosing a suitable transformer turns-ratio, LLC resonant converter could operate with resonant frequency at normal condition and achieve high efficiency [D-13]. Since at resonant frequency, converter voltage gain is equal to 1. To allow LLC converter operating with resonant frequency at normal condition, transformer turns-ratio in turn requires meeting the equation

$$n = \frac{V_{in}}{V_o}$$

In this equation, V_o is the desired output voltage, V_{in} is the resonant tank input voltage at normal operation condition, which is equal to the bus voltage for full bridge structure and is equal to half of the bus voltage for half bridge structure.

At resonant frequency, neglecting the dead time, resonant tank current i_r can be simplified as a sinusoidal wave, and the magnetizing current i_m is simplified as a triangle wave. As shown in Figure 4-15.

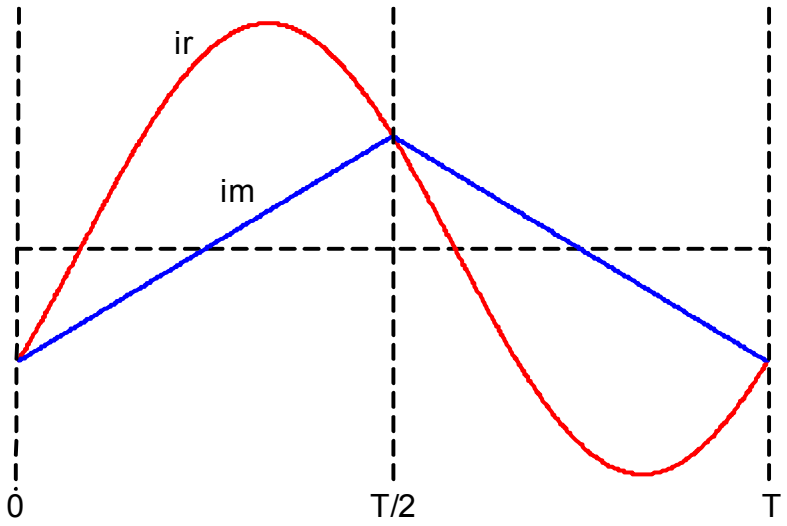


Figure 4-15. Resonant tank current and magnetizing current at resonant frequency.

Thus the resonant tank current can be expressed as

$$i_r = I_{RMS} \sin(\omega_0 t + \phi) \qquad \omega_0 = 2\pi f_0 = \frac{2\pi}{T}$$

In this equation I_{RMS} is the resonant tank RMS current, and ω_0 is angle frequency of resonant frequency. At resonant frequency, magnetizing inductor

current is a triangle waveform, because magnetizing inductor is charged and discharged by output voltage. Therefore, the magnetizing inductor current can be represented as

$$i_m(t) = -i_{m\_\max} + \frac{nV_o}{L_m}(t - nT) \qquad \text{when } nT \le t < \left(n + \frac{1}{2}\right)T$$

$$i_m(t) = i_{m\_\max} - \frac{nV_o}{L_m}\left[t - \left(n + \frac{1}{2}\right)T\right] \qquad \text{when } \left(n + \frac{1}{2}\right)T \le t < (n+1)T$$

Here n is an integer and T is the switching cycle at resonant frequency. i_{m_max} is the peak magnetizing inductor current, which can be calculated as

$$i_{m\_\max} = \frac{nV_o}{L_m}\frac{T}{4}$$

Here V_O is the output voltage, n is the transformer turns ration, L_m is the magnetizing inductance.

According to circuit property, at beginning of each switching cycle, resonant tank current is equal to magnetizing current. Therefore,

$$\sqrt{2} I_{RMS} \sin(\phi) = -\frac{nV_o}{L_m}\frac{T}{4}$$

Meanwhile, the difference between resonant tank current and magnetizing inductor current flows through the load.

$$\int_0^{T/2}\left[\sqrt{2} I_{RMS} \sin(\omega t + \phi) + \frac{nV_o}{L_m}\frac{T}{4} - \frac{nV_o}{L_m} t\right] dt = \frac{V_o}{nR_L}\frac{T}{2}$$

In this equation, R_L is the load resistance. So resonant tank RMS current can be calculated as

$$I_{RMS} = \frac{1}{4\sqrt{2}} \frac{V_o}{nR_L} \sqrt{\frac{n^4 R_L{}^2 T^2}{L_m{}^2} + 4\pi^2}$$

Since the resonant tank current continuously flows trough the primary side switches, its RMS value determines the primary side conduction loss. After it is normalized with load current reflected to primary side, resonant tank RMS current is only related to the magnetizing inductance, the load resistance and the switching cycle. While the switching cycle and load resistance are predetermined values according to the converter specifications, RMS current is only determined by the magnetizing inductance.

However, if considering the definition of L_n and Q, resonant tank RMS current can be transformed into

$$I_{RMS} = \frac{1}{2\sqrt{2}} \frac{V_o}{nR_L} \sqrt{1 + \left(\frac{1}{L_n Q}\right)^2}$$

From the new equation, for the predetermined output voltage, transformer turns ratio and load resistance, the primary side RMS current at resonant frequency is determined by the product of L_n and Q. The calculated primary side RMS current can be normalized with load current, and used to evaluate the primary side conduction loss of the circuit designs, because the output current is the same for different designs.

$$I_{RMS\_normal} = \frac{1}{2\sqrt{2}} \sqrt{1 + \left(\frac{1}{L_n Q}\right)^2}$$

The relationship between the production of L_n and Q is shown Figure 4-16. Primary side RMS current keeps decreasing with the increasing of L_nQ. However, the effectiveness of increasing L_nQ is limited when it is larger than 4. Because when L_nQ is 4, the normalized primary side RMS current is equal to 0.364 and when L_nQ is infinite, the normalized RMS current is reduced to 0.354, only 2.7% improvement can be achieved.

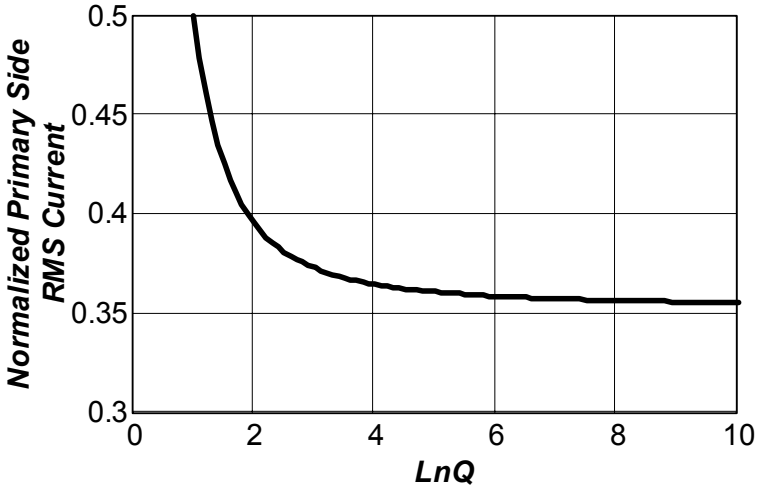


Figure 4-16. Relationship between primary side RMS current with the product of Ln and Q.

Besides the primary side conduction loss, secondary side rectifier conduction loss is also a concern for LLC resonant converter, especially for the low voltage high current applications. Although, diode conduction loss mainly comes from its forward voltage drop and is proportional to the output current, if considering the equivalent resistance of the diode or using synchronous rectification, it is also desirable to minimize the secondary side RMS current.

According to the operation principles of LLC resonant converter, the diode current should be the difference between the resonant tank current and magnetizing inductor current, and its RMS value can be calculated as

$$I_{RMS\_S} = \sqrt{\frac{\int_0^{T/2}[i_r(t) - i_m(t)]^2 dt}{T}}$$

According the equation, secondary RMS can be expressed as

$$I_{RMS\_S} = \frac{1}{4}\frac{V_o}{nR_L}\sqrt{\frac{5\pi^2 - 48}{12\pi^2}\frac{n^4 {R_L}^2 T^2}{{L_m}^2} + 1} = \frac{1}{4}\sqrt{\frac{5\pi^2 - 48}{3}\left(\frac{1}{L_n Q}\right)^2 + 1}$$

In this equation, secondary RMS current is reflected to transformer primary side. Same as the primary side RMS current, secondary side RMS current is also decided entirely by magnetizing inductance. Secondary side RMS can also be normalized with load current, as shown in Figure 4-17. From this curve, it still can be seen that, when $L_n Q$ is larger than 4, increasing it has very limited effects on RMS current reduction.

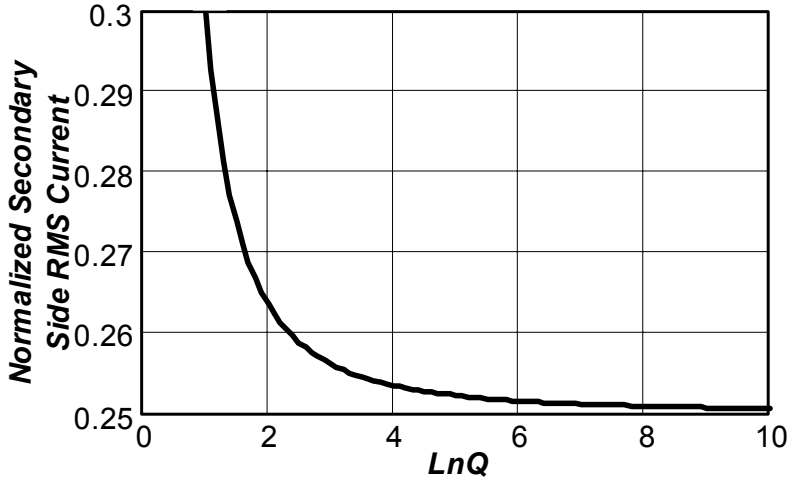


Figure 4-17. Normalized secondary side RMS current.

Through the analysis, both the primary side and secondary side RMS current is only determined by the magnetizing inductor. By increasing the magnetizing inductance, the product of L_n and Q is increased, and the RMS current is reduced, so is the circuit conduction loss. However, when L_nQ is larger than 4, very limited effects can be observed.

The switching loss of LLC resonant converter is caused by the turn-off loss of primary side switches. Because ZVS turn-on can be achieved for primary side switches, there is no turn-on loss generated. However, primary side MOSFETs turning off is hard switching and large turn-off loss is generated. It is desired to have smaller turn-off current. The turn-off current is peak magnetizing current. By choosing a suitable magnetizing inductance, both the ZVS turn-on the small turn-off current can be achieved. Furthermore, secondary diode turn off current has small di/dt because of the resonant tank, which ensures small reverse recover current and loss on the secondary diode. Low di/dt turn off on the diodes also ensures low voltage stress on the secondary rectifier, which enables the circuit use low voltage rating rectifiers and further improve the circuit efficiency.

4.3.2 Performance Analysis During holdup time

During holdup time, LLC resonant converter reduces its switching frequency and boosts the gain up to compensate the reducing input voltage and regulates the output voltage. Because the switching frequency is far away from the resonant frequency, its efficiency is getting lower. However, this operation mode only lasts

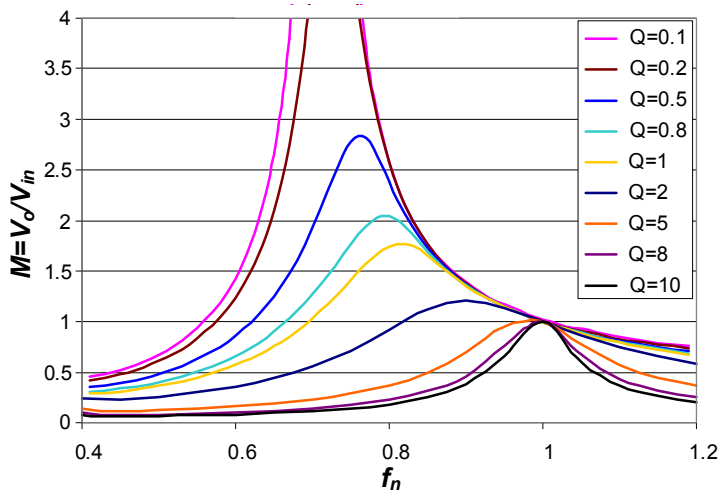
20mS and low efficiency shouldn't be a concern of extra thermal stress. To maintain wide input voltage range and reduce holdup time, circuit should be able to generate enough voltage gain to main regulation during holdup time.

The minimum input voltage that LLC resonant converter allows is decided by the peak voltage gain that can be achieved. At normal operation mode, LLC has a voltage gain equal to one at 400V input voltage. If the converter can achieve a maximum gain of 2, it will be able to regulate output voltage with 400/2=200V input. Obviously, higher the peak gain, the wider the operation range of LLC resonant converter can be achieved.

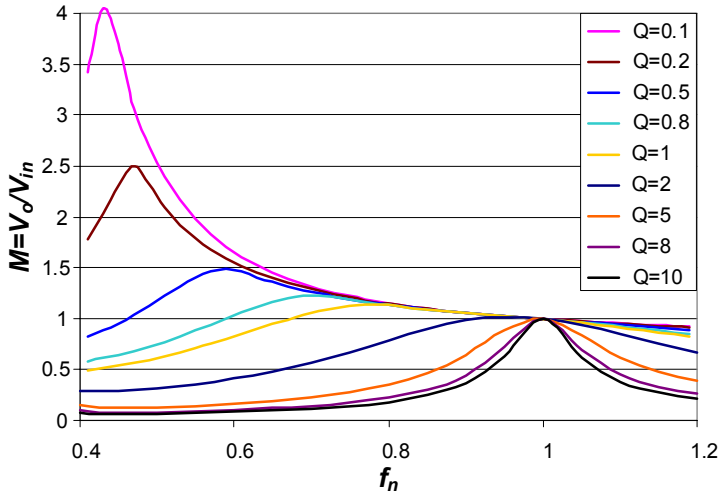
From the operation principle, it can be observed that voltage gain is always equal to 1 when the switching frequency is equal to resonant frequency, no matter what L_n or Q values are. However, for different L_n and Q values, the peak gains that the converter can achieve are different. Although the peak gain might be calculated based on theoretical analysis, there is no close form solution can be found. To simplify the analysis, gain characteristics at different Ln and Q combinations are simulated based on the simulation tool Simplis, which can automatically reach the circuit steady state within short simulation time. The simulation results are shown in Figure 4-18.

From the simulation results, it can be observed that converter voltage gain reaches its peak value at certain switching frequency that is below the resonant frequency. This frequency is determined by L_n and Q values. Different peak gain

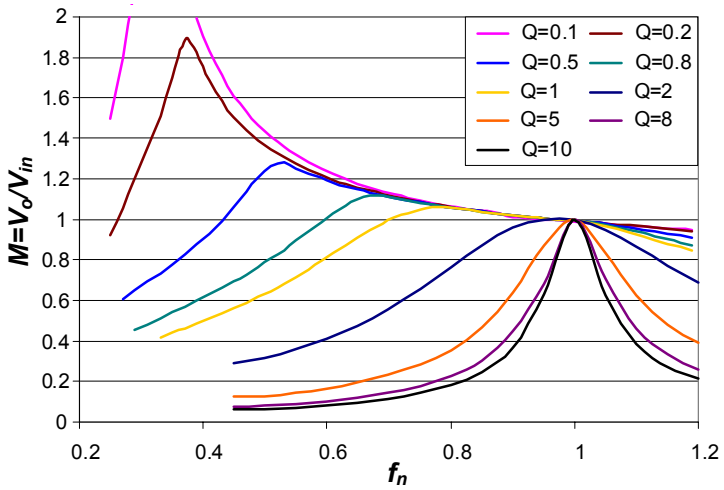
can be achieved according to different L_n and Q combinations. Reducing L_n or Q value can increase peak gain value. Moreover, when L_n value increases, the distance between the peak-gain frequency to the resonant frequency increases accordingly. Moreover, peak gain happens when the circuit is running at the boundary of zero current switching (ZCS) and zero voltage switching (ZVS) modes.



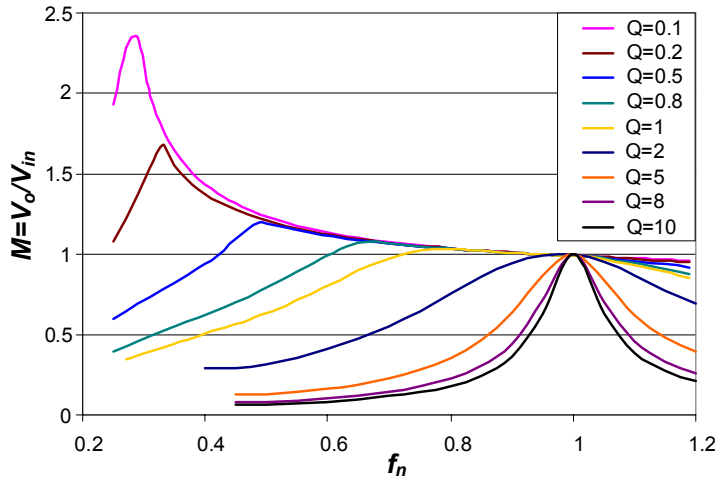
(a) Ln=1



(b) Ln=5



(c) Ln=10



(d) Ln=15

Figure 4-18. Gain characteristics for different Ln and Q.

For each Ln and Q combination, there is one corresponding peak gain that the converter can realize. Therefore, peak gains for different Ln and Q values can be summarized as the colored surface in the 3D map in Figure 4-19. Apparently, peak gain is affected by both Ln and Q values. By reducing L or Q value, higher peak gain can be achieved. According to this map, the valid Ln and Q combinations can be easily narrowed down. For instance, it the converter is required to be able to achieve gain higher than 2, a flat plane with gain equal to 2

can be used to intersect with the peak gain surface. Only the portion that is above the flat plane becomes the valid design, as shown in Figure 4-19.

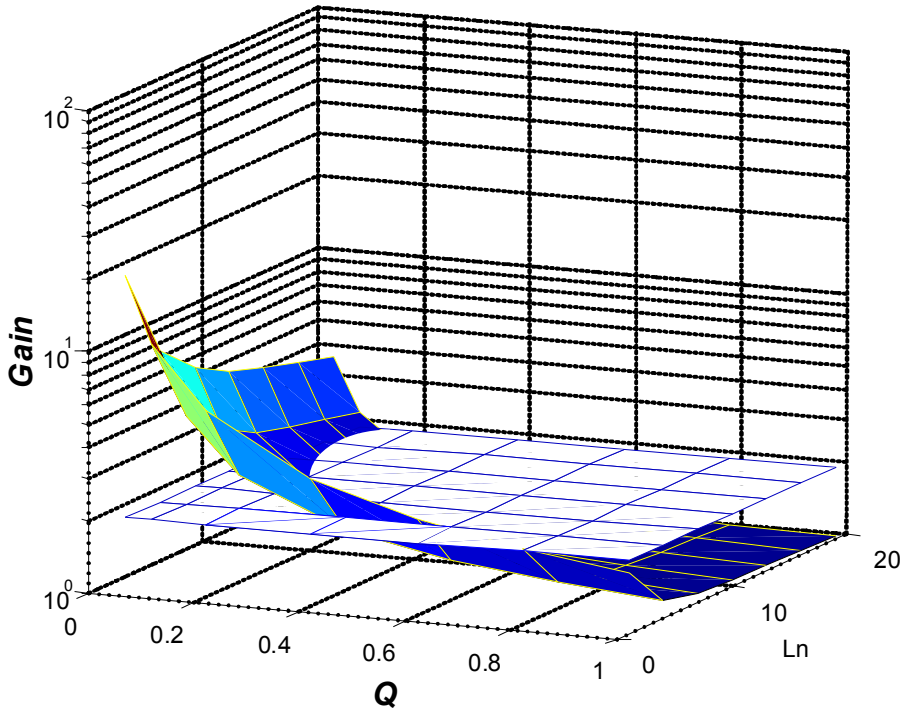


Figure 4-19. Achievable peak gain for different Ln and Q values.

4.4 Design of LLC Resonant Converter

The LLC resonant converter design goal is to achieve minimum loss at normal operation condition together with the capability of achieve required maximum gain to ensure wide operation range. According to previous analysis, the relationships between the design parameters Ln and Q with the converter performance, especially the conduction loss at normal operation condition and the operation range, is revealed. These relationships can be used to develop an optimal design methodology of LLC resonant converter. The proposed design

methodology can be explained by the flow chart shown in Figure 4-20. The keys of successful design relies on choosing the suitable magnetizing inductor and the inductor ratio

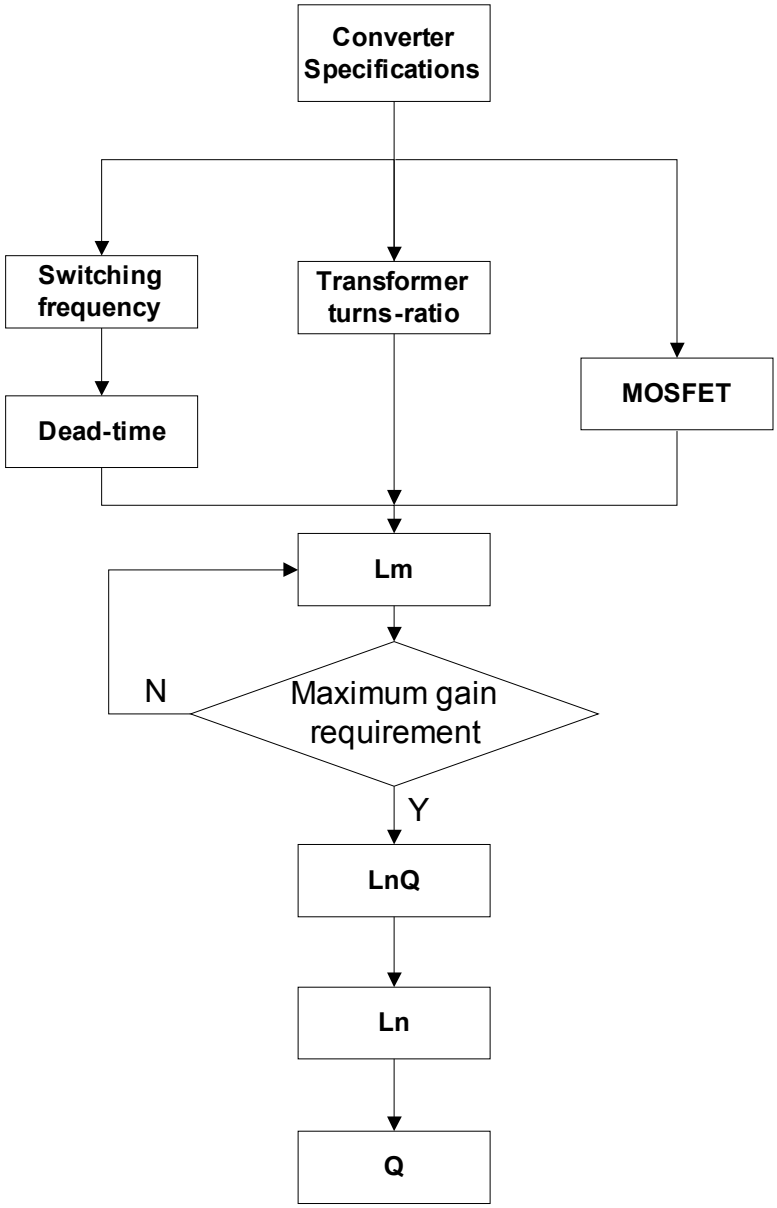


Figure 4-20. Design procedure for LLC resonant converter.

In the design process, switching frequency is determined by the desired coverter efficiency and power density requirement. Normally higher switching

could results in less passive converter size, but less efficiency. Therefore, trade-off is required to choosing a suitable switching frequency. Because switching frequency of LLC resonant converter is equal to resonant frequency for most of the time, this switching frequency also determines the resonant frequency of resonant tank.

4.4.1 Choosing Transformer turns-ratio

The purpose of choosing transformer turns-ratio is to achieve desired voltage gain at normal operation condition. As discussed before, LLC resonant converter could achieve maximum efficiency when its switching frequency is the resonant frequency. Therefore, transformer turns-ratio should be chosen so that, when the input voltage is 400V, the switching frequency should be resonant frequency, which means converter voltage gain is equal to one. Thus

$$n = \frac{V_{in\_normal}}{V_o}$$

In this equation, V_{in_normal} is the resonant input voltage, and it is 400V for a full bridge structure and 200V for a half bridge structure.

4.4.2 Choosing of magnetizing inductor

According to the circuit analysis during normal operation condition, the relationship between the conduction loss and circuit parameters has been revealed. The results show that the conduction loss is purely determined by the

magnetizing inductor value. Larger the inductor value results in a smaller conduction loss.

Beside the conduction loss, switching loss also needs to be minimized. From the circuit operation analysis, LLC converter is able to achieve ZVS turn-on for all the load conditions, as long as the turn-off current meets the ZVS requirement. The soft switching transient happens during the dead-time between two primary side switches gate signals. At resonant frequency, during dead-time, both the primary side switches and secondary side diodes are off. Resonant tank is series with magnetizing inductor and charging the junction capacitors of primary side switches. The equivalent circuit during dead-time can be illustrated in Figure 4-21.

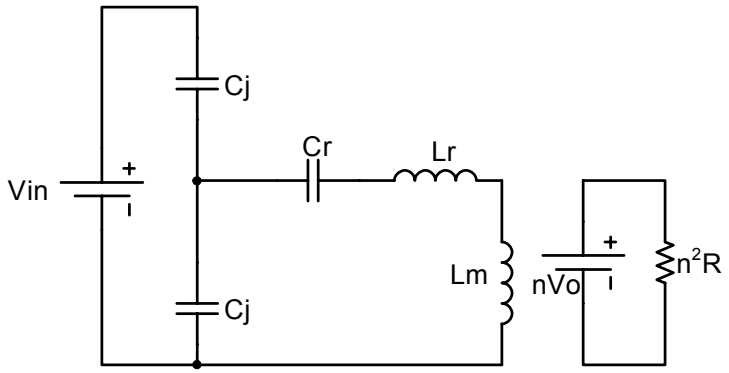


Figure 4-21. Equivalent circuit during dead-time.

Primary side switch turns off with magnetizing inductor peak current. During the transient period, magnetizing inductor current almost keeps constant. To ensure ZVS, peak magnetizing inductor current should be able to discharge the junction capacitors. Thus,

$$I_{m\_\max} t_{dead} \geq 2V_{bus} C_{eq}$$

Here V_{bus} is bus voltage, $I_{m\_\max}$ is peak magnetizing inductor current, t_{dead} is the dead time, and C_{eq} is equivalent MOSFET output capacitor. Because of the nonlinearity of MOSFET junction capacitor, this equivalent capacitor is based on the stored charge.

Considering at resonant frequency, converter voltage gain is equal to one, together with the ZVS criteria, magnetizing inductor should fulfill the equation

$$L_m \leq \frac{T \cdot t_{dead}}{16 C_{eq}}$$

This equation is based on half bridge structure and voltage gain is equal to 1. When the circuit changes into full bridge structure, the equation changes into

$$L_m \leq \frac{T \cdot t_{dead}}{8 C_{eq}}$$

From this equation, it can be observed that magnetizing inductor is proportional to the switching cycle and dead-time, and it is inverse proportional to the equivalent junction capacitor. Increasing dead-time or reducing MOSFET junction capacitor could result in a larger magnetizing inductor and less loss.

Based on the analysis on the RMS currents, the conduction loss increases with the increase of magnetizing inductor, which means the magnetizing inductor is required to be as large as possible. On the other hand, the soft switching requirement gives the maximum magnetizing inductor. Therefore, the optimal

design should be the magnetizing inductor that just meets the soft switching requirement.

However, according to the ZVS criteria, magnetizing inductor is determined by the switching cycle, dead-time and MOSFET junction capacitor. By increasing the dead-time, magnetizing inductor can be increased accordingly, which results in a smaller turn-off current and less turn-off loss. For certain stitching frequency and MOSFET junction capacitor, it is essential to choose a suitable dead-time to achieve the trade-off between the conduction loss and switching loss.

When the dead-time is larger, larger magnetizing inductor can be used while circuit still maintains ZVS capability. In this way, magnetizing inductor could be smaller and turn-off loss is smaller. However, due to the large dead-time, less time is used to transfer energy to the load. Thus, primary side current has to be increased to compensate the duty cycle loss caused by large dead-time.

On the other hand, when the dead-time is chosen too small, more turn-off current is required to maintain soft switching requirement. Therefore, less magnetizing inductor is needed, which results in more magnetizing current and more conduction. Meanwhile due to the large turn-off current, more switching loss is generated.

Apparently, the magnetizing inductor should be designed based on the trade off between the switching loss and conduction loss.

4.4.3 Choosing inductor ration L_n

Besides high efficiency at normal operation condition, LLC resonant converter is required regulating the output voltage during holdup time by reducing its switching frequency. Input voltage range of LLC converter is desired to be larger so that the holdup time capacitor can be reduced. Once input voltage range is decided, resonant tank can be designed accordingly. As analyzed before, the minimum operation voltage of LLC resonant converter is determined by its peak voltage gain. Therefore, to achieve wide operation range of LLC resonant converter, it is essential to achieve enough voltage gain. By using simulation tool, peak gains for different L_n and Q combinations have been demonstrated in Figure 4-19. It can be redrawn into contour curves as in Figure 4-22, which can be used to locate valid design parameters. For instance, if the minimum voltage is required to be 250V, the peak gain of the designed converter has to be higher than 400/250=1.6. Thus, all the L_n and Q combinations that allow the converter peak gain higher than 1.6 could be the valid design. Comparing with the contour curve, all the L_n and Q combinations beneath line 1.6 become the valid designs.

Apparently, there are infinite choices of solutions, to further narrow down the design parameters, magnetizing inductor is considered. The magnetizing inductor is determined by soft switching and conduction loss requirement. However, once magnetizing inductor is chosen, the relationship between L_n and Q has been fixed. From the definition of L_n and Q, their product is

$$L_n Q = \frac{L_m}{L_r}\frac{\sqrt{\frac{L_r}{C_r}}}{n^2 R_L} = \frac{L_m}{n^2 R_L \sqrt{L_r C_r}} = \frac{2\pi f_0 L_m}{n^2 R_L}$$

Once converter specification is defined and switching frequency is chosen, the product of L_n and Q is only determined by the magnetizing inductor. Therefore, for the designed magnetizing inductor, the product of L_n and Q is set.

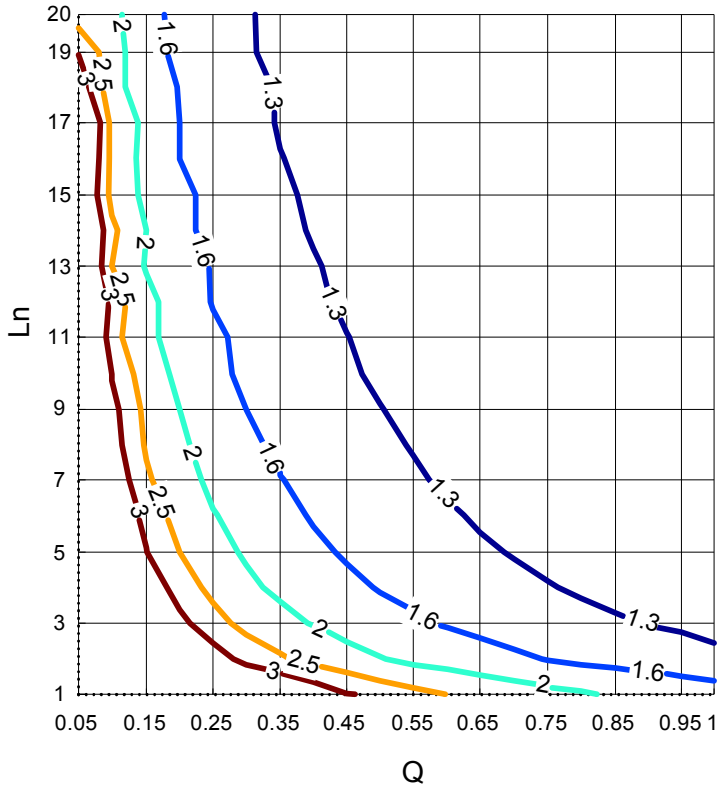


Figure 4-22. Contour curves for LLC converter peak gains.

For instance, for a 200 kHz switching frequency, 1kW output DC/DC converter with 100nS dead-time, if it chooses IXFH21N50 as the switching device, according to the equivalent junction capacitor, the magnetizing inductor is required to be 70uH. Thus, the product of L_n and Q should be

$$L_n Q = 2.2$$

Since the product is a constant, it can be draw in Figure 4-22 as a line, which represent the relationship between L_n and Q for a constant magnetizing inductor value. As shown in Figure 4-23, the marked line represents all the L_n and Q combinations that have the product of 2.2.

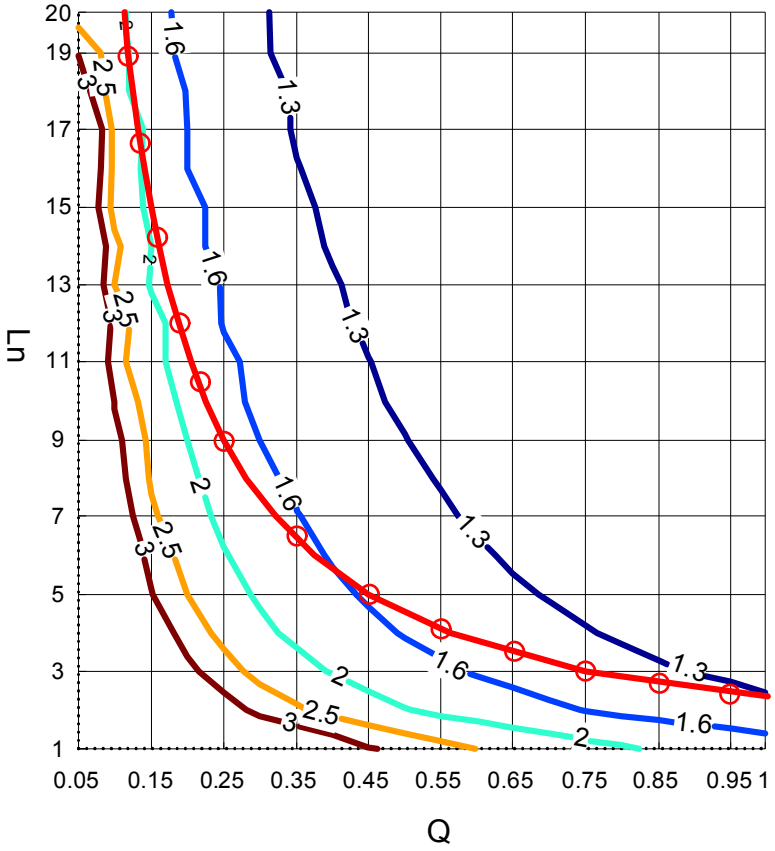


Figure 4-23. Design example of LLC converter.

Therefore, all the L_n and Q combinations along the marked line would give the same conduction loss and switching loss at normal operation condition, because of the same magnetizing inductor. But along the same line, due to different L_n and Q values, the maximum gain can be achieved are different. According to the

maximum gain requirement from the desired operation range of LLC resonant converter, only certain range on the line could be a valid design. From Figure 4-23, all the L_n and Q combinations below line 1.6 could meet the gain requirement. Combining the magnetizing inductor line, L_n has to be larger than 5.5 to meet the gain requirement.

After going through the loss analysis at normal operation and peak gain analysis during holdup time, the choices of circuit parameters have been narrowed down to a portion of constant magnetizing inductor line. Along the line, still infinite L_n and Q combinations can be chosen as valid design. Therefore, the trade off design is required to find a suitable L_n vale. The trade-off should be based on the converter parameters impacts on converter performance.

To evaluate circuit performance, normalizing method is always used for resonant circuit. The normalization method is summarized in Table 4-1.

Table 4-1. Normalization for LLC resonant converter.

	Base
Frequency	$1/\left(2\pi\sqrt{L_r C_r}\right)$
Current on primary side	$V_o/\left(nR_L\right)$
Current on secondary side	V_o/R_L
Voltage on resonant capacitor	V_o
Volt-second on transformer	$2\pi\sqrt{L_r C_r}nV_{out}$

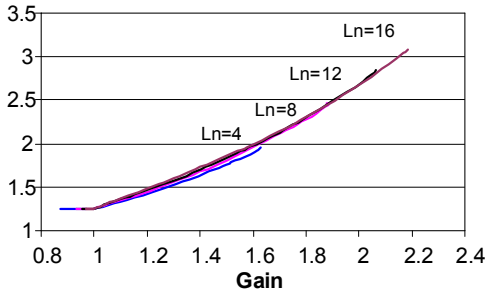
For LLC resonant converter, no matter it is during normal operation condition or holdup time, the input voltage is varying while its output voltage and current keeps the same. Therefore, it is more make sense to use output voltage and current as the normalization base. By using the proposed normalization method, LLC resonant converter can be evaluated with different L_n and Q value for different switching frequency and different power levels.

The primary side current, secondary side current, transformer volt-second and resonant capacitor voltage stress are evaluated with different voltage gains, which are summarized in Figure 4-24. The x-axis is the voltage gain of converter instead of switching frequency, because under the same voltage gain, different converters have the same input voltage and output voltage, which means a fair comparison.

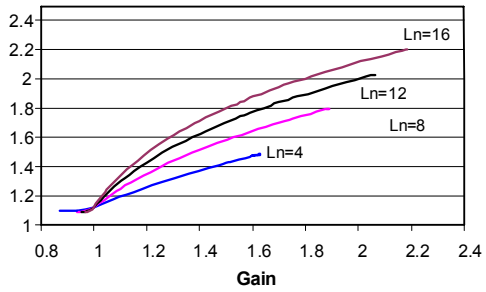
For different L_n value, it can be observed that, when the gain is equal to one, circuit operates at resonant frequency, primary side and secondary side RMS current keeps the same. Because the conduction loss at resonant frequency is mainly determined by magnetizing inductor, different L_n value has no impact on the conduction loss.

However, the capacitor voltage stress reduces with increasing L_n value. Because, according to the definition of Q, for the same magnetizing inductor, larger Ln value means smaller Q value. Thus, the resonant capacitor is lager. Therefore, the voltage stress on the resonant capacitor is reduced.

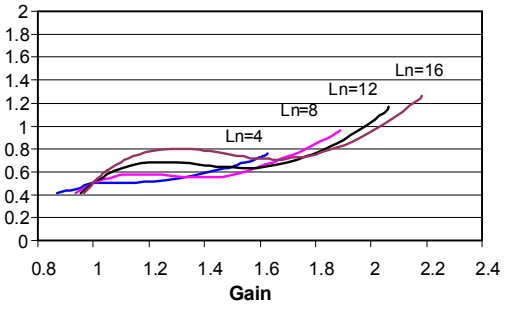
When the voltage gain is larger than one, which means the circuit is at holdup time, larger Ln value results in higher secondary side RMS current and lower voltage stress on the resonant capacitor. For the transformer volt-second, due to large design margin, saturation is not a concern. Besides, the holdup time is only requires 20mS, the extra loss caused by large transformer volt-second won't cause extra thermal stress.



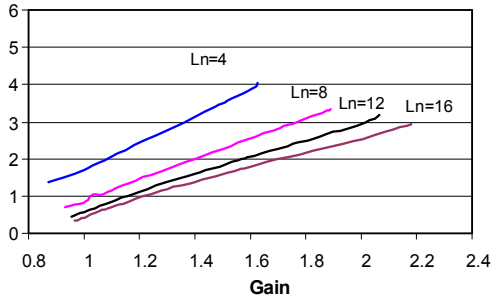
(a) Normalized primary side RMS current



(b) Normalized secondary side RMS current



(c) Normalized transformer volt-second



(d) Resonant capacitor voltage stress

Figure 4-24. Impacts of Ln.

By summary, larger Ln value is desired to achieve smaller resonant capacitor voltage stress. Smaller Ln value is desired to have smaller conduction loss during holdup time. Therefore, the Ln value should be chosen based on the available resonant capacitors voltage rating and its value should be minimized to achieve higher efficiency during holdup time. Based on the chosen Ln and Q values, Lr and Cr can be calculated accordingly.

The design procedure can be summarized as: According to the converter specifications, especially the input and output voltage at normal operation condition, transformer turns-ratio can be design accordingly. By choosing certain switching frequency, the optimal dead-time can be chosen. According to the dead-time and selected MOSFET junction capacitor, magnetizing inductor can be designed. For the designed magnetizing inductor, designer is able to judge if the converter has enough gain to achieve desired operation range. If the converter peak gain is not enough, magnetizing inductor is required to be reduced to meet the gain requirement. Or the trade-off between the holdup time capacitor and converter efficiency can be performed to meet the design goal. After that, Ln value can be chosen based on resonant capacitor voltage stress, and Q can be designed accordingly.

4.5 Mega Hz LLC Resonant Converter

After deriving the design procedure for LLC resonant converter, LLC resonant converter with less conduction loss and switching loss can be achieved [D-1][D-14].

From the previous research results, it can be demonstrated that LLC resonant converter is able to achieve around 95.5% efficiency at 200 kHz switching frequency with 1kW output power. The prototype is shown in Figure 4-25.

Because of the low switching frequency, although the converter is able to achieve high efficiency, only 28W/in^3 power density is achieved.

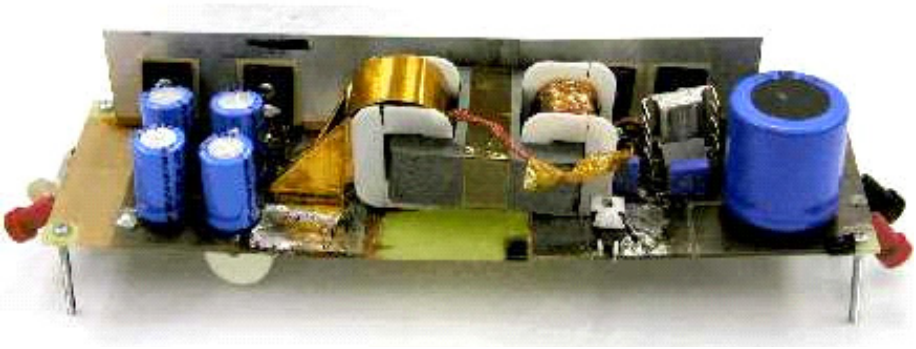


Figure 4-25. 200 kHz LLC resonant converter prototype.

To achieve higher power density, LLC converter switching frequency was pushed up to 400 kHz and still maintain high efficiency. As demonstrated in Figure 4-26, 48W/in^3 power density can be achieved and circuit still maintains efficiency around 94.7%. Comparing with 200 kHz switching frequency, the converter achieves much higher power density with small efficiency drop. Thus, the circuit efficiency is less sensitive to the switching frequency, which means the circuit is able to achieve much higher switching frequency but still maintains high efficiency.

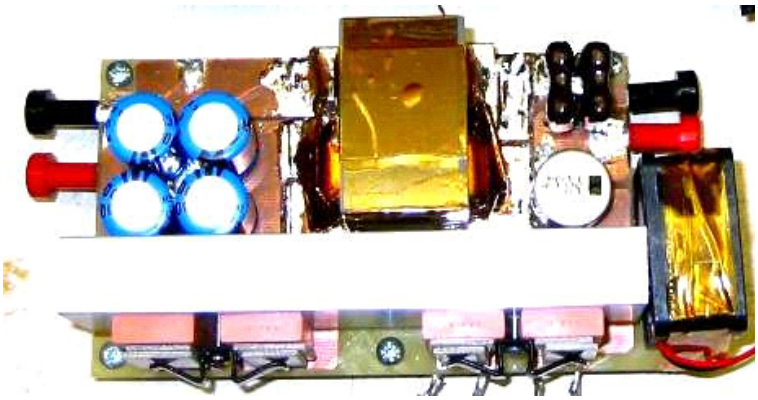


Figure 4-26. 400 kHz LLC resonant converter prototype.

Besides, previous LLC converter design was based on try and error approach, by comparing different designs and picking up a better one. And the operation range of LLC resonant converter is chosen to be from 300V to 400V. Although comparing with the conventional PWM converter, it shows some holdup time capacitor reduction capability. By using the proposed design methodology, LLC resonant converter is able to achieve even wider operation range and further reduces holdup time capacitor, without affecting the converter normal operation condition efficiency.

To demonstrate the high switching frequency operation capability of LLC resonant converter, together with the effectiveness of the proposed design methodology, a 1 MHz switching frequency 1kW LLC resonant converter with 48V output is designed.

According to the analysis on the holdup time capacitor requirement, input voltage range of LLC converter is desired to be wider to achieve smaller holdup time capacitor. However, according to the capacitor manufacturers, the capacitance can be used as holdup time capacitor is limited. The commercially available 450V electrolytic capacitor is 330uF, 270uF, 220uF, and 180uF. To ensure even distribution of ripple current, identical capacitors are used when the parallel is required. Therefore, by considering this effect, the relationship between the holdup time capacitor and the minimum DC/DC stage input voltage can be refined as shown in Figure 4-27.

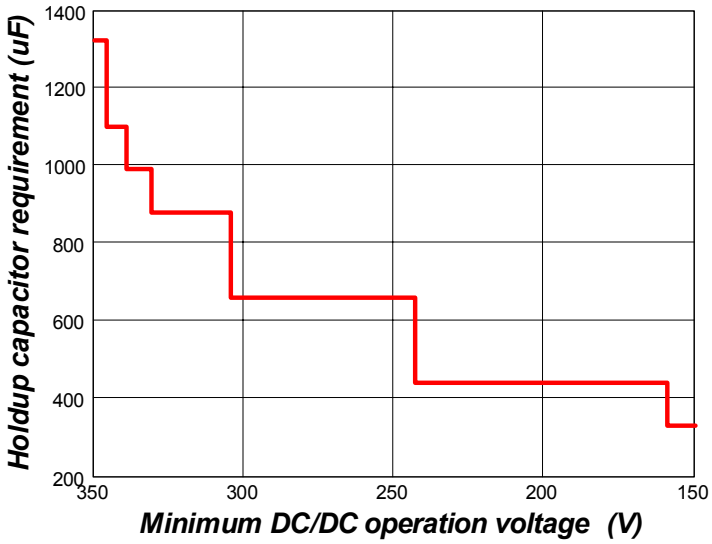


Figure 4-27. Relationship between holdup time capacitor and minimum DC/DC input voltage by considering limited capacitor choices.

The holdup time capacitor requirement changes dramatically around certain voltages. Slightly reduce the minimum input voltage could result in a much smaller holdup time capacitor. For conventional PWM converter to achieve high efficiency at normal operation condition, minimum operation voltage is normally set to around 330V. Thus, 880uF capacitors are required to meet the holdup time requirement. However, if the minimum operation voltage can be reduced to around 230V, the holdup time capacitor can be reduced to 440uF and achieve 50% size reduction. Thus, the peak gain of LLC resonant converter has to be higher than 1.8 to meet the operation range requirement.

Because the input voltage at normal operation condition is 400V and output voltage is 48V, to ensure the converter operating at resonant frequency at normal operation condition, the transformer turns-ratio is required to be the ratio between input and output voltage. Thus,

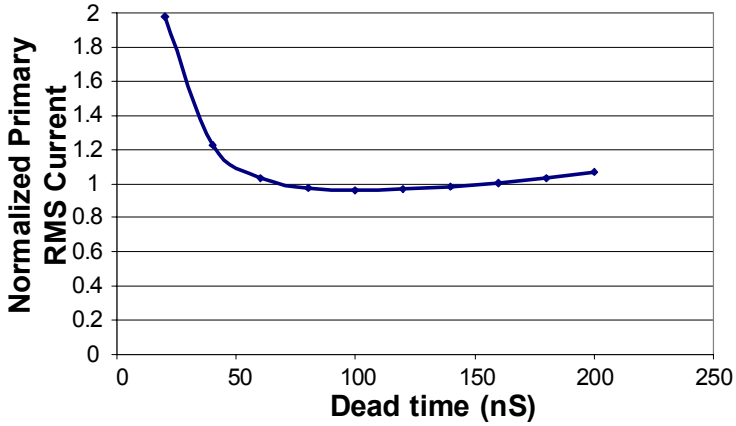
$$n = \frac{400/2}{48} \approx 4$$

Because of the half bridge structure, half of the input voltage is used to calculate the turns-ratio.

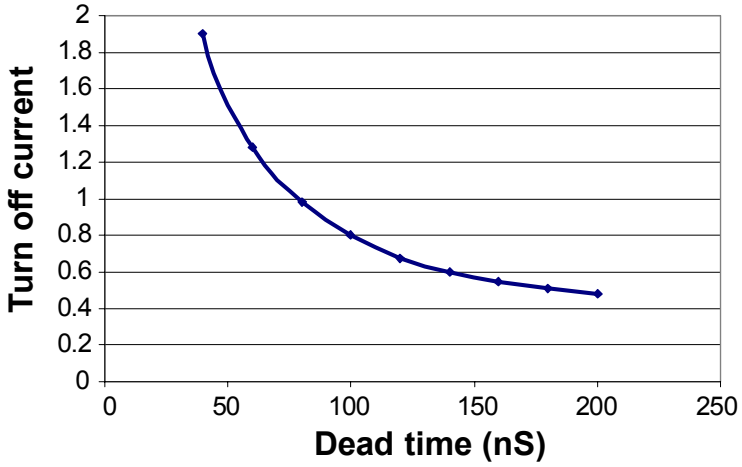
According to the 400V input voltage and 1 kW power level, IXFH21N50F from IXYS is chosen as the switching device, because of its small input capacitor and fast recovery body diode. Due to the high switching frequency, driver circuit for the MOSFET is a big challenge. To ensure small driver loss and fast driving speed, it is desirable to have MOSFET with smaller input capacitor. Moreover, because MOSFET body diode is used to achieve ZVS turn-on, it is required to be fast recovery diode, so that it can block voltage after MOSFET turning off. For secondary side rectifiers, MBR20200CT from Onsemi was used. Although its voltage rating is 200V, it shows the better performance comparing with other 150V rating diode from other venders.

After the selection of switching devices, the magnetizing inductor can be chosen according to the dead-time. As discussed before, the chosen of dead-time is based on the trade-off between the conduction loss and switching loss. For 1 MHz switching frequency, the relationship between the dead-time and converter conduction loss and switching loss can be represented in Figure 4-28. The switching loss is represented by primary side switch turn-off current and conduction loss is represented by primary side RMS current. It can be observed that the switching loss keeps decreasing with increasing dead-time. While for the

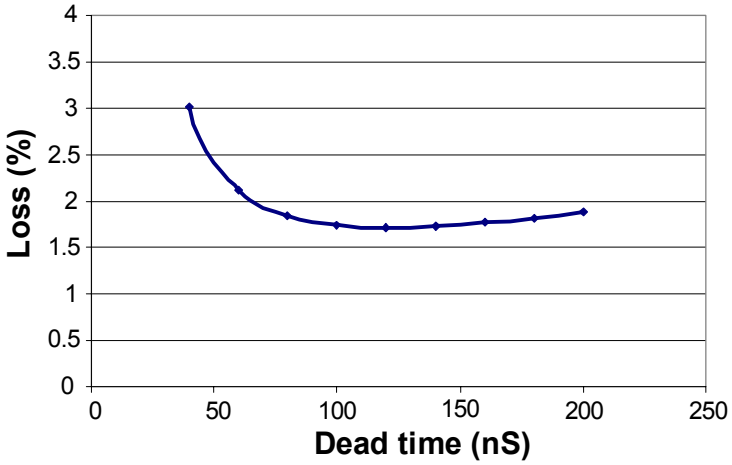
conduction loss, it firstly decreases with increasing dead-time. After dead-time is larger than 150nS, the conduction loss increases again. By combining the conduction loss and switching loss, it can be observed that the total loss reaches its minimum value around 120nS. Thus, 100nS dead-time is chosen as the design. According to the dead-time selection, together with the junction capacitor of IXFH21N50F, the magnetizing inductor can be chosen as 13uH.



(a) Normalized primary side RMS current



(b) Normalized primary side turn-off current



(c) Total loss

Figure 4-28. Relationship between dead-time and converter losses, (a) conduction loss, (b) switching loss, (c) total loss.

To realize operation range from 230V to 400V, according to the peak gain map of LLC resonant converter, the valid design of Ln and Q combinations are required to below the line that represents peak gain equal to 1.8, as demonstrated in Figure 4-29. Combining the designed magnetizing inductor, Ln value can be chosen as the intersection of two curves and equal to 10. To leave enough design margin, chosen as 15. Therefore, the resonant inductor is 0.85uH. According to 1MHz resonant frequency, the resonant capacitor needs to be 30nF.

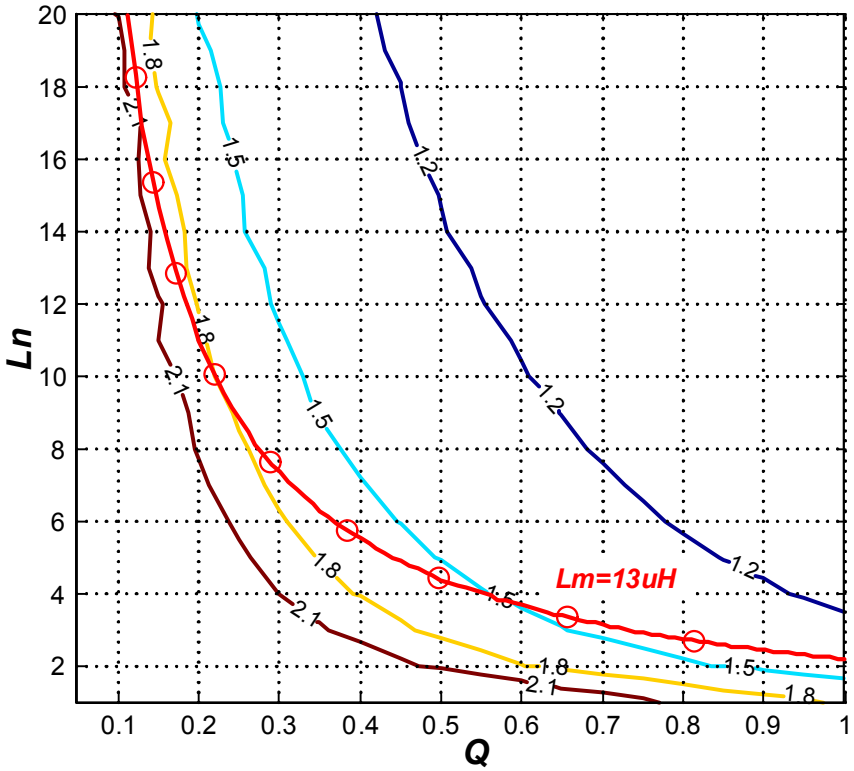


Figure 4-29. Design curves for 1MHz LLC resonant converter.

The circuit parameters have been summarized in Table 4-2 and compared with 200 kHz and 400 kHz switching frequency. It can be observed that the transformer size can be dramatically reduced by using 1MHz switching frequency. Although at 1MHz switching frequency, the resonant capacitor keeps the same value as 200 kHz switching frequency, the designed converter allows the minimum input voltage lower down to 200V and reduces the holdup time. Comparing with conventional design shown in Figure 4-1, the holdup time capacitor could be reduced from 11000uF to 440uF, and about 60% size reduction can be achieved. The prototype of 1MHz LLC resonant converter is shown in Figure 4-30. Its dimension is 5"×1.5"×1.75". Thus, 76W/in^3 power density can be achieved.

Table 4-2. Design Parameter for LLC Resonant converter.

Switching frequency	200kHz	400kHz	1MHz
Magnetizing inductor	70u	40u	12u
Resonant inductor	14u	7u	0.85u
Resonant capacitor	48n	24n	30n
Transformer core size	1 Set EE55/28/21	2 Sets of E43/10/28	1 Set E43/10/28

Comparing with 400 kHz prototype, 70% power density improvemesnt has been achieved. Furthermore, by using the proposed design method, the minimum input voltage is around 200V, which reduces the holdup time capacitor to 440uF and achieves 30% size reduction comparing with 400 kHz LLC. The experimental waveforms at resonant frequency and during holdup time are shown in Figure 4-31 and Figure 4-32, respectively.

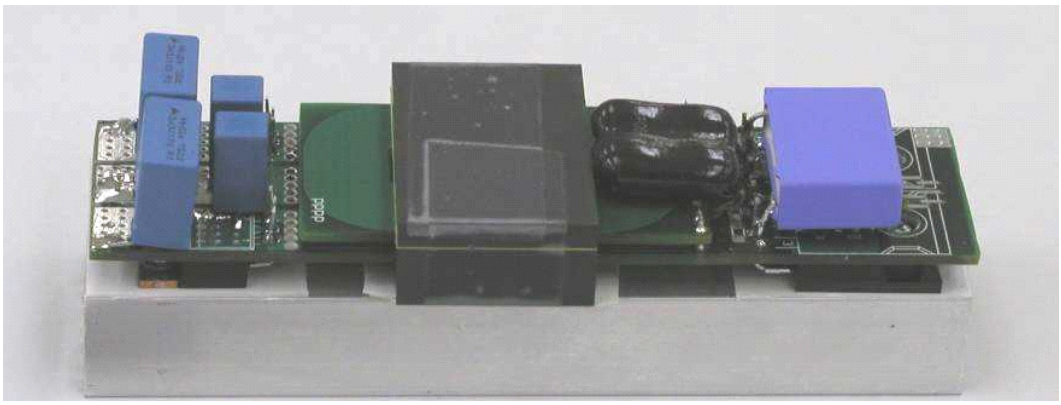


Figure 4-30. Prototype of 1MHz LLC resonant converter.

From the experimental results, at resonant frequency, soft switching can be achieved with minimum turn off current. By changing Lr and Cr combination, the

waveform keeps the same, which verifies the analysis that the loss purely relies on the magnetizing inductance. During holdup time, the converter has to reduce switching frequency to boost up voltage gain. As shown in Figure 4-32, most of the energy stored in the magnetizing inductor is transferred back to the resonant capacitor and gain can be achieved higher than 2.

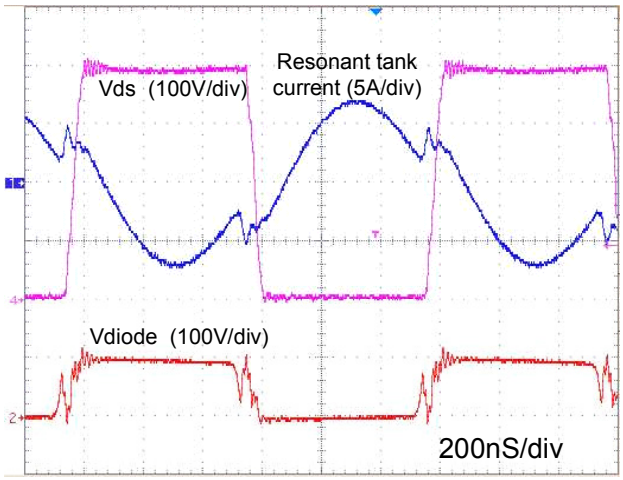


Figure 4-31. Experimental waveform at resonant frequency.

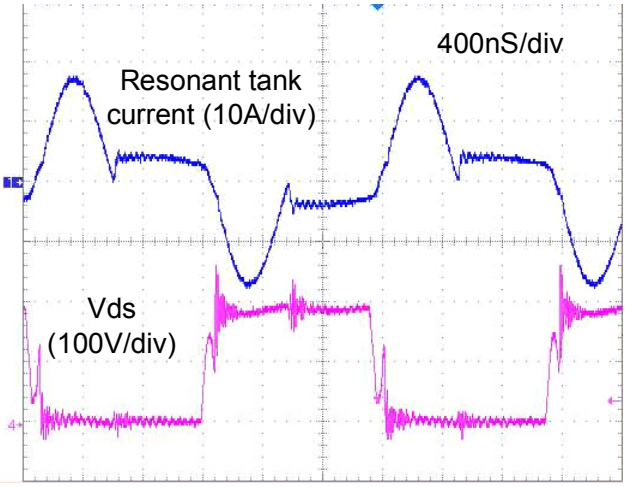


Figure 4-32. Experimental waveform during holdup time.

The efficiency of 1MHz LLC resonant converter with different load conditions is shown in Figure 4-33. The efficiency reaches its maximum

efficiency 94.5% at about 700W output power. At full load condition, the efficiency drops down to 92.5%. Comparing with lower switching frequency cases, slightly efficiency drop can be observed.

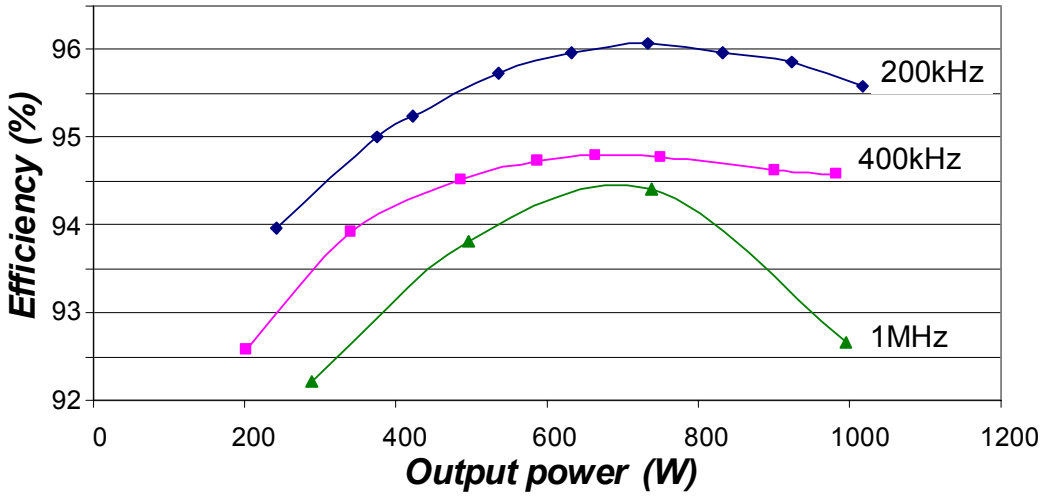


Figure 4-33. Efficiency comparison of LLC resonant converter.

Although the developed prototype is able to achieve high efficiency with 1 MHz switching frequency, it is important to get detailed loss breakdown and estimate the further switching frequency increasing possibility. According to the circuit operation waveform, loss breakdown of the designed converter under 400V input and 1kW output is summarized in Figure 4-34. Because of the diode rectification, secondary diode conduction loss is the main loss. Moreover, considering the switching loss on primary side, it reaches 5.6W at 1MHz switching frequency, which is about 0.5% of the total power. Moreover, the loss density of the transformer reaches 700kW/m^3, for ΔB is equal to 50mT.

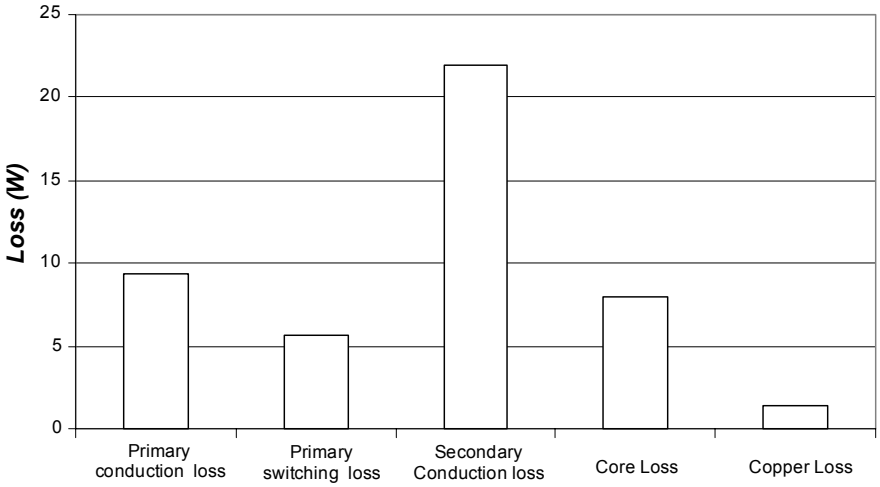


Figure 4-34. Loss breakdown of designed converter.

There is about 2% efficiency error between the theoretical analysis and experimental results, which is mainly caused by the loss estimation for the transformer copper loss and secondary diode switching loss. Because the planar transformer structure, skin effects and approximate effects can largely increase the conduction loss, which can be further improved by better winding structure design through 3D finite element analysis (FEA). For the diode switching loss, it is getting more and more sever when the switching frequency is higher because di/dt of turn-off current is getting higher for high frequency case. Thus the switching loss is no longer neglectable at higher switching frequency.

The major benefit of higher switching frequency for DC/DC converter is to shrink the passive component size. But its effectiveness is limited by the thermal management. For the present transformer design, to achieve low loss density, high performance 3F4 material was used, which is suitable for the switching frequency 1 to 2 MHz. Although ΔB is chosen as 50mT, 700kW/m^3 loss density is generated

in the ferrite core. The relationship between 3F4 material loss density and switching frequency, peak flux density can be represented as

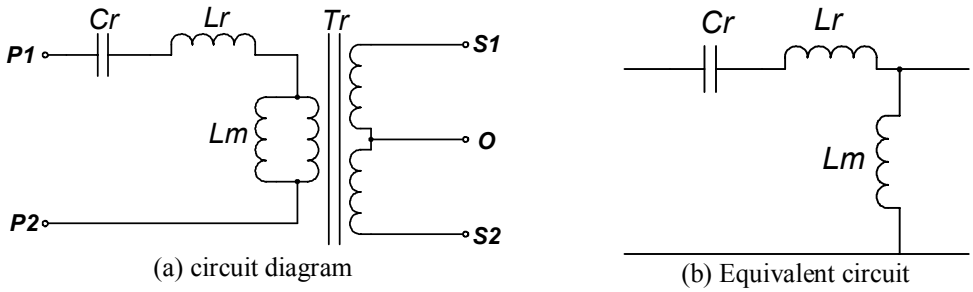
$$P_h = 0.0001005 \cdot f^{2.8} \Delta B^{2.4}$$

When the switching frequency is further increased, transformer flux density has to be decreased to maintain similar loss density. Thus, the transformer size decreasing is getting less to maintain similar loss density, which means the diminishing return on the high switching frequency. Therefore, more detailed analysis is required to estimate the switching frequency impacts on the transformer size.

Furthermore, when switching frequency is getting higher, switching loss increases linearly. In the designed prototype, switching loss takes 1~2% efficiency. Apparently, further increasing switching frequency needs to consider the converter efficiency requirement.

4.6 Future work for LLC resonant converter

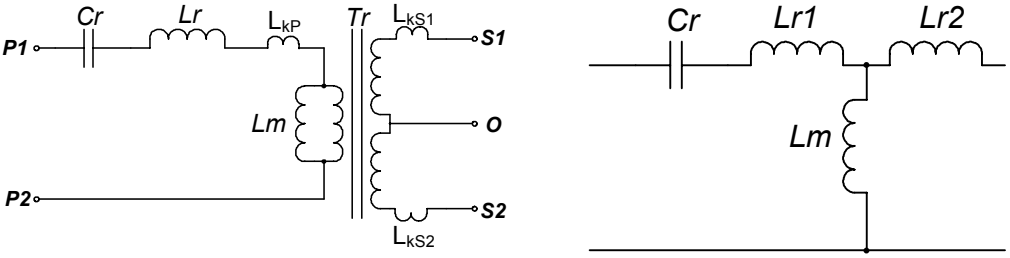
For LLC resonant converter, the key components are the resonant inductor, capacitor and magnetizing inductor. To achieve the performance as theoretical analysis, the desired equivalent circuit is shown in Figure 4-35.



(a) circuit diagram (b) Equivalent circuit

Figure 4-35. Equivalent circuit for ideal LLC resonant tank.

When the switching frequency is low, parasitics of transformer, especially the leakage inductance on transformer primary and secondary side can be ignored. However, when switching frequency is pushed up, resonant components values keep decreasing. Thus transformer parasitic components can't be ignored. They begin to participate into resonance. Because the leakage inductances exist on both primary and secondary side, the equivalent circuit for resonant tank changes in to the equivalent circuit shown in Figure 4-36. Therefore, these leakage inductances should be controlled as small as possible. Further more, because of diode turn-off current has higher di/dt at high switching frequency, leakage inductances of secondary windings are desired to be well coupled together, so that the extra switching loss caused by diode reverse recovery current can be recovered.



(a) LLC Passive IPEM considering leakage (b) Equivalent resonant tank

Figure 4-36. LLC Passive IPEM with leakage inductance

Therefore, different transformer winding structures need to be investigated, so that these parasitic components can be controlled. Besides, because of the low output voltage and high output current interleaving winding structure also need to be considered to achieve smaller winding loss.

Furthermore, because the parasitic components couldn't be totally removed, it might be new research opportunities to find a suitable resonant tank that can absorb the transformer parasitics while maintain same gain characteristic of LLC resonant converter.

4.7 Summary

Front-end AC/DC converter is under the pressure of continuous increasing power density requirement. By using high switching frequency PFC stage, Boost inductor size and EMI filter size can be reduced to achieve higher power density. However, to further improve the power density, bulky holdup time capacitor becomes the bottleneck for further improvement.

To reduce the holdup time capacitor, wide operation range DC/DC converter is required. For conventional PWM converters, increasing operation range is achieved by sacrificing the normal operation efficiency. Although by using auxiliary holdup time extension circuit, high efficiency can be achieved together with smaller holdup time capacitor size. Due to the complex structure, it becomes less attractive comparing with LLC resonant converter.

By reducing the magnetizing inductor, LLC resonant converter modifies SRC and able to achieves gain higher or lower than 1. At normal operation condition, LLC resonant converter operates with resonant frequency and achieves maximum efficiency. When the input voltage drops, switching frequency can be reduced to boost converter gain up and maintain regulated output voltage. During holdup time, less efficiency is achieved, which is not a concern for the converter design. Furthermore, the smaller switching loss makes the converter suitable for operating with high switching frequency and maintains high efficiency.

Although smaller switching loss and the capability of wide input range operation makes LLC resonant converter quite attractive for front-end AC/DC converters, lack of design methodology makes the converter less valuable, because of its complexity. In this chapter, based on the theoretical analysis on the circuit operation at resonant frequency and maximum gain point, the relationship between the converter loss and operation range has be revealed. Based on the relationship, the converter efficiency can be optimized with a good magnetizing inductance design. Moreover, by choose Ln and Q from the peak gain curves, the operation range of the LLC resonant converter can be ensured.

The developed methodology has been implemented into a 1MHz 1kW LLC resonant converter design. And the experimental results verify the theoretical analysis. By pushing the switching frequency up to 1MHz, LLC resonant converter is able to achieve 92.5% efficiency at full load and 94.5% efficiency at

700W output. 76W/in^3 power density can be achieved. Comparing with 400 kHz switching frequency, 70% power density improvement is achieved. Furthermore, by using the proposed design method, the minimum input voltage can be reduced to 200V, which results in 440uF holdup time. Comparing with conventional PWM converter design with 330V minimum input voltage, 50% size reduction of holdup time capacitor can be achieved by using LLC resonant converter.

Chapter 5. Prospects of Power Integration

5.1 Introduction

With the development of information technology, power supply industries are under constant pressure of producing front-end AC/DC converters with higher power density, lower profile and less cost. To improve circuit power density, as discussed in previous chapters, different circuit topologies and semiconductor devices have been proposed and evaluated to find the best candidate to achieve higher efficiency. By using high frequency switching power conversion techniques, circuit power density can be greatly improved because of less passive components size. However, some fundamental limits start to show up when the higher frequency operation is desired. For example, the parasitic inductance in the switch commutation loop hampers the switching speed and causes more switching losses. Large voltage stress appears on switching devices due to large parasitic inductance, which greatly reduces circuit reliability. Besides, parasitic capacitance between high voltage transition points to the earth ground affects the common mode noise a lot. Moreover, the parasitic components brought by the interconnection of the electrical layout played a negative role in the system electromagnetic interference noise (EMI) if it is not treated carefully.

For the motor driver industries, because of the standard phase-leg topology, standardization has been implemented for many years. Power modules with semiconductor devices, drivers and protections are commercially available.

However, the front-end converter products to date are essentially custom-designed and manufactured using discrete parts, which increase labor and ultimately cost of power electronics equipment.

To address these issues and significantly improve the performance of the power electronics product, the integrated power electronics module (IPEM) concept was proposed by Center of Power Electronics Systems (CPES). Following the concept, integration efforts have been made for the front-end AC/DC converters [E-1][E-2][E-3][E-4].

IPEM concept relies on the integration of different devices used in power electronics converters, which includes the active device integration, or Active IPEM, and passive device integration, or Passive IPEM. One apparent benefits of integration comes from the size reduction. Besides size reduction, by integrating the switching devices together with their associated gate driver circuit, parasitic components on the switching commutation loop are greatly reduced, which results in smaller switching loss and less voltage stress. By integrating inductors, capacitors, together with power transformer, passive component size can be reduced. Moreover, due to the integration, circuit component number can be reduced, so are the interconnections, which make the system easier manufacturing. Furthermore, by using IPEM concept, switching stage and passive components become standard building block. Therefore, the cost of production could be greatly reduced.

In this chapter, IPEM concept is firstly introduced to a 200 kHz asymmetrical half bridge converter. By integrating the switching devices together with their associated gate drivers, switching commutation loop parasitic inductances are greatly reduced, which is demonstrated through Maxwell 3D simulation. Because of the parasitics reductions, switching performance of DC/DC converter can be largely improved. Besides active integration, Passive IPEM is also demonstrated through the integration. By integrating inductor, transformer and DC blocking capacitor together, passive components size could be largely improved. Furthermore, because of high integration level, interconnections among these devices are greatly simplified. Through the hardware demonstration, 3 times power density improvement can be achieved by IPEM approach.

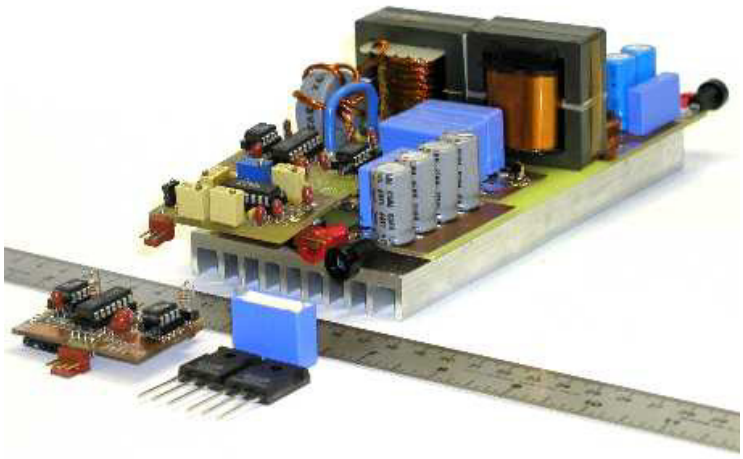
As demonstrated to Chapter 4, LLC resonant converter could achieve higher efficiency at higher switching frequency comparing with AHB converter. IPEM approach can also be implemented into this advanced circuit topology. By using Active and Passive IPEMs, 1.8 times power density improvement can be realized for 400 kHz LLC resonant converter. For 1 MHz switching frequency LLC converter, 1.4 time power density improvement can be realized. While the power density benefits have diminishing frequency with increasing switching frequency, switching loss reduction effects get more pronounced at higher switching frequency.

Furthermore, IPEM concept can be extended to the whole front-end converter. Similar to DC/DC stage, using Active IPEM in PFC stage can also reduce switching loss and switching device voltage stress. Besides, technology of integrating inductors and capacitors can also be implemented in the integration EMI filter (Filter IPEM). In this way, whole front-end can be built with several modules, design and manufacturing costs are greatly reduced. Prospects of power integration are demonstrated through an integrated front-end converter and further potentials are discussed.

5.2 Power Converter Improvement through Power Integration

Power converters in day are mostly custom designed and using discrete devices, as demonstrated in Figure 5-1. Different discrete devices are connected together though the copper traces on mother board. Because of different form factors, compact design is difficult to be realized. Thus, large parasitics are generated because of interconnections. These large parasitics begin to show the detrimental effects on circuit performance, especially on the switching loss and voltage stress on switching devices. Besides, with the development of power conversion technology, high density and low profile become the basic requirement for front-end converters. The high profile devices, such as the inductor and transformer prevent the designed DC/DC converter shown in Figure 5-1 to achieve 1U profile. Thus, low profile planar design is required.

Furthermore, large passive components and complex interconnections make it desirable to integrated different passive component together into a single module.



Power density: 12W/in^3
Baseline
1×

Figure 5-1. 200 kHz asymmetrical half bridge with discrete devices.

According the circuit diagram shown in Figure 5-2, switching commutation loop, including primary side half bridge and decoupling capacitor, is critical for circuit switching performance. Therefore, it is desirable to minimize the parasitic inductor associated with the loop. In the converter with discrete devices, decoupling capacitor is normally put close to switches to minimize the loop. However, through integration of device with their gate drivers, less parasitics, higher power density and better performance power converter could be realized. Besides, passive components can also be integrated together to simplify circuit interconnection and realize higher power density.

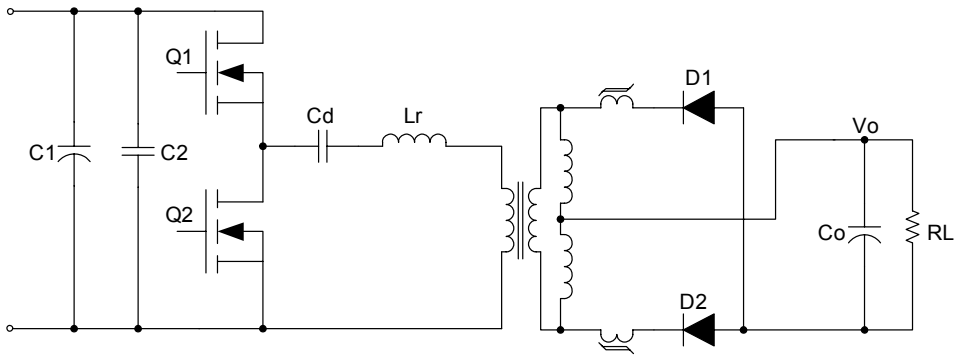
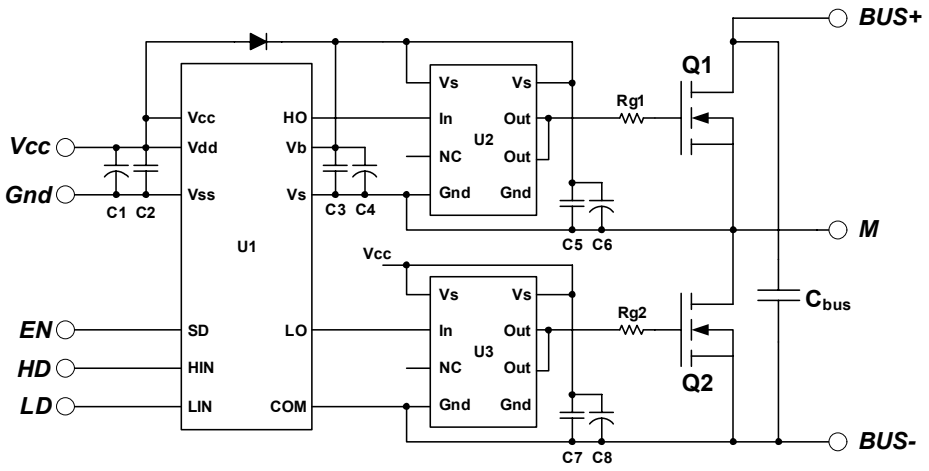


Figure 5-2. Circuit diagram of AHB converter.

5.2.1 Active integration (Active IPEM)

In AHB converter, active integration includes primary side half bridge MOSFETs, gate drivers and decoupling capacitor. MOSFETs use bare dies with part number IXTH24N50 from IXYS. Gate driver circuit uses two-stage structure. In first stage, bootstrap driver IC IR2113 from International Rectifier is used to transfer gate signals, as well as generate the energy source for driving the top switch. Using MIC4420 from Micrel as second stage driver can realize stronger driver capability to ensure smaller switching loss. Furthermore, to reduce the driver circuit size and fit it inside Active IPEM, thick film technology together with IC bare dies are used. Driver circuit size can be limited to 800mil×315mil. Schematic for system IPEM DC/DC part is shown in Figure 5-3. Same as PFC stage, a 0.56uF decoupling capacitor is also integrated into DC/DC part to reduce the circuit parasitics.



Q1, Q2: IXDH21N50

C_{bus}: 0.4uF/600V surface mount ceramic capacitor

D1: MURS160

C1, C4, C6, C8: 0.1uF/25V

Rg1, Rg2: 5.1Ω

U1: IR2113

U2, U3: MIC4420

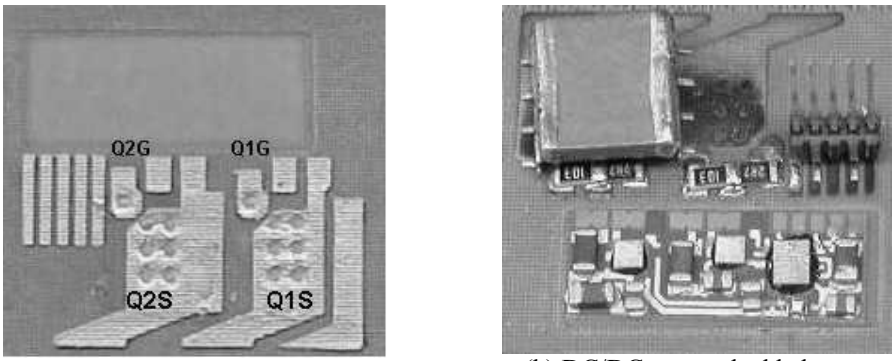
C2, C3, C5, C7: 5.1Ω

Figure 5-3. DC/DC Active IPEM.

To integrate these components into one compact module, different packaging technology can be used. For most discrete devices, wire bonding is the standard packaging technology. However, due to large parasitic caused by bonding wires, new packaging technology with less parasitics is desirable. Therefore, embedded power technology is used to construct the Active IPEM. Because laminated bus structure, embedded power technology could achieve less parasitics caused by interconnections. Moreover, 3 dimensional (3D) integration capability of embedded power technology allows higher density integration. Furthermore, because of the planar structure, double side cooling is possible, which can dramatically enhance the thermal management for switching devices [E-5][E-6].

The manufacture processes of Active IPEM can be illustrated in Figure 5-4. Firstly, two openings are formed in a ceramic plate, for embedding the bare dies

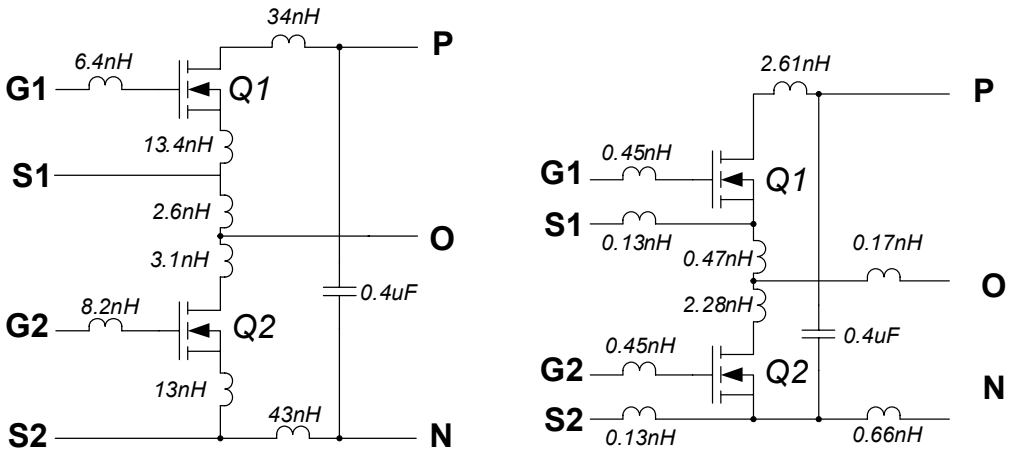
of MOSFETs. After applying the insulation layer, metallization layer is deposited on the top side and etched as designed pattern, which forms the interconnections for switching devices, as well as the traces for the connections of gate drive circuit, bus capacitor and input connectors, as shown in Figure 5-4 (a). On the backside, MOSFETs drains are directly exposed for soldering on to substrate. This ceramic frame-based stage can achieve a small size as $28.45\times27.32mm^2$. After manufacturing of switching stage, the associated gate drivers and decoupling capacitor components are mounted onto the top metallization to finish the embedded power stage.



(a) Metallization patterns on top (b) DC/DC part embedded stage

Figure 5-4. Fabrication of DC/DC integrated multi-chip stage.

After the Active IPEM is manufactured, Maxwell Q3D parasitic extraction tool is used to estimate the parasitic inductance and compared with discrete devices.

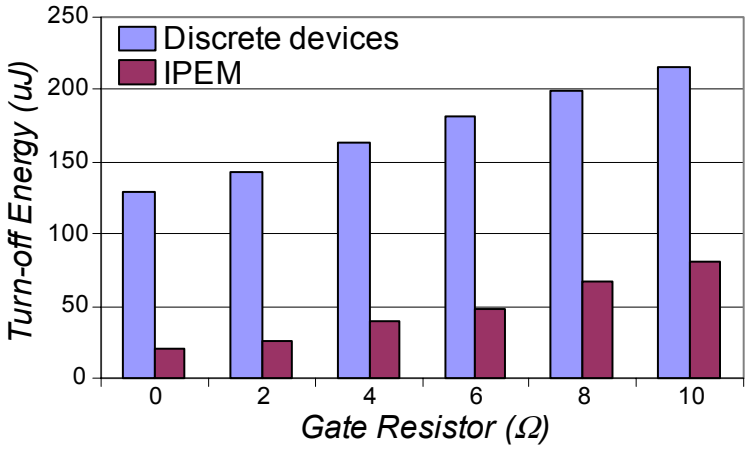


(a) Discrete devices (b) Active IPEM

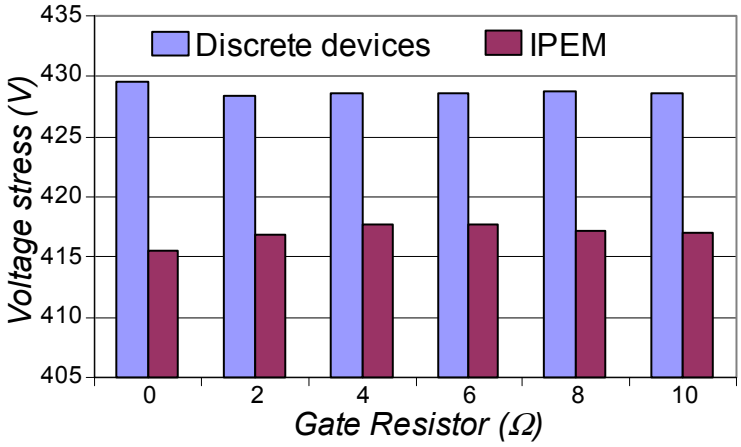
Figure 5-5. Switching stage parasitics.

As shown in Figure 5-5, the parasitic is much reduced comparing with discrete devices and especially the inductance that shares both the driving loop and switching commutating loop, which is critical for the switching loss [E-6][E-7][E-8][E-9]. Since for the IPEM case, the driver loop and power loop don't share the same trace, this parasitic is minimized, a better performance is expected. At the same time, the lower commuting path inductance will cause less voltage stress on the MOSFETs.

Switching performances of the discrete devices and Active IPEM are simulated with different gate resistors. From the simulation results as shown in Figure 5-21, both the voltage stress and the switching loss are much reduced.



(a) Turn-off energy



(b) Voltage stress

Figure 5-6. Switching performance comparison for different gate resistors.

Active IPEM is then tested with a simple chopper circuit to verify the switching performance improvement. Switching waveforms using discrete devices and IPEM are shown in Figure 5-7 and Figure 5-8, respectively. From the test results, it can be clearly seen that for same 10A turn-off current, discrete approach has a 74V voltage overshoot, but the IPEM approach only has 40V overshoot. Moreover, the inductor current waveform is much cleaner comparing with discrete approach, which means less EMI noise.

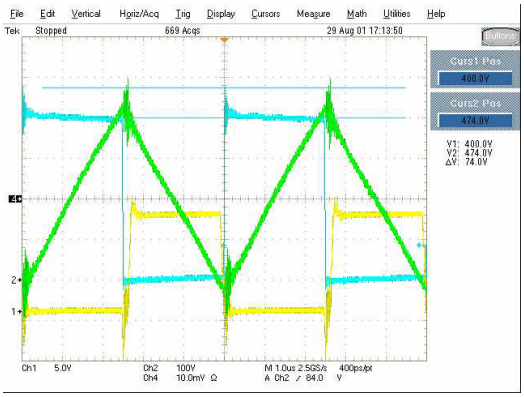


Figure 5-7. Discrete device test waveform.

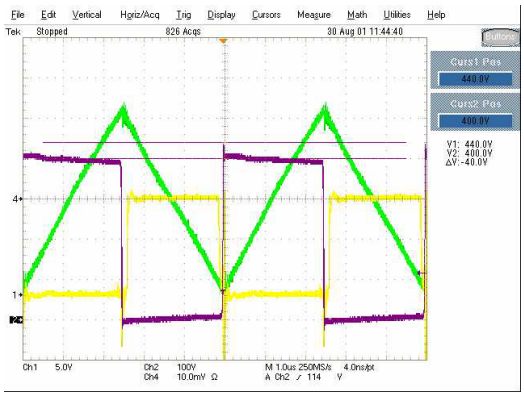
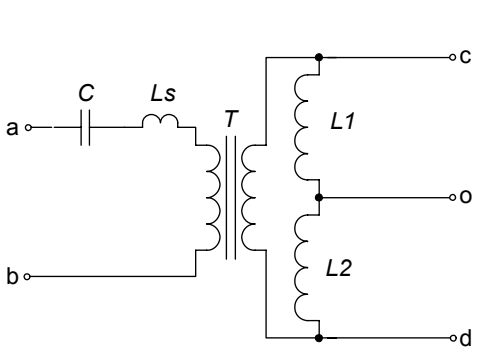


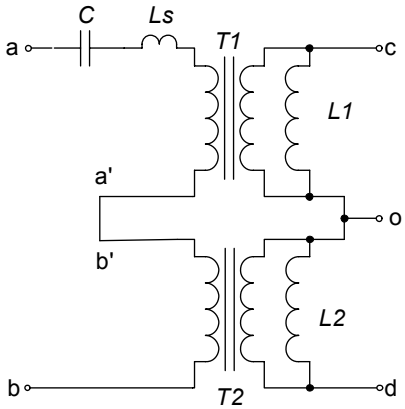
Figure 5-8. IPEM measurement results.

5.2.2 Passive Integration

Besides the active integration, IPEM concept can also be extended into passive components integration [E-10][E-11]. Passive IPEM for the AHB converter includes primary side DC blocking capacitor, resonant inductor, transformer and secondary side current doubler inductors. The schematic for the Passive IPEM is shown in Figure 5-9 (a). Because of current doubler configuration, to simplify manufacturing process, Passive IPEM is constructed by two transformers stacking together, as shown in Figure 5-9 (b). The current doubler inductors can be implemented using transformer magnetizing inductors.



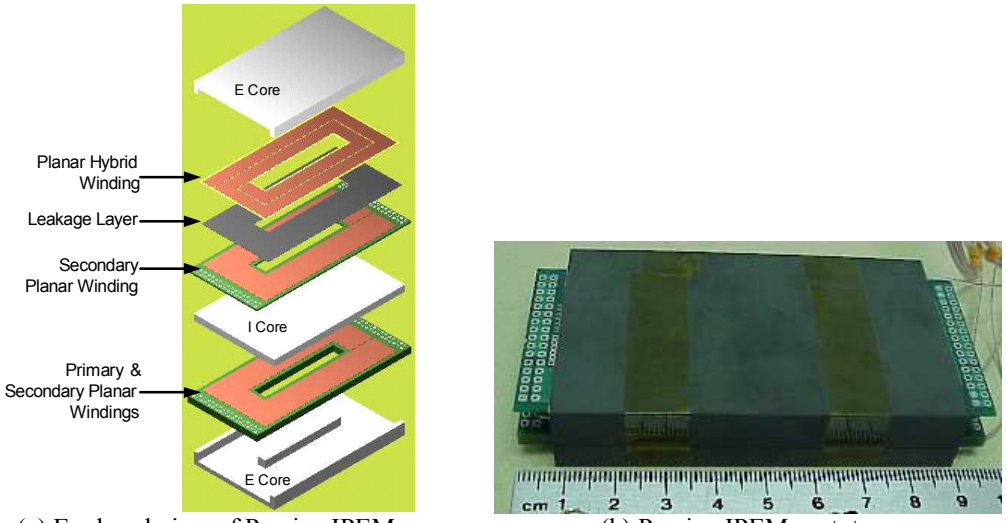
(a) Schematic for Passive IPEM



(b) IPEM implementation

Figure 5-9. Passive IPEM for Asymmetrical Half Bridge.

The transformers are built with two planar E-cores that share a common I-core, as detailed in Figure 5-10 (a). The DC blocking capacitor is implemented in only transformer T_1 using the hybrid winding technology. This technology is implemented using copper traces on both sides of a dielectric layer to create the desired DC blocking capacitor by employing the winding parasitic capacitor.



(a) Explored view of Passive IPEM (b) Passive IPEM prototype

Figure 5-10. Prototype of Passive IPEM.

Moreover, in transformer T_1, a layer of low permeability (μ_r=12) material is inserted between primary and secondary windings. Therefore, leakage flux between transformer primary and secondary windings can be great increased, which results in a large leakage inductance. By adjusting the thickness of inserted material, desired leakage inductance can be achieved. Besides, transformer T2 is a conventional planar low-profile transformer, with controlled magnetizing inductance as a current doubler inductor. Figure 5-10 (b) shows a picture of the final Passive IPEM implemented for the AHBC.

The manufactured Passive IPEM is then measured and characterized to compare with discrete approaches. Comparing with the discrete devices, transformer turns-ratio changes from 8:3 to 4:3. Since two transformers are series together to achieve the same transformer turns-ratio, Passive IPEM turns ratio is half of the discrete transformer. To achieve the proper circuit operation, circuit parameters should be the same. From the data summarized in Table 5-1, Passive IPEM can well achieve the desired parameters as in the discrete devices.

Table 5-1. Parameters comparison between discrete device and Passive IPEM.

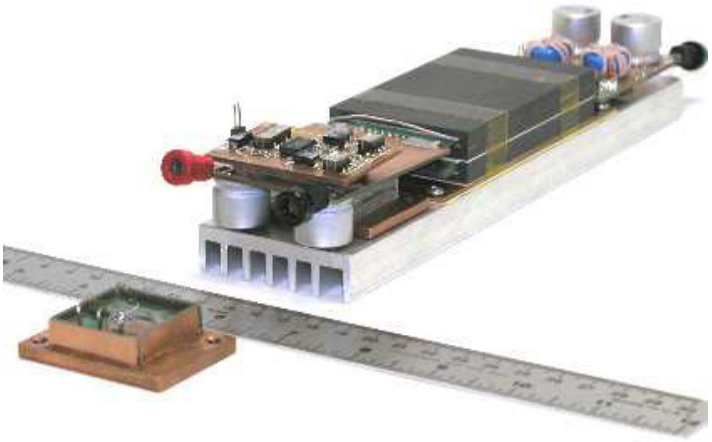
Parameters	Discrete	IPEM
Turns ration of transformer	8:3	4:3
Filter inductance (μH)	85	N/A
Magnetizing inductance of T1 (μH)	N/A	43.8
Magnetizing inductance of T2 (μH)	N/A	44.0
Resonant inductance (μH)	2.0	1.8
DC blocking capacitance (μF)	2.04	2.5
Profile (cm)	4.4	1.6
No. of passive components	6	1
No. of terminals	15	5
Total volume (cm3)	343	87

Besides achieving same performance of discrete devices, Passive IPEM can reduce the components size from 343cm^3 to 82cm^3, which means more than 75% size reduction. Furthermore, components number reduces from 6 to 1. Therefore, the total interconnections for the passive part can be reduced from 15 to 5. Thus,

by using Passive IPEM, power density can be greatly increased. Fewer interconnections make the circuit easier manufacturing.

5.2.3 Integrated DC/DC converter

After manufacturing Active and Passive IPEMs, they are put inside a 200 kHz, 1 kW, and 48V output AHB converter to demonstrate the benefits of using IPEM concept. Comparing with the discrete version shown in Figure 5-1, instead of using large amount of discrete devices, converter is simplified as putting several power modules together, which means easier design and manufacturing [E-12][E-13].



Power density: 34W/in^3
3×Baseline

Figure 5-11. 200 kHz asymmetrical half bridge with IPEMs.

Another change is the high profile magnetics are changed into low profile Passive IPEM. Thus, IPEM based AHB could easily fit in 1U profile enclosure. Moreover, power density of IPEM-based AHB converter is 34W/in^3. Comparing with 12W/in^3 power density for discrete version, three time power density improvement is achieved. Beside, due to less switching loop parasitics, less

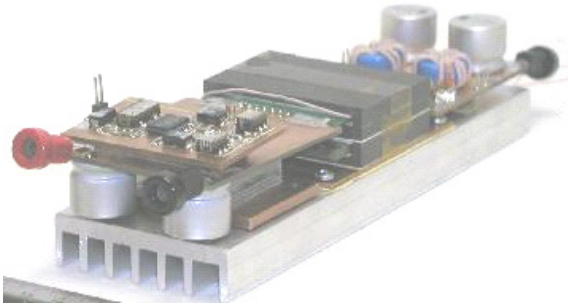
voltage stress is observed on MOSFETs, which means higher reliability for switching devices.

From the theoretical analysis, benefits of using Active IPEM also include the switching loss reduction. Because switching loss couldn't be directly measured in real circuit, only converter efficiency can be measured and compared. Although using IPEM concept AHB power density can be largely improved, large switching loss prevents the topology operating at higher switching frequency and shrinking the passive components sizes. To further improve converter power density and meets the continuous increasing power density requirement, better circuit topology needs to be used. Instead of using AHB converter, LLC resonant converter could operate at 400 kHz while maintain much higher efficiency. As shown in Figure 5-12, for 1 kW power level and 48V output, LLC resonant converter could achieve 44W/in^3 power density, with discrete devices. Thus, topology along could improve power density by 3.7 times, comparing with AHB converter with discrete devices.

Power density: 44W/in^3
3.7×Baseline

Figure 5-12. 400 kHz LLC resonant converter with discrete devices.

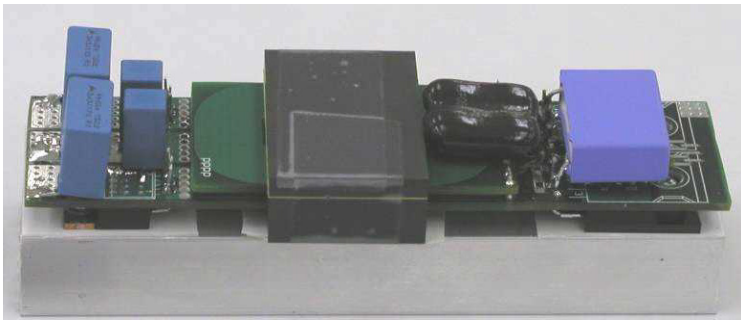
IPEM concept could also be implemented in LLC resonant converter. As demonstrated in Figure 5-13, IPEM-based converter could achieve 80W/in^3 power density. Comparing with its corresponding discrete version, 1.8 times power density improvement can be realized. Similar to AHB converter, due to the reduction of parasitics, switching loss and voltage stress reduction can be achieved. For LLC resonant converter, because high power density could be achieved with discrete devices, less power density improvement is achieved because of using IPEM.



Power density: 80W/in^3
6.7×Baseline

Figure 5-13. IPEM-based 400 kHz LLC resonant converter.

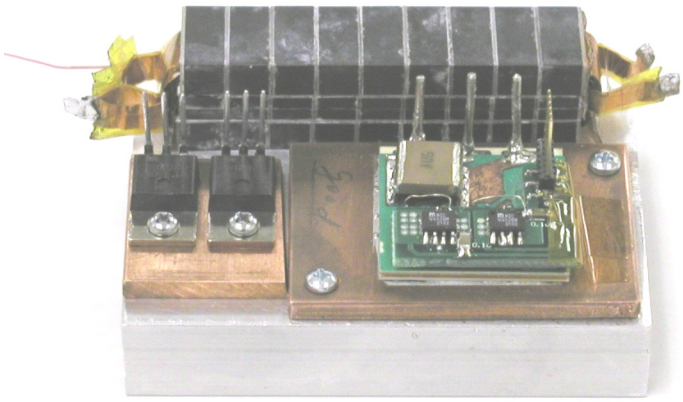
Furthermore, from the discussion in Chapter 3, , LLC resonant converter can operate at 1 MHz switching frequency while maintaining high efficiency, as demonstrated in Figure 5-14. Therefore, the power density of LLC resonant converter using discrete devices could achieve 76W/in^3 power density, at 1 MHz switching frequency. Comparing with 200 kHz AHB with discrete devices, more than 6 times power density improvement can be achieved.



Power density: 76W/in^3
6.3×Baseline

Figure 5-14. 1MHz LLC resonant converter with discrete devices.

By using the IPEM concept, power density can be further improved. Furthermore, because less parasitics, circuit switching performance is expected to be improved. The designed 1 MHz LLC resonant converter with Active and Passive IPEM is shown in Figure 5-15. Because of this ultra high switching frequency, gate driver circuit used in 200 kHz AHB can't be used because of higher driving loss and higher driving capability requirement. Therefore, new gate driver with stronger driving capability was designed. With MIC4452 MOSFET driver from Micrel, 12A peak driving current can be achieved to ensure fast switching speed and less switching loss. Moreover, to fit inside the IPEM, only the final driving stage is integrated inside the IPEM. While for the Passive IPEM, heat extractors are used to improve its thermal management. With the designed integrated 1 MHz LLC resonant converter 110W/in^3 power density can be achieved. Comparing with its corresponding discrete version, 1.5 times power density improvement can be realized [E-15][E-16][E-17][E-18].



Power density: 110W/in^3
9.2×Baseline

Figure 5-15. 1 MHz LLC resonant converter with IPEMs.

From IPEM implementation in LLC resonant converters, it can be observed that the power density improvement benefits are getting less with higher switching frequency. Because at higher switching frequency, passive components sizes are small, by integrating these devices together, less size reduction is achieved.

This diminishing return shows that size reduction effects could be even less when the switching frequency keeps increasing. However, at higher switching frequency, switching loss becomes more sever. Thus, benefits of switching loss reduction becomes more pronounced, which means IPEM approach becomes even more desirable at higher switching frequency.

5.3 Prospects of power integration

With the demonstration of DC/DC converter, higher power density, better performance can be achieved by using IPEMs. Therefore, IPEM concept should

be extended to the whole front-end AC/DC converter and maximize the benefits [E-19][E-20].

A typical front-end converter using discrete devices is shown in Figure 5-16. It can only achieve 7.5W/in^3.

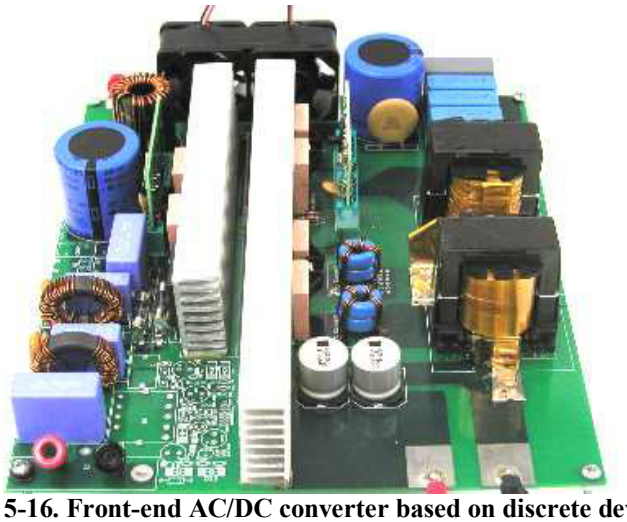


Figure 5-16. Front-end AC/DC converter based on discrete devices.

Its circuit diagram is shown in Figure 5-17. For PFC stage, 400 kHz switching frequency single switch PFC is used to achieve smaller Boost inductor and EMI filter size. For DC/DC stage, AHB topology is employed with 200 kHz switching frequency.

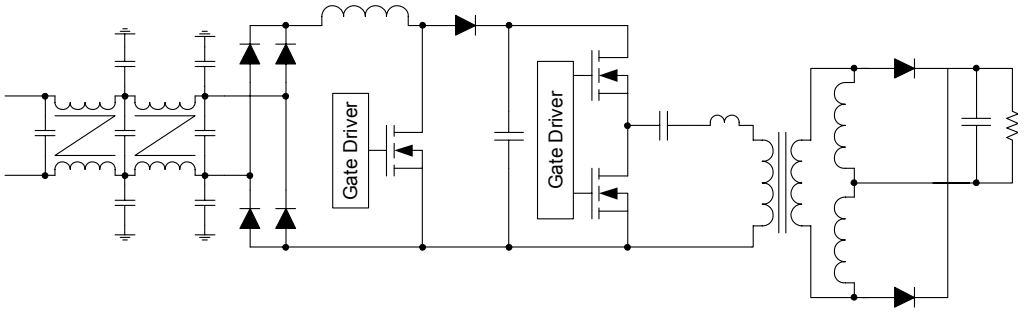


Figure 5-17. Schematic of front-end converter benchmark.

According to the circuit schematics, Active IPEM integrates all the switching devices together with their driving circuits. Same packaging techniques can be used for both PFC stage and DC/DC stage to simplify the manufacturing. Moreover, by combine PFC and DC/DC stage together, component number can be further reduced and it is easier for system layout.

For PFC stage, MOSFETs, diodes, and gate drivers are integrated in PFC part of system IPEM. To ensure smaller conduction loss, two20A 600V CoolMOS^{TM} with part number SPW20N60C3 are parallel together. Two 6A 600V SiC diodes with part number SDP06S60 are in parallel. The gate driver circuit is also integrated together with the active devices to minimize gate driver loop inductance. Gate driver uses commercial driver chip MIC4452, 12A non-invert driver with SO-8 packaging. And the gate resistor uses 3Ω for each MOSFET. To further decrease the parasitic, a ceramic decoupling capacitor is integrated just on top of those devices. The capacitor is 0.56uF with 500V rating. The schematic for system IPEM PFC stage is shown in Figure 5-18.

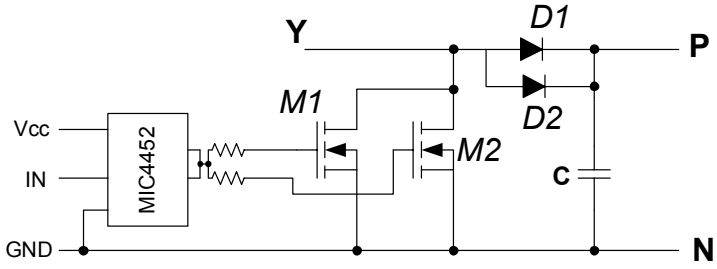
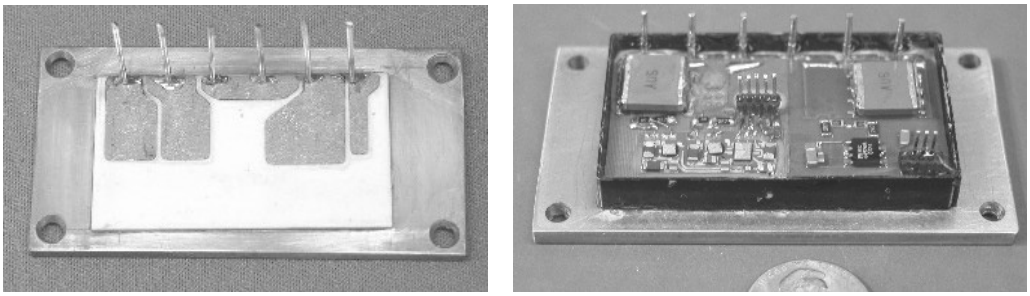


Figure 5-18. System IPEM PFC part.

With the same manufacturing process of DC/DC Active IPEM, Active IPEM for PFC stage is built. Together with DC/DC part, system IPEM is built by

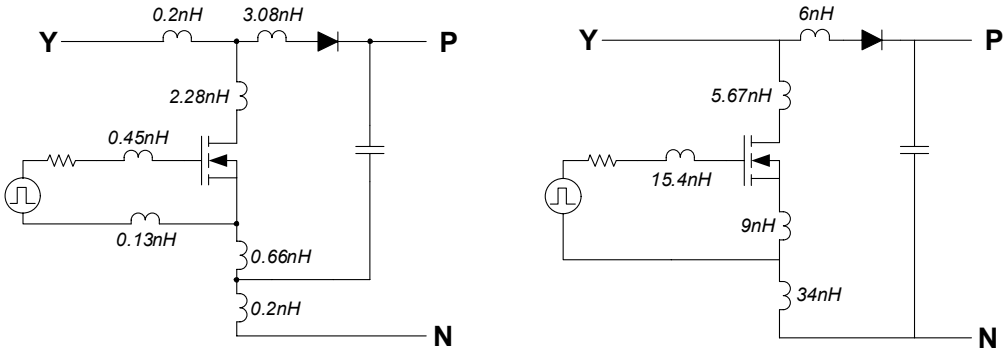
soldering these embedded power stage on the DBC substrate, as shown in Figure 5-19. Al_2O_3 DBC substrate of 28.45×50.44mm^2 is patterned on the topside, as shown in Figure 5-19 (a). The power terminals are used to realize the interconnection between the substrate and embedded power stage, as well as the I/O terminals of the Active IPEM. Figure 5-19 (b) shows the manufactured system Active IPEM. A large piece heat spreader is used for evenly thermal distribution and mechanical support for the module.



(a) Substrate (b) System IPEM

Figure 5-19. IPEM assembly from the integrated chip stages.

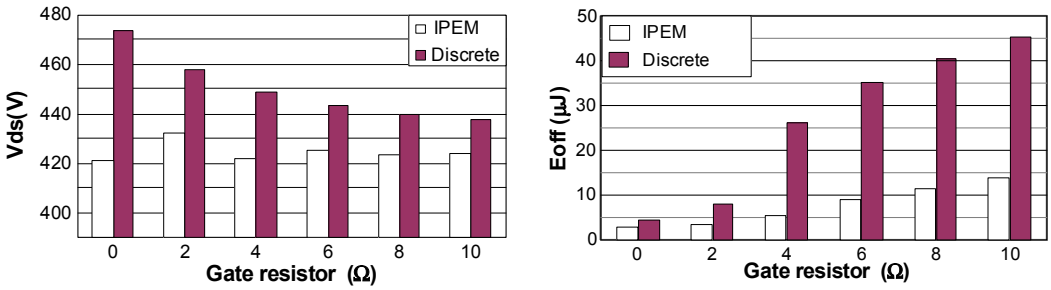
PFC part of system IPEM is then modeled by using Maxwell Q3D parasitic extraction tool and compared with discrete approach. Parasitic inductances comparison is demonstrated in Figure 5-20. Large parasitic inductance reduction can be observed.



(a) IPEM (b) Discrete devices

Figure 5-20. Parasitic comparison between PFC IPEM and discrete devices.

Switching performances of the discrete devices and Active IPEM are simulated with different gate resistors, to estimate the parasitic inductance impacts. From simulation results shown in Figure 5-21, both voltage stress and switching loss are much reduced. Based on the simulation results, for 400 kHz single switch PFC, together with 3Ω gate resistor, 6W switching loss reduction is expected by using Active IPEM.

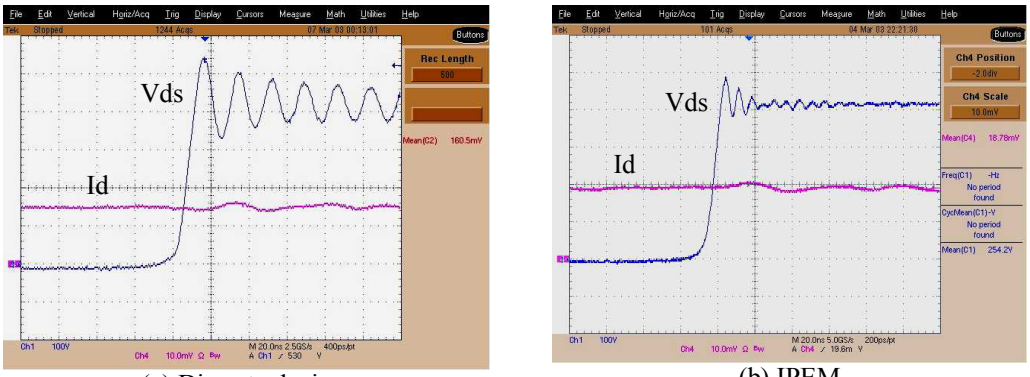


(a) (b)

Figure 5-21. (a) Voltage overshoot comparison based on simulation; (b) Turn off loss comparison based on simulation.

The discrete devices and Active IPEM are then tested using a simple Boost DC/DC converter. Because of the compact packaging of Active IPEM, it is difficult to measure the switching loss. Thus, only MOSFET voltage stress is compared. The measured switching waveforms are shown in Figure 5-22 . For the

discrete devices, when the MOSFET turns off 7A current, the voltage overshoot is 106V and the ringing frequency is 52MHz. But for the IPEM, when the MOSFET even turns off 10A current, the voltage overshoot is only 73V and the ringing frequency is 153MHz. A higher resonant frequency demonstrates the smaller parasitic inductance by using IPEM. Furthermore, because of large voltage stress reduction, higher reliability can be achieved by using IPEM approach. On the other hand, keeping the same voltage stress, IPEM approach can use even faster gate driving speed. Therefore the switching loss can be further improved, so does the converter efficiency.



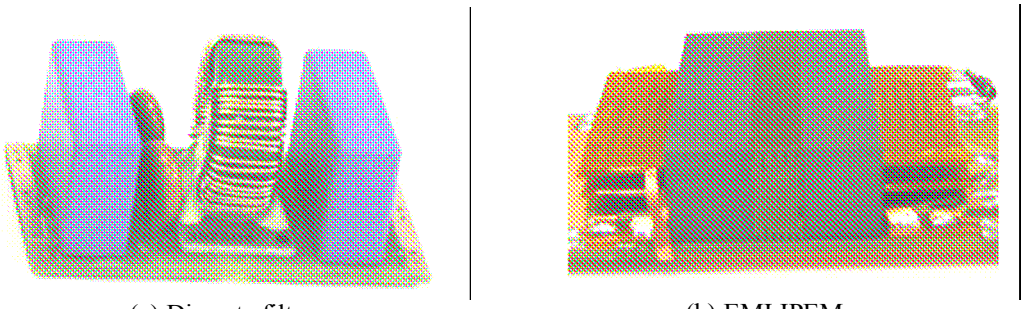
(a) Discrete devices (b) IPEM

Figure 5-22. MOSFET drain to source voltage during turn off 100V/div, 5A/div, 20nS/div.

Same Passive IPEM integrating inductors, transformer and DC blocking capacitor is built for the integrated system. At the same time, from the schematic shown in Figure 5-17, input EMI filter is constructed by inductors and capacitors, which means same technology used for Passive IPEM can be employed to build the integrated EMI filter (EMI IPEM). For discrete EMI filters, different form factors make it difficult to optimally utilize the space. Besides, due to undesired parasitic components, such as equivalent parallel capacitor (EPC) for inductor and

equivalent series inductor (ESL) for capacitor, filter attenuation reduces dramatically at high frequency range. Furthermore, different components in discrete EMI filter use different materials and manufacturing process. Thus, production cost is high.

By utilizing the hybrid winding technology used in Passive IPEM, integrated EMI filter can be designed. In EMI IPEM, EPC could be minimized through different winding structure designs. Meanwhile, ESL of integrated capacitors can be reduced by using the transmission line connection method. Thus, better EMI filter performance can be achieved by using EMI IPEM. Furthermore, because of using planar structure, low profile, high density EMI filter module can be realized. As shown in Figure 5-23, EMI filter IPEM can achieve 50% size reduction and better performance.



(a) Discrete filter (b) EMI IPEM

Figure 5-23. EMI filter.

After Active and Passive IPEMs are manufactured, they are implemented into a front-end AC/DC converter to evaluate the effectiveness of achieving higher performance and power density. Meanwhile, a front-end converter using identical topologies and switching frequencies is manufactured and set as the benchmark.

The design front-end AC/DC converter works with single phase AC input, with universal input. The maximum output power is 1kW, with 48V DC output. Because the PFC stage efficiency decreases with the decreasing of input AC line, to ensure thermal handling capability, the converter is designed to derate its output power to 600W when the input voltage is less than 150V. The final prototypes of discrete version and IPEM version of front-end AC/DC converters are shown in Figure 5-24 and Figure 5-25.

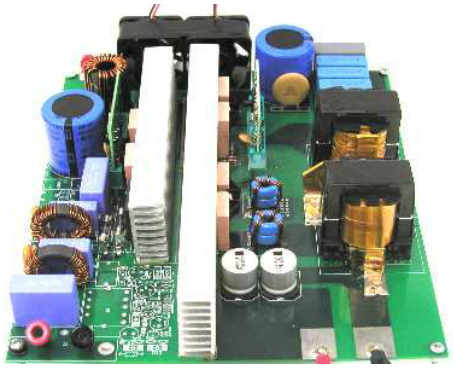
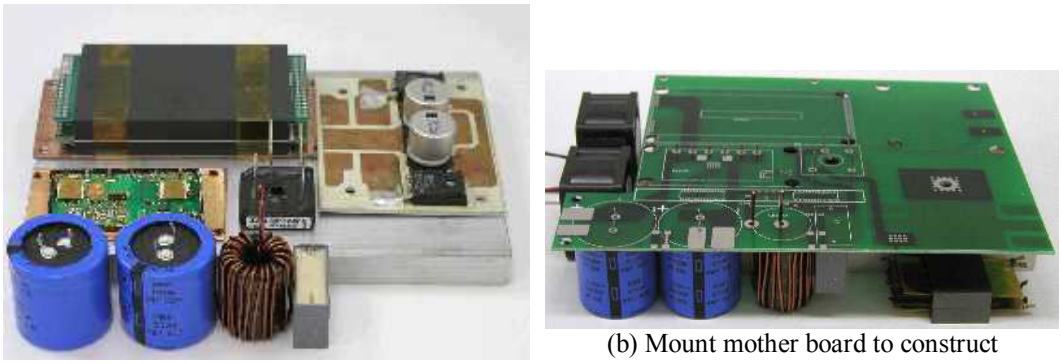


Figure 5-24. Discrete version of front-end AC/DC converter.

Figure 5-25. IPEM-based front-end AC/DC converter.

Comparing with discrete version, the IPEM version has much less components number. Using Active and Passive IPEM, by adding several associated capacitors, inductor and output rectifiers, the system can be constructed as putting several building blocks together, which makes the system easier manufacturing and much cost effective comparing with discrete version. Moreover, due to the modular approach, automatic manufacturing becomes possible. For the discrete-based converter, all the components are mounted on top of the mother board, including the heat-sinks. However, for the IPEM version,

due to the interconnect structures of Active and Passive IPEMs, the components are mounted beneath the motherboard, as illustrated in Figure 5-26.



(a) Step 1, mount components on heat-sink

(b) Mount mother board to construct interconnection

Figure 5-26. Assembly of IPEM-based front-end AC/DC converter.

Firstly, low profile devices, including Active and Passive IPEMs, Diode Bridge and output rectifier and filter are mounted on the heat-sink. Instead of using vertical mounting heat-sink, the horizontal mounting heat-sink fully utilizes the profile of whole converter and ensures good thermal conductivity. To keep the low profile of whole converter, high profile components, such as the Boost inductor, holdup time capacitor and EMI filters are not mounted on the heat-sink. By mounting the mother board on top of these components, interconnections are achieved through the traces on the mother board. As analysis on previous sections, due to the decoupling capacitor inside Active IPEM, the bus capacitors are no longer required to be close to the switching devices to ensure small voltage stress. In this way, the circuit layout could be much easier comparing with discrete approach.

One important measurement of IPEM effectiveness is the power density improvement. For both the converters, to meet the 1U profile requirement, all the components profiles have to be smaller than 1.75". However, do the large transformer and inductor size, discrete version can't meet 1U profile requirement and has a 1.5U profile, which results in a 7.5W/in^3 power density. Meanwhile, because of low profile Active and Passive IPEMs, the IPEM version converter can easily meet U profile requirement, and achieve 11.7W/in^3 power density. Thus, 56% power density improvement has been achieved by replacing the discrete devices with IPEMs.

After the converters are manufactured, they are powered with different input and output condition. Although IPEM approach can easily achieve higher power density and easier manufacturing, it is important to evaluate the total loss of the converter, which is ultimately key factor for converter power density.

Firstly, the PFC stage efficiency is compared for two different approaches, as shown in Figure 5-27. Measured efficiency demonstrated the capability of increasing converter efficiency by using IPEM approach. From 150V to 250V, the maximum efficiency improvement can be achieved is more than 1%. Because circuit topology, switching frequency, semiconductor devices are identical for two cases, the main reason for efficiency improvement comes from the parasitic inductance reduction. Based on the simulation results summarized in Figure 5-21 (b), 15uJ switching loss energy can be saved by using IPEM, which can be

translated in to 6W loss reduction when the switching frequency is 400 kHz. Thus, both the simulation results and experimental results verified the benefits of using IPEM.

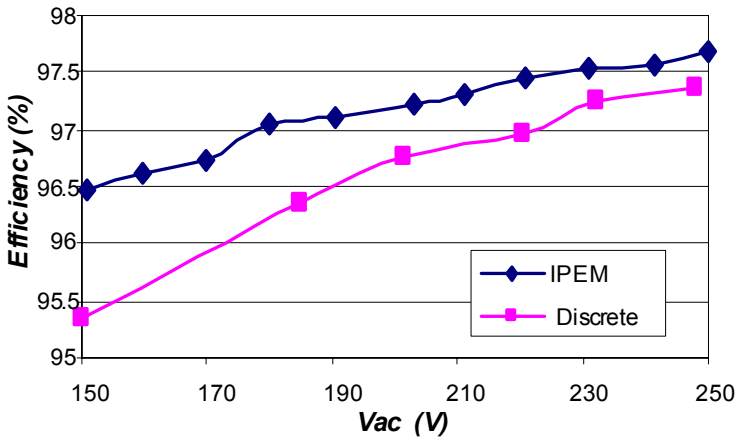


Figure 5-27. PFC stage efficiency comparison.

Furthermore, the system efficiency is compared at whole input voltage range with corresponding maximum output power. The experimental results are shown in Figure 5-28.

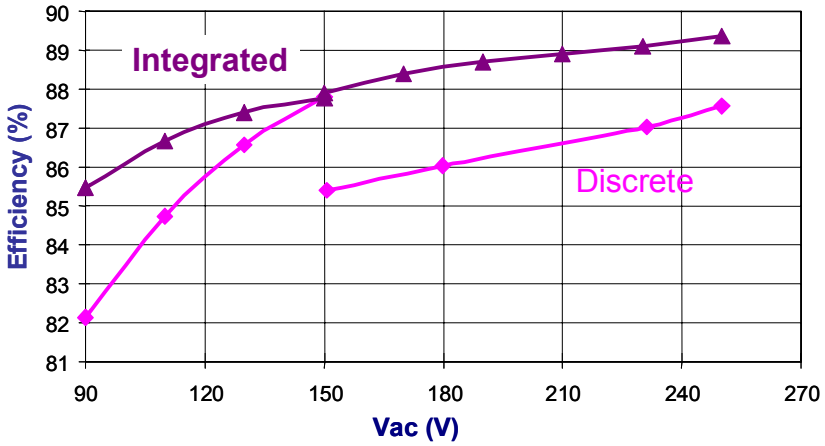


Figure 5-28. Efficiency comparison between two converters.

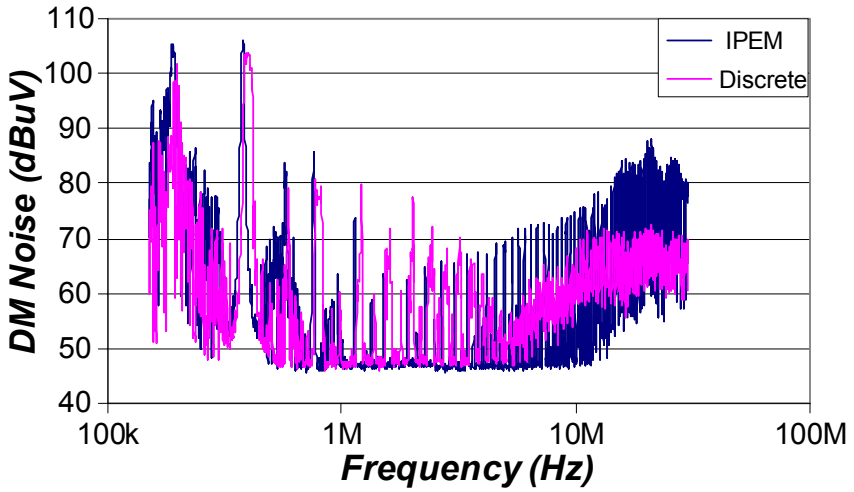
When the input voltage is higher than 150V, IPEM approach can achieve around 2 to 2.5 percent efficiency improvement. In this case, the converters

output 1kW power. However, when the input voltage is less than 150V, converter output power is derated to 600W. In this case, 3% efficiency improvement can be achieved by using IPEM at 90V input voltage. When input voltage increase to 150V, IPEM approach and discrete approach reach similar efficiency. From the simulation on Active IPEM, for both PFC part and DC/DC part, efficiency improvement can be achieved. However, due to the existence of Passive IPEM, the efficiency improvement is offset by the passive IPEM. .

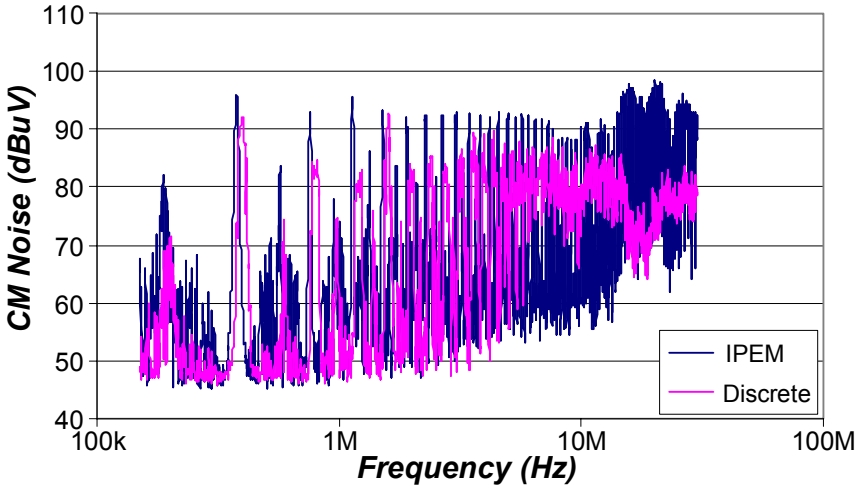
Besides the efficiency improvement, using IPEM can also reduce the voltage stress on the switching devices. The voltage stress reduction has been demonstrated in the device level. Moreover, for discrete device version, the layout of bus capacitors is critical for device voltage stresses. Because the layout can largely change the parasitic inductance in the circuit, it is important to layout the bus capacitors as close as possible to switching devices. However, for the IPEM implementations, because of the integrated decoupling capacitor, loop inductances are already minimized in the device level. Thus, the layout of bus capacitors is no longer critical for circuit performance. Therefore, circuit layout can be much simplified without sacrificing the performance.

After that, EMI performances of two converters are compared. The experimental results are shown in Figure 5-29. The IPEM approach has worse EMI noise performance comparing with discrete version. This is mainly caused by different layout of the converters. In discrete version, heat-sinks are using two

pieces of long extrusion type. However, in IPEM version, a big flat heat-sink is used to simplify the components mounting. Thus much larger parasitic capacitance exists between the heat-sink and earth ground comparing with the discrete version, which causes higher CM noise level. Thus, higher CM noise can be observed in the IPEM version.



(a) Differential mode noise comparison



(b) Common mode noise comparison

Figure 5-29. EMI performance comparison between two converters.

For IPEM-based system, due to low profiles of Active IPEM and Passive IPEMs, the footprints of these devices are larger comparing with discrete devices.

Therefore, to fully utilize the 1U profile, IPEMs are mounted on a whole piece of heat sink. The fins are on the bottom side of heat-sink. In this way, efficient air flow path is generated by the fins and the converter case. To evaluate the thermal performance of the converter, temperatures of different locations in the converter have been measured through thermal couplers, under 150V AC 1kW output condition. The experimental results are summarized in Figure 5-30. At 150V AC input, 48V output and 1kW load condition, after about 15 minutes, the temperatures at different locations reach steady state value.

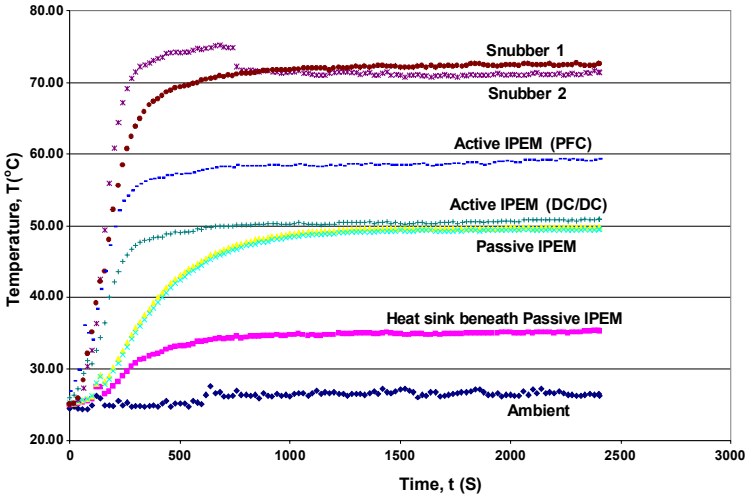


Figure 5-30 Thermal Measurement results

From the experimental results, the highest temperatures are on the secondary side saturable inductor, which is predicted by the thermal simulation. Meanwhile, the PFC part and DC/DC part of the IPEM have temperatures of 59°C and 51°C, respective. Comparing with 26°C ambient temperature, less than 35°C temperature rise is achieved. Therefore, at 50°C ambient temperature, the highest temperature in Active IPEM is only 84°C. Plenty design margin has been

achieved. As for the Passive IPEM, the highest temperature is less than 50°C. Because Passive IPEM has large footprint and mounted on heat-sink, good thermal transfer capability has been achieve, which results in low thermal stress.

Similar to DC/DC converter, IPEM-based system could also be implemented with better topologies. With LLC resonant converter, power density of DC/DC stage can be largely improved. Using 400 kHz PFC and 400 kHz LLC resonant converter, together with Active, Passive and EMI IPEMs, 14.6W/in^3 power density is expected, as shown in Figure 5-31. Moreover, because of the reduction of switching loss, 1~1.5% efficiency improvement is expected. Because LLC resonant converter has much less switching loss, less efficiency improvement is expected comparing with using AHB topology.

Figure 5-31. IPEM-based front-end converter with 400 kHz PFC and 400 kHz LLC.

When switching frequency of LLC resonant converter increases to 1 MHz, power density of the front-end converter could reach around 25W/in^3. Besides,

because of the increasing switching frequency, benefits of using Active IPEM could become more pronounced. Thus, around 2% efficiency improvement might be accomplished by replacing discrete devices with IPEMs.

5.4 Summary

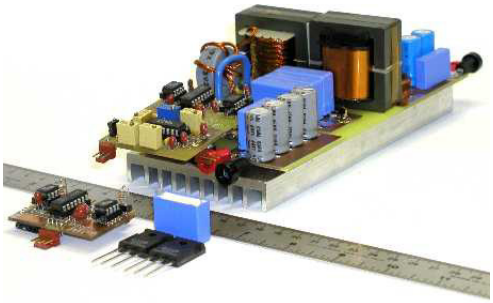
With the development of high switching frequency technology, front-end AC/DC converter power density can be largely increased. However, detrimental effects of circuit parasitic components become more pronounced when the switching frequency is higher. Therefore, the circuit parasitic components are desired to be small when circuit is operating at very high switching frequencies.

Besides the pressure of higher power density, front-end AC/DC converter is also under the pressure of lower cost. For today's power supply industry, customized design and lack of standardization cause high manufacturing cost and difficult to implement automatic manufacturing.

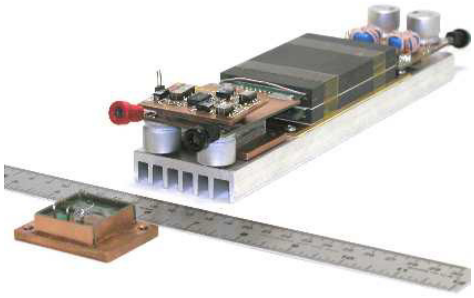
To address these issues, Integrated Power Electronics Modules (IPEMs) concept was proposed. According to the functions and properties of different components, front-end AC/DC converter system is partitioned into Active, Passive and EMI IPEMs. In this way, whole system could be easily manufactured by putting different modules together, which results easier manufacturing and less cost. Furthermore, with integrated solution, both switching loss and voltage stress

on the switching devices can be reduced, which results in higher efficiency and higher reliability.

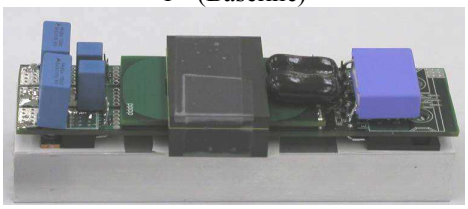
With the demonstrations in DC/DC converters, IPEM could be simplify the converter construction and dramatically improve power density. Its effectiveness is summarized in Figure 5-32, by using IPEMs together with 1 MHz LLC resonant converter, power density of DC/DC converter can be improved by 9 times from the base line of 200 kHz AHB with discrete devices.



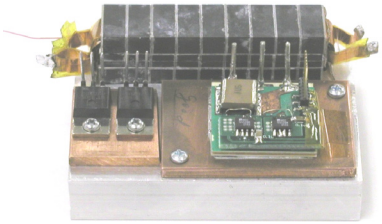
(a) 200 kHz AHB, Discrete devices
Power density: 12W/in^3
1× (Baseline)



(b) 200 kHz AHB, IPEM-based
Power density: 34W/in^3
3× (Baseline)



(c) 1MHz LLC, Discrete devices
Power density: 76W/in^3
6.3× (baseline)



(d) 1MHz LLC, IPEM-based
Power density: 110W/in^3
9.2× (baseline)

Figure 5-32. Summary of IPEM improvement on DC/DC converter.

IPEMs concepts are then extended to the system level and implemented into whole front-end AC/DC converter. Through embedded power technology, both PFC stage and DC/DC stage switching devices are integrated into System Active IPEM. In this way, layout of bus capacitor is no long critical to system

performance and simplifies the system design. Due to switching loss reduction, experimental results demonstrated that by using integrated approach, converter efficiency can be improved by 2% at high input line and around 3% at 90V AC input. Meanwhile, due to the larger parasitic capacitance caused by the flat shape heat-sink, the EMI performance of IPEM version front-end AC/DC converter is worse than the discrete version. This can be further improved by using better layout of the system.

Prospects of power integration can be expected based on the experimental results. For 400 kHz PFC with 400 kHz LLC, IPEM-based front-end converter is expected to achieve around 15W/in^3 power density. While for 400 kHz PFC with 1 MHz LLC, IPEM-based front-end converter, 25W/in^3 power density is expected.

Chapter 6. Summary and Future Work

6.1 Summary

Because of high performance, high reliability, and easy maintainability, distributed power systems (DPS) are widely adopted by telecom and high-end server applications. In recent years, with the development of information technology, demands for power management of telecom and server applications is keep increasing, which provides large market for DPS systems. As the key component for DPS systems, front-end AC/DC converters are under the pressure of continuously increasing power density, which attracts large research efforts to investigate different improvement solutions. In this dissertation, high-density integrated solution for front-end AC/DC converter of a distributed power system has been discussed.

Because of the two-stage structure, it is required to achieve high efficiency and high power density for both the PFC stage and DC/DC stage.

For PFC stage, conventional single switch CCM PFC is the most widely used topology because of its simple structure and smaller EMI filter size. However, to meet the EMI standard, as well as maintain small filter size, switching frequency of PFC circuit is normally chosen below 150 KHz. Because of the low switching frequency, PFC inductor size is large and difficult to achieve high power density. In Chapter 2, based on the analysis on switching frequency impacts on PFC

circuit, especially the Boost inductor and EMI filter, it was revealed that switching frequency of PFC circuit is required to be higher than 400 kHz. In this way, both the PFC inductor and EMI filter size will keep decreasing with the increasing of switching frequency. Furthermore, switching frequency of PFC circuit should avoid the region between 150 kHz and 400 kHz.

Although the theoretical analysis and experimental results verify the effectiveness of increasing PFC circuit switching frequency, it is important to find a suitable PFC topology that allow the high switching operation. For single switch CCM PFC, with conventional MOSFETs and Si-based fast recovery diode, large switching loss and conduction is generated, which prevents the circuit operating at higher switching frequency. With the development of semiconductor devices, CoolMOS^{TM} and SiC diode dramatically improve the switching performance of MOSFETs and diode. Therefore, conventional PFC could operate at 400 kHz or even higher while still maintains high efficiency. Meanwhile, PFC efficiency could be further improved via other topologies. In Chapter 3, three-level PFC with range switch and dual Boost PFC have been investigated. Comparing with conventional PFC circuit, due to the less conduction loss and switching loss, these alternative topologies can further improve the PFC efficiency. Or in other words, to maintain same efficiency, these circuits could operate with much higher switching frequency. Thus, more size reduction of PFC inductor and EMI filter could be achieved.

After the high density PFC stage, high density DC/DC stage is discussed in Chapter 4. Due to holdup time requirement, bulky holdup time capacitors are normally used in front-end converters. Although holdup time capacitor could be reduced with wide input range DC/DC converter, conventional PWM DC/DC converter with wide input range couldn't achieve high efficiency. Instead of using PWM converters, LLC resonant converter is able to achieve high efficiency together with wide input range, because of its gain characteristics. Moreover, due to less switching loss, LLC resonant converter can operate at 1 MHz to achieve high power density. By using the proposed design method, a 1 MHz LLC resonant converter, with 48V 1kW output is able to achieve 92.5% efficiency at full load and 94.5% efficiency at 700W load, with 76W/in^3 power density. At the same time, because of wide input range design, the holdup time capacitors could be reduced from 880uF to 440uF and achieves 50% size reduction.

Besides improving circuit topology and performance, high density front-end converter could be realized by using integrated solution. By integrating active devices together with the associated gate drivers, Active IPEM could largely reduce switching circuit parasitics and improve switching loss and voltage stress on the devices. By integrating the passive components, such as capacitors, inductors and transformers together, Passive IPEM can reduce the components profiles, size and interconnections. Furthermore, Passive IPEM concept can be further extended to EMI filter implementation. Therefore, integrated solution for front-end converters could results in higher power density, better electrical

performance and better thermal management. Moreover, due the modular approach, whole front-end converter could be assembled by putting different IPEM modules together. Therefore, automatic manufacturing is possible, which can result in much less cost.

6.2 Future work

Although the converter level improvement by using better semiconductor devices, better circuit topologies, and better packaging technology, higher efficiency and higher power density of the front-end converter could be realized, further investigation is still needed to improve energy transfer efficiency via system level improvement.

A simplified DPS system without considering the parallel front-end converters is shown in Figure 6-1. It can be observed that the energy transferred to loads passes through many processing stages. Therefore, energy transfer efficiency is low.

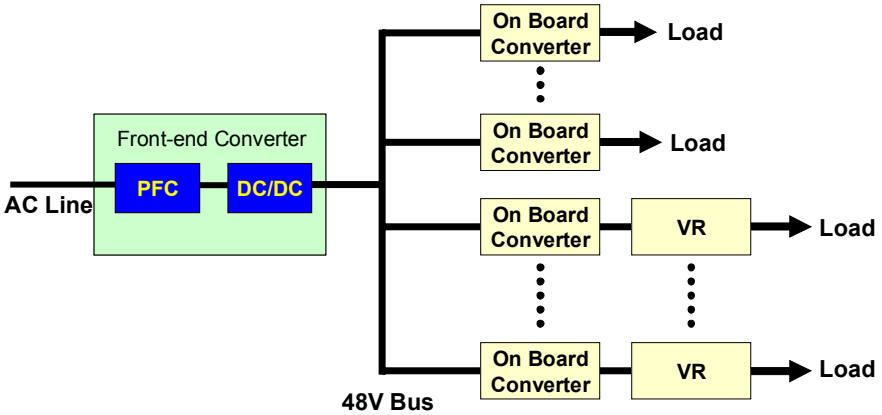


Figure 6-1. Simplified DPS system.

Instead of simply focusing on improving each power processing stage efficiency, more improvement could be realized by modifying the system structure. For on board converters, 48V input is not an optimal input voltage, because of large step down ratio and high switching loss caused by high input voltage. By adding an intermediated bus converter, as shown in Figure 6-2, 48V bus is firstly step down to an unregulated 12V intermediate bus. In this way, on board converters can be optimally designed and achieve higher efficiency. At the same time, because the bus converter only generates an unregulated bus voltage, it could always operate with it optimal operation point and maximize its efficiency. This intermediate bus structure could further improve system efficiency.

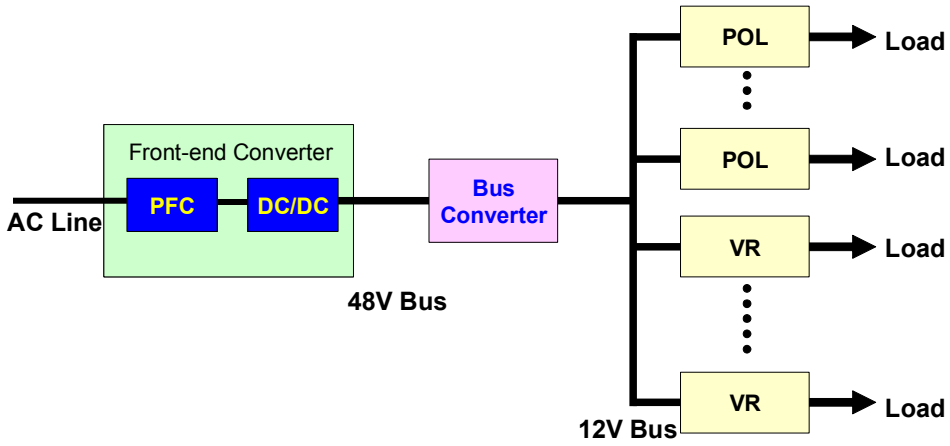


Figure 6-2. DPS system with unregulated intermediated bus.

Furthermore, after examining the system shown in Figure 6-2, it can be observed that DC/DC stage in front-end converter and intermediated bus converter are cascade together. They could be replaced with a single bus converter that directly transfers 400V DC to 12V unregulated bus, as shown in Figure 6-3.

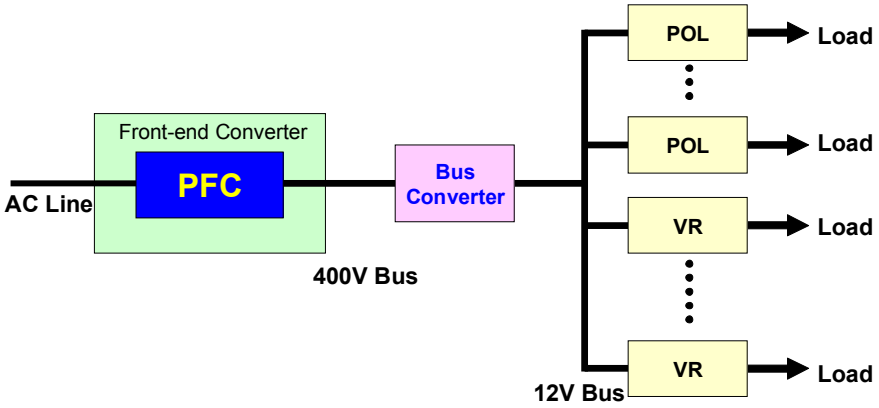


Figure 6-3. Improved DPS system

In this new system structure, one power processing stage is removed. Thus, higher efficiency can be expected.

According to these discussions, system energy transfer efficiency could be improved by both circuit improvement and system structure improvement. The further investigation should focus on searching for optimal system structure and high efficiency bus converter .

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