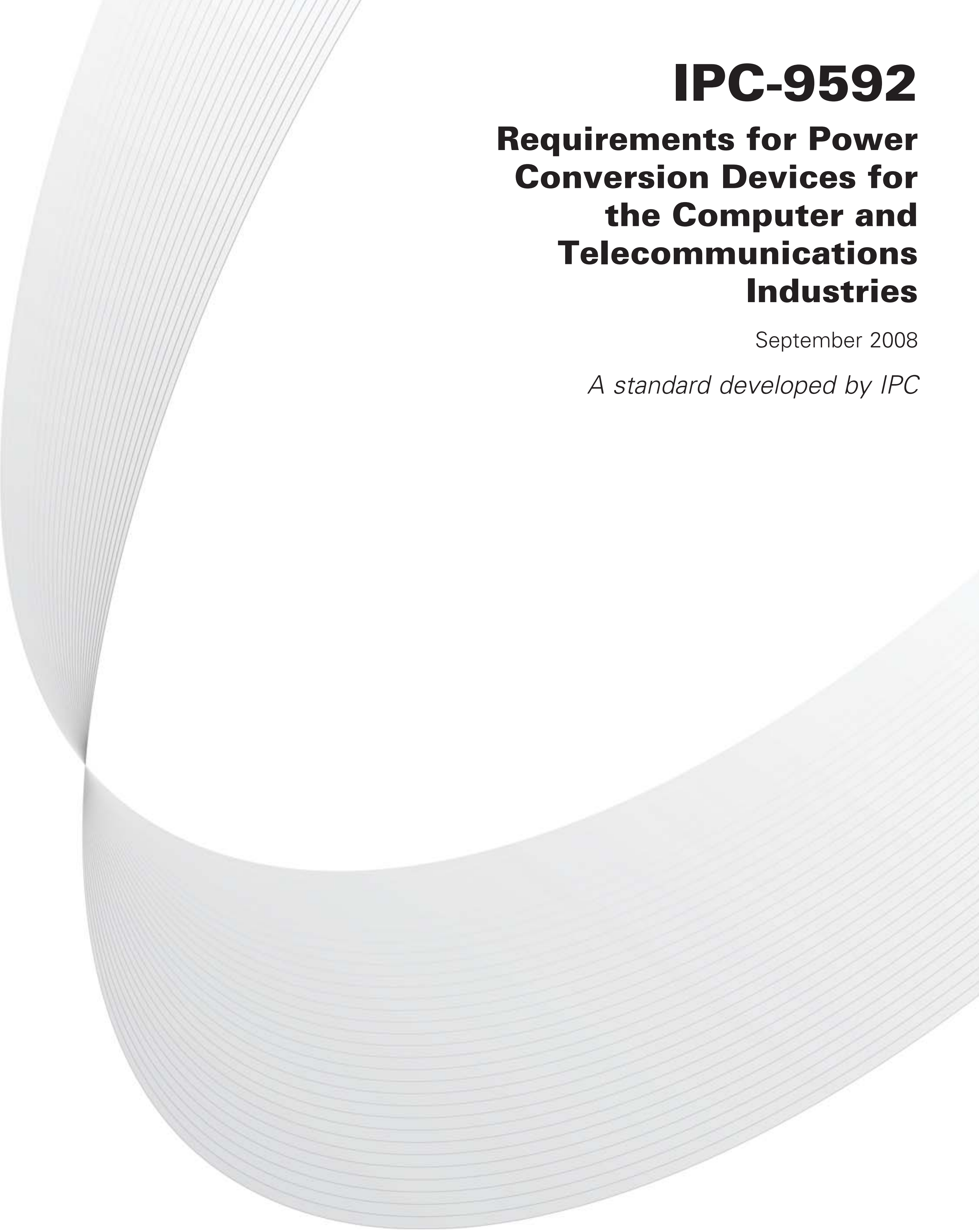

# IPC-9592

## Requirements for Power Conversion Devices for the Computer and Telecommunications Industries

September 2008

*A standard developed by IPC*

*Association Connecting Electronics Industries*

IPC®

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## IPC-9592

# Requirements for Power Conversion Devices for the Computer and Telecommunications Industries

Developed by the Power Conversion Devices Standard Subcommittee (9-82) of the OEM Management Council Steering Committee (9-80) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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# Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Power Conversion Devices Standard Subcommittee (9-82) of the OEM Management Council Steering Committee (9-80) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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# Requirements for Power Conversion Devices for the Computer and Telecommunications Industries

## 1 SCOPE

**1.1 Statement of Scope** This document standardizes the requirements for power conversion devices (PCDs) for the computer and telecommunications industries. The phrase ''power conversion devices'' refers to ac to dc and dc to dc modules, converters and power supplies. This specification sets the requirements for design; qualification testing; conformance testing and manufacturing quality/reliability processes, but does not include the functional requirements of the specific equipment.

**1.2 Description** Power Conversion Devices (PCDs) addressed in this document are used in the electronics industry to provide conversion of main power sources, usually ac, to lower dc voltages either for direct use of electronic circuits, or as a secondary source for additional dc to dc PCDs to provide several dc voltage levels for various electronic devices in a product. Any deviations due to applicable regulatory standard updates take precedence over this document.

***Performance Parameters*** are comprised of mechanical, electrical, environmental, quality/reliability and regulatory requirements:

Mechanical requirements include form and size, connector and wiring configurations and cooling needs.

Electrical requirements define the electrical interface, including power source (ac or dc), input voltage, frequency and current needs, output voltages and current capabilities and, where applicable, logic controls.

Environmental requirements entail both operating and shipping temperatures, humidity, shock and vibration limits.

Quality/Reliability Assurance requirements include definitions and requirements for the design and testing of the quality and reliability of PCDs.

Regulatory requirements are international standards for safety, electronic interference and environmental impact of PCDs.

***Methods*** This document describes specific methods to meet the defined performance parameters. These methods are ***Design for Reliability, Design Qualification Testing, Manufacturing Conformance Testing,*** and ***Quality Processes.*** In addition, this document specifies key ***Regulatory Requirements*** pertaining to PCDs.

**1.3 Purpose** The purpose of this document is to create a set of consistent specifications and methods to assure suitability, quality, safety and reliability of PCDs for the electronics industry. These specifications will apply to suppliers of PCDs, including their design and testing, and will provide guidelines for the end user to ensure adequate specifications for use in their products. All of the specifications and requirements defined in this document are intended to be part of suppliers' PCDs certifications outlined by the customers and will ship with first article and any design changes to the PCD, on request by the user.

**1.4 Order of Precedence When Purchasing** In the event of conflict when this document is utilized for purchasing a product addressed by this IPC standard, the following order of precedence **shall** apply:

a. Purchase order.
b. Master drawing.
c. This standard.
d. Applicable documents (see Section 2).

## 2 APPLICABLE DOCUMENTS AND TERMS AND DEFINITIONS

### 2.1 IPC[1]

**IPC J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies

**IPC/ECA J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires *(Please note that the most current revision of this standard is not available from the JEDEC organization.)*

**IPC-T-50** Terms and Definitions for Interconnecting and Packaging Electronic Circuits

**IPC-A-610** Acceptability of Electronic Assemblies

**IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

**IPC-9591** Performance Parameters (Mechanical, Electrical, Environmental and Quality/Reliability) For Air Moving Devices

**IPC/JEDEC J-STD-020** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

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[1] www.ipc.org

### 2.2 International

#### 2.2.1 Canadian Standards Association (Canada)[2]

**CAN/CSA C22.2 No. 60950-1** Safety of Information Technology Equipment, Including Electrical Business Equipment

#### 2.2.2 International Organization for Standardization[3]

**ISO 3741** Determination of sound power levels of noise sources - Precision methods for broad-band sources in reverberation rooms (equivalent to ANSI/NAIS S12.51)

**ISO 3744** Determination of sound power levels of noise sources using sound pressure - Engineering method in an essentially free field over a reflecting plane (equivalent to ANSI/NAIS S12.54)

**ISO 7779** Acoustics - measurement of airborne noise emitted by information technology and telecommunications equipment

**ISO 9001** Quality management systems - Requirements

**ISO 9296** Acoustics - Declared noise emission values of computer and business equipment

**ISO 10302** Method for the measurement of airborne noise emitted by small air-moving devices (equivalent to ANSI S12.11)

#### 2.2.3 GB China[4]

**GB 4943-2001** Safety of Information Technology Equipment (Including Electrical Business Equipment)

#### 2.2.4 International Electrotechnical Commission[5]

**IEC 60028-2-27** Environmental Testing - Part 2.27 Test Ea and guidance: Shock

**IEC 60068-2-31** Environmental Testing - Part 2.31 Test Ee: Drop and topple, primarily for equipment-type specimens

**IEC 60068-2-32** Environmental Testing - Part 2.32 Test Ed: Freefall

**IEC 60068-2-64** Environmental Testing - Part 2.64 Test Fh: Vibration, broad-band random (digital control) and guidance

**IEC 60529** Degrees of Protection Provided by Enclosures (equivalent to EN 60529)

**IEC 60950-1** Safety of Information Technology Equipment, Including Electrical Business Equipment, including all national deviations as specified in the current CB Bulletin

**IEC 61000** Electromagnetic Compatibility (EMC) - consists of over 30 documents covering electromagnetic and radio interference, power line interference, ESD, immunity and ground (earth connection) testing

**IEC 61000-3-2** Electromagnetic Compatibility (EMC) - Part 3-2 Limits - Limits for Harmonic Current Emissions (Equipment Input Current ≤16A per Phase)

**IEC 61000-4-2** Electromagnetic Compatibility (EMC) - Part 4-2 Testing and Measurement Techniques - Electrostatic Discharge Immunity Test

**IEC 61000-4-3** Electromagnetic compatibility (EMC) - Part 4-3 Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test

**IEC 61000-4-4** Electromagnetic compatibility (EMC) - Part 4-4 Testing and measurement techniques - Electrical fast transient/burst immunity test

**IEC 61000-4-5** Electromagnetic compatibility (EMC) - Part 4-5 Testing and measurement techniques - Surge immunity test

**IEC 61000-4-6** Electromagnetic compatibility (EMC) - Part 4-6 Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields

**IEC 61000-4-11** Electromagnetic compatibility (EMC) - Part 4-11 Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests

**IEC 61000-4-12** Electromagnetic compatibility (EMC) - Part 4-12 Testing and measurement techniques - Oscillatory waves immunity test

**IEC 62040-1-1** 1st edition and IEC 62040-1-2 1st edition Components and Subassemblies used in Uninterruptible Power Systems (and their equivalent adapted standards such as EN 62040-1-1 or UL 1778, etc. in different countries)

#### 2.2.5 Norma Oficial Mexicana[6]

**NOM-019-SCFI** Safety of Data Processing Equipment

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[2] www.csa.org
[3] www.iso.org
[4] www.bzcbs.com
[5] www.iec.ch
[6] www.normex.com.mx

### 2.2.6 European Norm[7]

**EN 50116** Information Technology Equipment. Routine Electrical Safety Testing in Production

**EN 55022** Information Technology Equipment - Radio Disturbance Characteristics - Limits and Methods of Measurement

**EN 55024** Information Technology Equipment - Immunity Characteristics - Limits and Methods of Measurement

## 2.3 United States

### 2.3.1 TELCORDIA[8]

**GR-1274-CO** Generic Requirements for Reliability Qualification Testing of Printed Wiring Assemblies Exposed to Airborne Hygroscopic Dust

**SR332** Reliability Prediction Procedure for Electronic Equipment

### 2.3.2 JEDEC[9]

**EIA/JESD22-A101** Steady State Temperature Humidity Bias Life Test

**JESD22-A108** Temperature, Bias and Operating Life

**JESD22-A114** Electrostatic Discharge (ESD) Sensitivity Testing - Human Body Model (HBM)

**JESD47E** Stress-Driven Qualification of Semiconductor Circuits

**2.4 Terms, Definitions and Acronyms** The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined below.

***AABUS –***

(As an Acronym): As Agreed Between User and Supplier

(As a Term): Indicates additional or alternate requirements to be decided between the user and the supplier in the procurement documentation. Examples include contractual requirements, modifications to purchase documentation and information on the drawing. Agreements can be used to define test methods, conditions, frequencies, categories or acceptance criteria within a test, if not already established.

***AFR –*** Annualized Failure Rate: The average failure rate of a population of products normalized to a year.

***ASD –*** Acceleration Spectral Density.

***AST –*** Accelerated Stress Testing.

***AQL –*** Average Quality Level.

***Arrhenius Relationship –*** Mathematical model for relation of failure rate to temperature.

***ATE –*** Automated Test Equipment.

***Baseplate –*** A mounting surface used to conduct heat away from a PCD.

***BI –*** Burn-In.

***BIA –*** Burn-In audit.

***BOM –*** Bill of Material.

***BMP –*** Board Mount Power: Refers to encapsulated and open PWB power converters that are mounted on larger PWBs.

***CIP –*** Continuous Improvement Process.

***Cp –*** Process Capability: An indicator of process capability using the ratio of specification width to process variation.

***Cpk –*** Process Capability Index: Adjustment of Cp for the effect of a noncentered distribution. Measures how close a process is running to its specification limits, relative to the natural variability of the process and center of the distribution.

***Cross Regulation –*** In a multiple output power supply, the change in output voltage at one output caused by the load change on another output (adapted from the PSMA Handbook of Terms).

***Custom –*** Product developed and qualified to meet customer specific requirements.

***DFMEA –*** Design Failure Modes and Effects Analysis.

***DL –*** Destruct Limit: The stress level at which a product will fail. When the stress level is reduced, the failure will not recover (i.e., this is a hard failure).

***DPMO –*** Defects per Million Opportunities.

***DVT –*** Design Verification Test: A qualification test to assess if design specifications are met.

***EDVT –*** Electrical Design Verification Test: A qualification test to assess if electrical design specifications are met.

***EFT –*** Electrical Fast Transient.

***EMC –*** Electro-Magnetic Compatibility.

***EMI –*** Electro-Magnetic Interference.

***EN –*** European Norm.

***ESD –*** Electro-Static Discharge.

***EST –*** Environmental Stress Testing.

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[7] www.ansi.org
[8] www.telcordia.com
[9] www.jedec.org

***FET –*** Field Effect Transistor: includes power MOSFETS commonly used in power converters.

***FIT –*** Failures in Time (Reliability): 1 FIT = 1 Failure/1,000,000,000 devices hours. The FIT rate (measured) = $\Sigma$ Failures $\approx \Sigma$ Operating Hours * $10^9$ and the relationship of FIT to MTBF is: MTBF = $10^9/\Sigma$ FIT (Also, see MTBF)

***Fit (as part of Form, Fit and Function) –*** The suitability or readiness of a product for a particular application, including environmental extremes, marginal parameters, physical and signal compatibility with interfacing systems and surroundings, level of performance, safety margins, reliability, maintainability and installability.

***Form (as part of Form, Fit and Function) –*** The weight, density, chemical or material composition, size, shape, structure, appearance, protocol, pattern, composition, configuration and marking/identification of a product.

***Function (as part of Form, Fit and Function) –*** The set tasks or purposes for which a product is used by the customer, including all the tasks generally accepted for the product and those specifically designated by the customer.

***Grms –*** Root Mean Square value of G, where G is acceleration due to gravity - a measure of dynamic acceleration used in vibration testing.

***HALT –*** Highly Accelerated Life Test: Design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits.

***HASA –*** Highly Accelerated Stress Audit: Performed via sample testing as opposed to 100% that is done with HASS.

***HASS –*** Highly Accelerated Stress Screening: Used to improve the robustness/reliability of a product through test-fail-fix process where the applied stresses may be beyond the specified operating limits (OL) determined by HALT. This is applied to 100% of the manufactured units.

***High Line –*** For devices designed to operate from ac sources, the highest rated nominal input voltage. For devices designed to operate from dc sources, the maximum rated input voltage.

***Hipot –*** High Potential Testing.

***Hot Swap –*** To remove or insert a PCD from or into a system that is operating.

***HTOB –*** High Temperature Operating Bias.

***IEC –*** International Electrotechnical Commission.

***IFIR –*** Initial Field Incident Rate: The defect rate experienced in the first 30 to 90 days of field usage and is the customer's initial experience with the product. The time-frame depends on the user's point of view and needs. That is, if the user is a retail consumer, then 30 days is most common because such consumers begin using the product upon delivery. For commercial or industrial users, the time-frame is more likely 60 to 90 days, where the final product my not be put into service for some number of weeks after the product is delivered and the final commercial rack-mounted device is assembled and placed into service.

***LDL –*** Lower Destruct Limit, e.g., -50 °C (also, see DL).

***Life Test –*** A test run specifically to determine reliability (or failure rate) over time of a component or product.

***Line Regulation –*** The change in output voltage for a specified change in the input voltage, at specified loads with all other factors constant, sometimes expressed as a percentage (adapted from the PSMA Handbook of Terms).

***Load Regulation –*** The change in output voltage when a load is changed from one specified steady-state value to another, with all other factors held constant (adapted from the PSMA Handbook of Terms).

***LOL –*** Lower Operational Limit, e.g., -20 °C (see OL).

***Low Line –*** For devices designed to operate from ac sources, the lowest rated nominal input voltage. For devices designed to operate from dc sources, the minimum rated input voltage.

***LSL –*** Lower Specification Limit.

***LTR –*** Long Term Reliability: Described as one or more of the following: a) Expected annual failure rate over the usable product life, expressed as a percent per year; b) Expected service life of a product in a given use condition; c) End of life is characterized where it exceeds the annual steady state failure rate by 20%; or d) Service life, expressed in years, for a given use condition.

***LTPD –*** Lot Tolerance Percent Defects.

***LRR –*** Line Reject Rate: The defect rate experienced at the OEM manufacturing line (not at the PCD supplier's manufacturing line). It defines the number of failed PCD units during the manufacturing and testing of the OEM PCD system. For an item that does not enter the OEM manufacturing process (referred to as a drop shipped PCD from the PCD manufacturer directly to the OEM's customer, there is no LRR metric.

***Maverick Control –*** The control process utilized to reduce or eliminate a maverick product.

***Maverick Product –*** Product that exhibits significant anomalous characteristics that may cause a higher than normal level of failure anywhere in the user's application or manufacturing line.

***MAX –*** The maximum value of a specified parameter.

***MIN –*** The minimum value of a specified parameter.

***MSL –*** Moisture Sensitivity Level.

***MTBF –*** Mean Time Between Failure (Hours): MTBF (measured) = Σ Operating Hours ≈ Σ Failures. For a population of products, MTBF **shall** apply *during* useful life when failure rates are relatively constant. MTBF is *not* a measure of how long a power supply can be expected to survive. (MTBF may be estimated from methods such as Telcordia SR332, or from hardware tests.)

***MTR –*** Manufacturing Test Requirement.

***OBA –*** Out of Box Audit.

***OCP –*** Overcurrent Protection.

***OL –*** Operational Limit: The stress level at which a product may lose its function. However, when the stress level is reduced, the function will recover.

***ORT –*** Ongoing Reliability Test.

***OTP –*** Overtemperature Protection.

***OVP –*** Overvoltage Protection.

***PARD –*** Periodic and Random Disturbance.

***PCB –*** Printed Circuit Board (preferred term): Same meaning as PWB (Printed Wiring Board).

***PCD –*** Power Conversion Device: Refers to ac to dc and dc to dc modules, converters and printed circuit board assemblies.

***Performance Level A –*** No Effect: ''Normal performance within limits specified by the manufacturer, requestor or purchaser.''

***Performance Level B –*** Temporary Effect, Self Recovering: ''Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention.''

***Performance Level C –*** Needs Help to Recover: ''Temporary loss of function or degradation of performance, the correction of which requires operator intervention.''

***Performance Level D –*** Damaged Beyond Recovery: ''Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.''

***PFMEA –*** Process Failure Modes and Effects Analysis.

***POL –*** Point of Load.

***Power Train –*** Components that directly transform input power into output power in a PCD.

***Product Family –*** Products will be considered similar and of the same family if they use the same power train topology and component set and have printed circuit boards with equivalent minimum spacings with only minor differences for output voltage and alarm/communication functions. In addition, similar products must have equivalent mechanical dimensions with an exception for pin length on BMP devices.

***Product Specification –*** The comprehensive description of form, fit and function for a product, often expressed in a product data sheet (although some data sheets are only excerpts of key specifications).

***PSD –*** Power Spectral Density.

***PWB –*** Printed Wiring Board: Same meaning as PCB (Printed Circuit Board).

***RPN –*** Risk Priority Number

***RTV –*** Room Temperature Vulcanizing: A sealant or coating composed of a silicone elastomeric polymer that cures/vulcanizes by moisture.

***Service Life –*** Minimum time, specified in years, during which failure rates are constant or decreasing and cumulative failures for a single wearout failure mechanism do not exceed 1%.

***SOA –*** Safe Operating Area.

***Standard (Noncustom) –*** Product developed and qualified without customer specific requirements.

***Statistical Confidence Limits –*** Mathematical bounds on distribution estimates made from a sample.

***Statistical Process Control –*** Methods using statistical techniques to assess the stability of processes in order to take appropriate action to reduce defects, and to determine the quality level of components, assemblies and products. Often called SPC and also called SQC (Statistical Quality Control).

***Statistical Quality Control –*** See Statistical Process Control.

***STRIFE –*** Stress + Life Test: Design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits (also, see HALT).

***Sub-Tier Supplier –*** In this document, applies to a component/subassembly supplier to the PCD supplier.

***Supplier –*** In this document, applies to a PCD supplier.

***Temperature Regulation –*** The change in output voltage when the ambient temperature is changed from one specified steady-state value to another, with all other factors held constant.

***Thermally Stable –*** A device is considered to be thermally stable (at a constant temperature) when the device temperature does not change after three successive temperature readings that are taken at least 15 minutes apart.

***THB –*** Temperature Humidity Bias.

***Thermal Stability Time –*** The total time from the first temperature reading of a device to the last reading that incorporates at least 3 successive readings, separated by a minimum of 15 minutes apart from each other and during which there is no difference in the device's recorded temperature.

***Turn-Off Delay Time –*** The time from the removal of input power or negation of an on/off control signal until the output voltage starts to decrease (usually measured at the point where the voltage is at 90% of its initial value).

***Turn-Off Fall Time –*** The time required for the output voltage to fall, typically measured from the points where the output voltage is equal to 90% of initial value to 10% of initial value.

***Turn-Off Time –*** The time from the removal of input power or negation of an on/off control signal until the output voltage is off. This is typically the sum of the Turn-Off Delay Time and the Turn-Off Fall Time

***Turn-On Delay Time –*** The time from the application of input power or assertion of an on/off control signal until the output voltage starts to increase (usually measured at the point where the voltage is at 10% of its final value) (adapted from PSMA Handbook of Terms).

***Turn-On Rise Time –*** The time required for the output voltage to rise, typically measured from the points where the output voltage is equal to 10% of final value to 90% of final value.

***Turn-On Time –*** The time from the application of input power or assertion of an on/off control signal until the output voltage is in regulation and meets the specification. This is typically the sum of the Turn-On Delay Time and the Turn-On Rise Time (adapted from the PSMA Handbook of Terms).

***UDL –*** Upper Destruct Limit, e.g., 150 °C or 40Grms Vibration (see DL).

***UOL –*** Upper Operational Limit, e.g., 100 °C or 30Grms Vibration (see OL).

***Useful Life –*** See Service Life.

***User –*** In this document, applies to the customer of the PCD supplier.

***USL –*** Upper Specification Limit.

***UVP –*** Undervoltage Protection.

***Vsb –*** Standby Voltage: An output voltage available when the PCD has an input voltage ≥ the Turn-on voltage, even when the PCD is turned off.

***Wearout –*** The time at which a PCD's average failure rate increases by greater than 50%.

## 3 PRODUCT SPECIFICATION AND DOCUMENTATION REQUIREMENTS

The information presented in Section 3, on specifications and documentation requirements, is to be imposed or held to be in-force only for the technology specific application need as discussed between the user and supplier.

**3.1 Product Classification System** Two general classes of PCDs have been established to reflect progressive increases in sophistication, functional performance requirements and testing inspection frequency. It should be recognized that there may be an overlap of both computer and telecommunications end equipment categories in different classes. The user has the responsibility to specify in the contract or purchase order the performance class required for each PCD, and **shall** indicate any exceptions to specific parameters where appropriate.

**3.1.1 Class 1 General or Standard PCDs** Includes PCDs for consumer computer, telecommunications products and peripherals. These PCDs are generally designed to operate in controlled environments, with intermittent and interruptible service, and with up to five years of product life.

**3.1.2 Class 2 Enhanced or Dedicated Service PCDs** Includes PCDs for carrier grade telecommunications equipment and network grade computers, sophisticated business machines and instruments where high performance and extended life is required. These PCDs are generally designed to operate in controlled environments, with limited excursions to uncontrolled levels, and with uninterrupted service, and with no less than five years and up to fifteen years of product life.

**3.1.3 ac to dc and dc to dc PCDs** This document **shall** also, where appropriate, differentiate requirements between ac to dc PCDs and dc to dc PCDs, as these devices tend to have different interface requirements due to the characteristics of the sources and load that connect to each type of PCD.

**3.1.4 Three Categories of Product**

*Category 1:* dc output power supplies to be embedded in equipment, whether the input power is ac or dc.
*Category 2:* Board mounted dc to dc converters including both isolated and nonisolated converters
*Category 3:* ac to dc power supplies used as adapters and chargers that are external to the equipment being powered.

**3.2 Documentation Requirements** The supplier **shall** be able to supply the user with the following pertinent documentation in a reasonable time frame. This documentation **shall** be provided, AABUS, before the evaluation of engineering first article samples and with appropriate NDA protection executed.

- Theory of operation.
- Applicable schematics.
- Qualification test plan.
- EMC reports.
- Reliability data and calculation.

- Design checklist.
- Sample qualification test report.
- DVT report.
- HALT report.
- SMT Power Module Solder Attachment Reliability report.
- Failure Mode and Effect Analysis (FMEA) - Custom products only.
- BOM.
- Approved supplier list for all components.
- PCB artwork.
- Component drawings, including magnetic.
- Manufacturing drawings.
- Regulatory reports (if applicable).
- Change history.
- Mechanical dimension measurements.
- Derating report.

**3.3 Data Sheet Information - Form, Fit and Function** The supplier **shall** provide complete specifications of form, fit and function, including electrical specifications and whether it **shall** be Class 1 or Class 2. The data sheet **shall** be dated and have revision level marked at the bottom of the sheets. Not all of these elements will necessarily apply to a given PCD. Specific values for these parameters cannot be defined in this section as they will depend on the particular device application and requirements.

### 3.3.1 Input Power Specifications

**3.3.1.1 ac to dc PCD Data Sheet** Data sheet **shall** include nominal input voltage, input voltage range, universal versus switched input voltage, input frequency range, input impedance, inrush current (primary inrush and subsequent pulses), minimum efficiency at a defined load, power factor, Turn-on time, auto-restart specifications, input overcurrent protection and fuse type, ac input receptacle type, limits for harmonic current emissions (EN61000-3-2), isolation voltage, ac leakage current, slow line transient performance (sag and surge), ac line dropout response, full cycle ride thru frequency, maximum chassis current or Y capacitor value, dielectric withstand voltage and Energy Star® (US Environmental Protection Agency) requirements, as applicable - technology specific.

**3.3.1.2 dc to dc PCD Data Sheet** Data sheet **shall** include number of voltage inputs, input voltage range(s), minimum efficiency at a full load (define this full load), input overcurrent/reverse voltage protection and fuse requirements, input filter capacitance requirements and conducted EMI, as applicable - technology specific.

**3.3.2 Logic, Indicator and Control Specifications** (As applicable) Data sheet **shall** include remote on-off signal requirements, power good signal specifications, communications bus or other serial port specifications, control logic timing requirements, control and logic signal ripple and noise requirements, fan speed control specifications and LED indicator specifications, as applicable - technology specific.

The PCD supplier **shall** provide the trim equations and schematics, and a table showing the trim resistor values. Additionally, detailed information and recommendation on Trim Control via external voltage or current source (D/A converter), $I^2C$ or equivalent communications bus, overvoltage, undervoltage, overcurrent and overtemperature (latching or not) performance **shall** be provided on request.

### 3.3.3 Output Specifications

**3.3.3.1 ac to dc PCD Data Sheet** Data sheet **shall** include the time when the device is considered to be thermally stable, dc output voltages, output current capability, minimum load requirements, dc voltage output tolerances, output load regulation, output temperature coefficient (%/°C) output ripple and noise, common-mode voltage and common-mode current, output to output isolation, voltage adjustment range, output transient response to dynamic loading, capacitive loading capability, Turn-on overshoot characteristics, overcurrent protection, short circuit protection, overvoltage and undervoltage protection, reverse voltage protection, thermal protection, reset after shutdown conditions *(hiccup or latch off)*, remote sense specifications, current sharing/parallel operation requirements and output connector specifications, as applicable - technology specific.

**3.3.3.2 dc to dc PCD Data Sheet** Data sheet **shall** include number of outputs, nominal output voltage(s), voltage tolerance (each output), line regulation (each output), load regulation, output capacitance range noise and ripple, short circuit protection time, transient response, output temperature coefficient (%/°C), I/O isolation voltage and isolation resistance, as applicable - technology specific.

**3.3.3.3 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** include storage temperature, operating temperature, nonoperating humidity, operating humidity, nonoperating altitude, operating altitude, cooling requirements method, cooling requirements versus altitude, output derating versus temperature, shipping/storage vibration, operating vibration, shipping/storage shock and operating shock, as applicable - technology specific.

### 3.3.4 Reliability

**3.3.4.1 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** include reliability specified as FIT rate at a specified operating condition and service life, as applicable - technology specific.

### 3.3.5 Safety and Regulatory

**3.3.5.1 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** list certifications for safety, EMC compliance, lead-free and restricted materials compliance such as RoHS/WEEE certification, as applicable - technology specific.

### 3.3.6 Physical Dimensions and Electrical Connections

**3.3.6.1 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** include acoustics measurements and methods, complete dimensions, weight, electrical connector definitions and drawings of PCD and of shipping and packaging configurations, as applicable - technology specific.

**3.4 Material Control and Labeling** The PCD supplier **shall** implement a documented, capable material control system for all incoming, in-process and outgoing material. Documentation of a material control plan **shall** be made available, AABUS. The material control system **shall** include the following elements:

A. ***Material Identification*** All material **shall** be properly segregated and/or labeled throughout the testing and manufacturing process.

B. ***Discrepant Material*** All discrepant material **shall** be reworked or disposed of according to the supplier's material control system requirements. Records of all rework and scrap **shall** be kept and summary reports provided to the user on request.

C. ***Labeling*** All PCDs **shall** be labeled and each PCD **shall** have the markings of 1 through 9, below. For smaller PCDs, space may not be available for all these items on the PCD. Therefore, items are shown in priority of importance, and **shall** be included from item 1, until space is exhausted. Remaining items **shall** be included on the PCD packaging.

   1) Part number, serial number and lot date code in human readable text format (space permitting, otherwise in machine readable format).
   2) Appropriate regulatory certification labels and any required cautionary statements.
   3) Model and Manufacturer's name.
   4) For ac to dc units: Nominal ac input voltages and frequencies. Maximum ac input currents. For dc to dc units: Nominal dc input voltages. Maximum dc input currents.
   5) Nominal Output Voltages and Maximum Continuous Output Currents.
   6) Maximum Continuous Output Power.
   7) Country of Origin [i.e., (Product of XXXX) where XXXX is country of final assembly].
   8) Date of latest printed circuit board artwork revision and revision level of the schematic.
   9) For ac to dc units, caution label **shall** be located on the visible side of the PCD, stated in English, French, German, Italian, Spanish, Portugese and Chinese.

**3.5 Revision Control** All changes affecting form, fit, function, or regulatory agency requirements **shall** cause a next level revision of the supplier's part numbers, or be correlated to a cut-in date that **shall** be tracked by specific production week code contained in the product serial number. Specific information for change traceability **shall** be provided in the Change Notice as discussed in Section 6. The revision control number and/or production date code **shall** be placed on the ID label away from the PCD part number. The user **shall NOT** ship to its customers, nor accept units for revenue that have not been released to manufacturing at the supplier's facility. The release of units to manufacturing indicates that the PCD is fully agency approved (regulatory and safety), where such agency approval is required.

## 4 DESIGN FOR RELIABILITY

This section describes industry best practices for PCD suppliers to specify, design and document the performance and reliability of a PCD. Exceptions to these methods **shall** be documented and shared with the user as agreed between user and supplier (AABUS).

**4.1 Reliability Prediction (FIT)** With user's operating specifications provided, the supplier **shall** define expected reliability of a PCD and the conditions under which the reliability is specified. The overall Power Supply FIT rate **shall** be supplied and **shall** be calculated using Telcordia Technologies SR-332, *Reliability Prediction Procedure for Electronic Equipment* (Method 1, Case 1: Parts Count, AABUS). The supplier **shall** specify the quality level used. Caution should be exercised when interpreting FIT rates using any predictive model. Models may not consider actual electrical stresses on the power components or may rely strictly on temperature rise estimation and component count. In addition, individual component FIT rate estimates used in these models may not accurately reflect the actual FIT rates of components used by a given power manufacturer. As a result, predictions are often subjective and may vary significantly from actual reliability. Using these methods for comparing one PCD supplier to another could lead the user to the wrong conclusion with respect to the overall reliability of the design.

**4.2 Component Selection** The PCD supplier **shall** have a documented process in place to select all components for product designs and **shall** provide information on all components and all component suppliers to the PCD user as described below, AABUS. The component selection process **shall** incorporate the following factors:

- The supplier **shall** assure that electrical, mechanical and thermal specifications for all components meet the requirements of the Derating Guidelines, described in 4.3 and Appendix A, for the operating conditions of the PCD design. Exceptions to derating guidelines are allowable only if documented with data supporting that the violation will not negatively impact reliability or service life.
- For custom products, the supplier **shall** assure that effects of all critical component failure modes have been considered in the DFMEA analysis and that appropriate corrective action has been taken where required. Supplier **shall** upon request, provide a report to the user, as described in 4.4.
- The supplier **shall** develop and implement a quality management system that will define quality and technical requirements to their sub-tier suppliers. Quality and technical requirements are defined as quality programs, software control processes, engineering drawings, specifications and functions to be performed by sub-tier suppliers. The PCD supplier may elect to use a contract, purchase order or other suitable means in defining these requirements, as long as the quality and technical requirements are fully documented and that the sub-tier supplier verify understanding and implementation of such requirements.
- The supplier **shall** perform a quality review of all proposed sub-tier suppliers prior to awarding business to a sub-tier supplier as described in 6.2.
- The supplier **shall** review component reliability requirements with their sub-tier suppliers. The supplier **shall** implement testing as required to verify performance and reliability of components, or **shall** assure that the sub-tier supplier implement and report on such testing. Test reports **shall** be provided on a regular basis as agreed upon by supplier and user.

**4.3 Derating Guidelines** In order to provide a reliable power conversion product the supplier **shall** use the method of component derating specified in Appendix A in all electrical designs and **shall** provide details on the derating methods, conditions and results to the PCD user upon request. Documentation reflecting results of the derating analysis is to be according to the items listed in 4.3.1. Exceptions to this are to be AABUS.

Derating is a technique used to ensure that component ratings are not exceeded, either under steady state or transient conditions. The intent of component derating is to improve reliability of electrical components in electronic products by compensating for many variables inherent in a design. Proper component derating will lower failure rates through reduced stresses, reduce the impact of material, manufacturing and operational variability, and enable continued circuit operation with long term part parameter shifts.

**4.3.1 Derating Documentation Requirements** The items listed below **shall** be documented for each derating evaluation. Soft and/or hard copies of each item **shall** be provided upon customer request.

- Applicable schematics.
- Data on component(s) where Derating Guidelines are not met, supporting the stress level to which each PCD component is exposed.
- Electrolytic Capacitor Life calculation from each supplier.
- Electrical and thermal stress levels (e.g., voltage, temperature, etc.) for each derated component shown by reference designator.
- Component ratings and specifications (upon user's request).
- Derated stress level in percent of specified maximum level.
- BOM.
- Approved supplier list for all components.
- Change history.

**4.4 Design Failure Modes and Effects Analysis (DFMEA)** PCD suppliers **shall** complete a Design Failure Mode and Effects Analysis for each custom PCD design on new topologies/architectures with no previous DFMEA, or in cases where there are new technology components, significant component changes, or AABUS. Supplier **shall** provide results of the analysis, and of any corrective actions, to the customer upon request DFMEA is to be performed early in the power supply development cycle.

The DFMEA activities are designed to:

1. Recognize and evaluate the potential failure modes of each component in a product and its effects on the product.
2. Identify actions that could eliminate or reduce the chance of the potential failure occurring.
3. Document the process for improvement of future designs.

Areas to be targeted are those critical to proper power supply operation, safety and areas that are considered to be a higher design risk (i.e., new technology, new topology, or new circuitry). The intent is not to cover every aspect of every circuit or sub-circuit. DFMEAs performed on similar products or families can be used providing the supplier can provide evidence of correlation. The processes and definitions used in IEC-60812, Analysis Techniques for system reliability - Procedures for failure modes effects analysis (FMEA), **shall** be used as reference.

A DFMEA is a team-based systematic approach that examines the effects of Single Point Failures (SPF) on overall system performance and mitigates system failure risk by corrective action implementation. Key features of a DFMEA are:

1. DFMEA is a team oriented analysis of a system design. DFMEA elements are the building blocks of related information that comprise an analysis. The team approach is essential in identifying DFMEA elements. Although actual document preparation is often the responsibility of an individual, DFMEA inputs **shall** come from a multi-disciplinary team. These contributors are also the major beneficiaries of the document and the knowledge gained in the DFMEA process.
2. DFMEA is a weakness-oriented, bottoms-up approach. To begin, the lowest levels of the system are outlined; this can be the individual components or the lowest assemblies in the system. For each lowest level element, a list of potential failure modes is generated; their local effects, next high-level effects and/or end effects are then determined. DFMEA focuses on failure mode consequences to the product's end use and assesses risk of each.
3. DFMEA is NOT a design review, but always works on the assumption that the design is nominally correct. It addresses single point failure modes. It does not cover improper usage, incorrect problem diagnosis or any software incompatibilities.

The DFMEA *method* consists of defining the DFMEA scope and the system to be investigated, identifying team members and beginning the DFMEA process itself.

The DFMEA *process* includes assignment of roles and responsibilities for team members, defining the scope of the DFMEA (finalizing DFMEA target areas, subsystem level interrelationships and level and type of the approach), differentiating between Causes, Failure Modes and Effects (being aware that failure modes can drive multiple effects, so that each unique end level effect **shall** be separated and causes for each end level effect **shall** be grouped), and defining severity, occurrence and detection rating scales for the DFMEA at hand.

One common format for a DFMEA worksheet report is shown in Figure 4-1. The supplier may share this detail of analysis with the PCD user, or may provide a summarized report listing all failure modes, effects and severity and corrective actions where effects are unacceptable to the operation of the PCD. Figure 4-2 below shows a table of Severity, Occurrence and Detection Ranking used in a DFMEA process. The ranking numbers are used in calculating the value of RPN, which is the product of the severity, occurrence and detection rank numbers. RPN stands for Risk Priority Number, and provides a relative measure of the importance of each effect. The higher the RPN, the higher the priority of its associated failure mode as needing to be resolved. Note that if the severity of a failure mode is a critical safety hazard (fire, electrical shock hazard, or other life threatening issue) the RPN value is

| Item/ Function | Potential Failure Mode | Potential Effect(s) of Failure | Severity | Class | Potential Cause(s)/ Mechanism(s) of Failure | Occurrence | Current Design Controls | Detection | Recommended Action(s) | Responsibility and Target Completion Date | Results of Action Taken | RPN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Control Chip U1 | Pin 1-2 short<br>Pin 2-3 short<br>Pin 3-4 short<br>Pin 4-5 short | No effects, however, need VRM supplier Test Plan to verify if they can detect these shorts | 1<br>1<br>1<br>1 | | Bad component, Solder bridge | 1 | | | Need VRM Supplier Test Plan to verify if they can detect these shorts | DJW - 10/20/06 | | 0<br>0<br>0<br>0 |
| | Pin 5-6 short | Shuts down the output | 4 | Signif. | Bad component, solder bridge | 1 | | 5 | Improve solder process and inspection | LBJ - 11/15/06 | | 20 |
| | Pin 6-7 short | V<5v, goes to some artificial V point | 4 | Signif. | Bad component, solder bridge | 1 | | 5 | Improve solder process and inspection | LBJ - 11/25/06 | | 20 |
| | Pin 7 to Gnd short | Short to ground, V goes up, output V high, full duty cycle (80%-90% of 12v), firing SCR and blowing fuse, possible smoke | 5 | Smoke hazard | | 2 | | 5 | Change Layout Mask | QRT - 11/30/06 | | 50 Must address because of Smoke Hazard |

**NOTE:** In Figure 4-1, the final failure mode, pin 7 to ground short, may result in emission of smoke (indicated in the Potential Effects of Failure column and in the Class column), a situation that for this example, and for PCDs in general, is an unacceptable hazard condition. Acceptable and unacceptable effects must be defined for each product type as required by the PCD user.

**Figure 4-1 DFMEA Worksheet Form Used by Many Companies**

| Severity | | | Occurrence | | | Detection | | |
|---|---|---|---|---|---|---|---|---|
| Ranking | Description | Interpretation | Ranking | Description | Interpretation | Ranking | Description | Interpretation |
| 5* | Hazardous | Safety related catastrophic failure* | 5 | Very High | Failure is almost inevitable, <1 in 3 | 5 | Absolute Uncertainly | Undetectable until catastrophic failure occurs, or there is no design control |
| 4 | High | Product is totally inoperable | 4 | Frequent | Repeated failure, <1 in 8 | 4 | Remote | Remote chance the Design Control will detect a potential Cause of failure or subsequent Failure Mode |
| 3 | Moderate | Product is operable, but at a reduced level of performance | 3 | Moderate | Occasional failure, <1 in 80 | 3 | Low | Low chance the Design Control will detect a potential Cause of failure or subsequent Failure Mode |
| 2 | Low | Product is operable, but comfort or convenience item(s) are inoperable or at a reduced level of performance | 2 | Infrequent | Relatively few failures, <1 in 150,000 | 2 | Moderate | Moderate chance the Design Control will detect a potential Cause of failure or subsequent Failure Mode |
| 1 | None | No effect | 1 | Rare | Failure is unlikely, <1 in 1,500,000 | 1 | High | High chance the Design Control will detect a potential Cause of failure or subsequent Failure Mode |

* When there is a safety hazard as a result of a failure, the failure mode MUST be eliminated

**Figure 4-2 DFMEA Severity, Occurrence and Detection Ranking Chart Used by Many Companies**

overruled by a note in the Class column that the failure mode **must** be eliminated before a design is released.

**4.5 Voltage Spacing Design Requirements** Recommended voltage-spacing between uninsulated conductors (external PWB layers) in a power assembly is defined in Figure 4-3.

All uninsulated PC board conductors, component leads, heatsinks and other conductive features **shall** meet the voltage-spacing requirements of Figure 4-3 for ac circuits, switching circuits, or any dc potential above 100V. It is recommended that these voltage-spacing guidelines be followed for dc circuits under 100V as well. Features with spacings not meeting the above voltage-spacing requirements must be insulated; for example by RTV, conformal coating, sleeving or a combination of these methods.

**NOTE:** Engineering exceptions may be taken to the above criteria based on a risk/cost analysis. Careful review of that decision is recommended.

Board-to metal chassis spacings must meet the criteria of Figure 4-3. For these situations, a guard band to the Figure 4-3 criteria is recommended. The guard band **shall** account for reasonable device lead length variability.

**NOTE:** Insulation is highly recommended between the underside of PC mother boards and chassis sheet metal, even if the above bolt-spacing requirement criterion is met.

In any case where the creepage or clearance requirements of IEC 60950 are greater than the requirements defined in Figure 4-3, they **shall** take precedence over this document.

**4.6 Moisture Sensitivity Level (MSL) Rating of Surface Mount Power Conversion Devices (PCDs)** Electronic components which are Moisture Sensitive (MS) may be susceptible to damage when exposed to elevated reflow temperatures. This is especially true for ICs exposed to lead-free reflow temperatures (up to 260 °C). Industry standards J-STD-020 and J-STD-033 define moisture sensitivity levels for SMT ICs and how they are to be packaged and handled. While there are currently no industry moisture sensitivity standards for bare printed circuit boards (PCBs), passive components or PCDs, some of these devices do exhibit moisture sensitivity.

Suppliers and users of PCDs should recognize this potential risk and take action accordingly. Examples of such actions are:

- Limit use of moisture sensitive components in PCD design.
- Package PCD in moisture barrier bags.
- Use desiccant and Humidity Indicator Card (HIC) in package.
- Limit long term exposure of PCDs to high humidity.
- Limit PCD reflow temperature exposure during customer assembly.

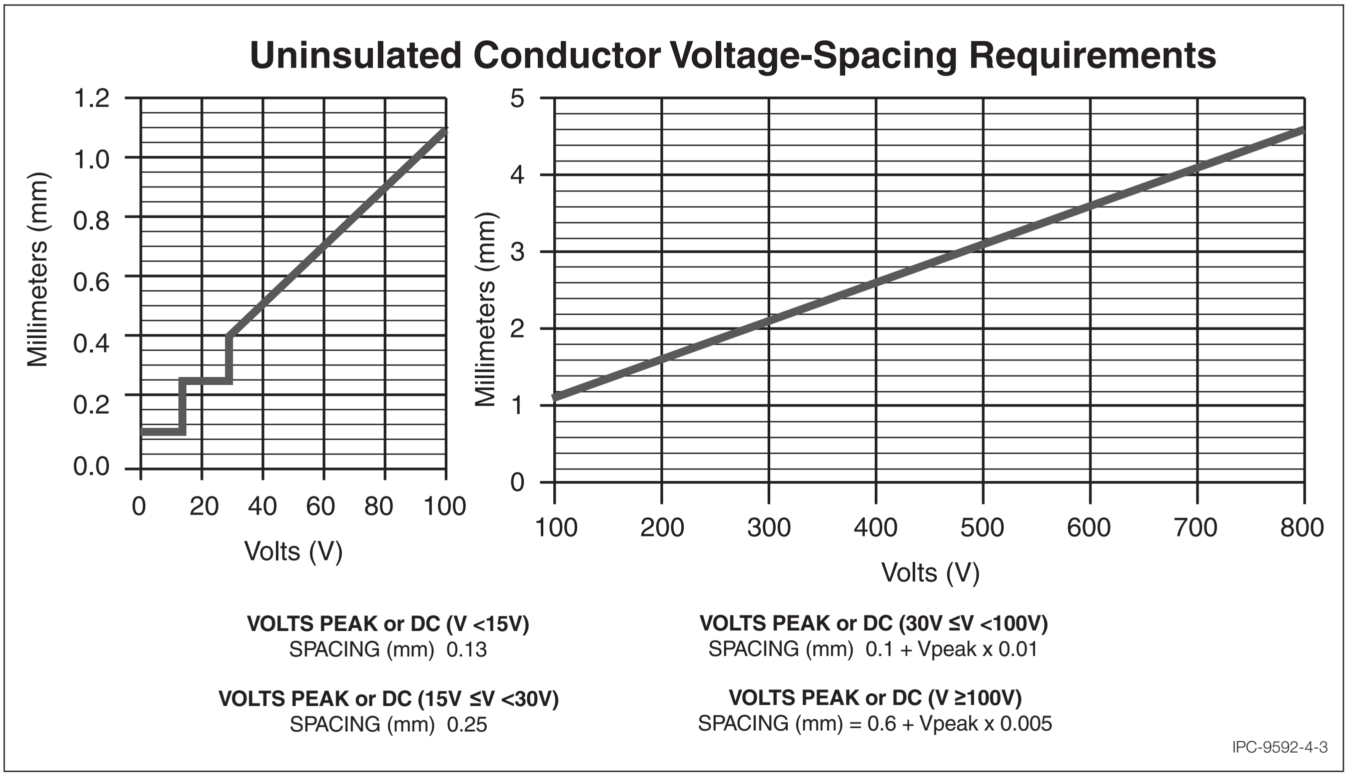


**Figure 4-3 Uninsulated Conductor Voltage-Spacing Requirements**

## 5 DESIGN AND QUALIFICATION TESTING

The testing described in this section has two main purposes. First, design verification testing and electromagnetic susceptibility testing including EMI and ESD testing, are intended to provide assurance that the device will function according to its specification. Second, environmental stress testing, including HALT, is intended to provide a measure of assurance (not proof) that the device is robust enough to operate in its intended environment without damage or degradation that would affect its operation.

After a PCD has been introduced to the market, any supplier design change requires that the supplier **shall** notify the user, per 6.5.1.3. Any additional testing required as a result of the design change **shall** be a subset of the tests detailed in this design and qualification testing section with the specific tests defined AABUS.

It is specifically not a purpose of the testing in this section to provide any measure of the device's reliability (failure rate) or expected service life.

### 5.1 Design Verification Testing (DVT)

**5.1.1 Scope of Testing** All parameters, features and functions listed or described in the device specification **shall** be tested for conformance to the specification. DVT applies to both Classes I and II.

In addition, suppliers **shall** test devices for any parameters, features or functions listed below that are not listed in the device specification.

**5.1.2 Sample Size** A complete DVT **shall** be performed on a minimum of three devices. The same devices **shall** be used for all tests.

If a unit fails during DVT testing and cannot be repaired to a like-new state, then an additional device may be substituted. This substituted device **shall** have all DVT tests performed on it. No credit can be claimed for tests performed on a device that does not complete the DVT.

**5.1.3 Test Methods** Suppliers **shall** use the test methods described in Appendix C for any parameter, feature or function for which a test method is given in Appendix C or in this section.

For parameters, features or functions for which no test method is given in Appendix C or this section, the supplier may use their own test method. This test method **shall** be sufficiently described in the test report so that a user can duplicate the test methods and conditions.

**5.1.4 Test Conditions and Limits** All test limits **shall** be at the minimum and maximum operating limits given in the device's specification.

**5.1.5 DVT Report** A report of the DVT **shall** be prepared. The DVT report **shall**:

- Provide the dates and locations of the design verification testing.
- List the serial numbers (if available), date codes and revision levels (both hardware and firmware) of the devices being tested.

- List the parameter, feature or function being tested.
- Provide a description or reference to the test method.
- Give the limits of the test.
- Provide the results of the test for each device tested. Tests providing parametric data, such as output voltage regulation, **shall** give the actual measured results of the test and not just ''Pass/Fail.''
- Provide the results of failure mode analysis for all failures in DVT and the correction action for each DVT failure.
- Provide for each parameter, feature or function tested a statement of ''Pass'' if all of the tested devices meet the specification or ''Fail'' if any of the devices did not meet the specification (one device failing any test is counted as a DVT failure).
- Give a statement that the device passed DVT if all tested units meet all specifications or that the device failed DVT if any tested device did not meet specification for any tested parameter, feature or function.

It is left to the supplier's discretion on whether or not to supply all or part of the DVT report to any particular customer.

### 5.1.6 Design Verification Testing - ac Input Parameters

**5.1.6.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.6.2 Parameters to Be Measured** DVT on a device operating from an ac power source **shall**, at a minimum, test all of the following parameters:

- Input current as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Input power as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Inrush current (The peak value and oscillograms of the inrush current from the application of power until the inrush current transient is complete **shall** be recorded. At least one oscillogram **shall** have a time resolution to show no less than one half cycle per division of the oscilloscope display.)
- Input current harmonics and power factor as a function of input voltage and output load.
- Input voltage at which the device becomes operational and the input voltage at which the device turns off.
- Hold-up time.

### 5.1.7 Design Verification Testing - dc Input Parameters

**5.1.7.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.7.2 Parameters to Be Measured** DVT on a device operating from a dc power source **shall**, at a minimum, test all of the following parameters:

- Input current as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Input power as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Input voltage at which the device becomes operational and the input voltage at which the device turns off.

### 5.1.8 Design Verification Testing - Overall Input to Output Parameters

**5.1.8.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.8.2 Parameters to Be Measured** DVT on all PCDs **shall**, at a minimum, test the following:

- Efficiency as a function of input voltage and output loading.
- Turn on delay time of each output.
- Ability to start and operate with the minimum specified output load.
- Start up at minimum and maximum specified ambient or baseplate temperatures.

### 5.1.9 Design Verification Testing - dc Output Parameters

**5.1.9.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.9.2 Parameters to Be Measured** The following parameters are the minimum that **shall** be tested on each sample:

- Load regulation (each output individually).
- Cross regulation.
- Line regulation.
- Temperature regulation.
- Short term (24 hour) output voltage drift.
- PARD on each output.
- Dynamic output voltage response to output load changes (maximum deflection and recovery time as a function of the magnitude and rate of output current change).
- Voltage rise time on each output.
- For devices with more than one output, the time delay and rise time of all relative to the other outputs.

**5.1.10 Design Verification Testing - Protection Features** Protection features are those features and functions intended to prevent damage, degradation or loss of data. Examples of protection features include circuits that:

- Prevent excessive output voltage (output overvoltage protection).
- Send an alarm or stop power conversion when the output voltage is less than the minimum specified value of the output undervoltage protection (UVP).
- Stop power conversion or disconnect the device from the source when the input voltage exceeds the maximum specified value of the input overvoltage protection (OVP).
- Respond to excessive output current by stopping power conversion or limiting the output current to a specified value of the output overcurrent protection (OCP).
- Stop power conversion when the ambient or internal temperature of the device exceeds limits determined by the supplier of the overtemperature protection (OTP).

**5.1.10.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.10.2 Parameters to Be Measured** For each protection feature or function, the minimum tests **shall** include:

- The voltage, current, temperature, power or other condition that causes the detector circuit to indicate an abnormal condition.
- The device's response to the detection of the abnormal condition.
- If applicable, the voltage, current, temperature, power or other condition that causes the detector circuit to indicate a return to normal operation.
- If applicable, the device's behavior during the change from an abnormal operating condition to normal operation.
- If applicable, the means or method used to reset a device that has shut down in response to an abnormal condition.

#### 5.1.11 Design Verification Testing - Input and Output Signals and Indicators

**5.1.11.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.11.2 Parameters to Be Measured** For all signals and indicators, all parameters given in the product specification **shall** be verified. This includes, but is not limited to:

- Conditions and criteria that cause a signal or indicator to be asserted, to be negated, or to change state.
- Signal electrical levels.
- Signal and indicator timing.

#### 5.1.12 Design Verification Testing - Other Electrical Parameters, Features and Functions

**5.1.12.1 Current Sharing** The tests in this section **shall** be applied to all devices whose specifications indicate that the outputs can be connected in parallel.

**5.1.12.1.1 Test Conditions** Sample units **shall** be connected and configured according to the supplier's instructions for current sharing operation.

At the minimum, the tests below **shall** be performed at all combinations of:

- Minimum, nominal and maximum ambient or baseplate temperature.
- Minimum, nominal and maximum input voltage.

**5.1.12.1.2 Test Procedure** All testing **shall** be performed according to the methods described in Appendix C. Specifically, for Current Sharing, see Appendix C-4.17.

**5.1.12.2 Design Verification Testing - Hot Swap** The tests in this section **shall** be applied to all devices whose specifications describe them as suitable for insertion into and removal from an energized system.

**5.1.12.2.1 Test Conditions** The test fixture is configured to hold at least two devices operating in parallel.

For standard product, the device manufacturer **shall** specify the text fixture used for hot swap testing. For custom devices, the test fixture **shall** utilize the customer end application equipment as much as possible to provide the maximum possible assurance that there is no hot swap problem in the end application.

The input voltage source is set to the nominal value. The ambient temperature is set to 25 °C ± 3 °C.

**5.1.12.2.2 Test Procedure** All testing **shall** be performed according to the methods described in Appendix C. Specifically, for Hot Swap, see Appendix C-4.18.

**5.1.13 Design Verification Testing - Mechanical Compliance** DVT **shall** include a mechanical compliance test. The supplier **shall** make dimensional measurements on at least three samples of a device.

The test report **shall** include a brief description of each measurement (such as ‘‘overall length’’), the specified dimension and tolerance from the specification, mechanical design file or drawing, and the results of the measurement, and a statement of whether the measured values are, or are not, within the tolerances allowed on the design file or drawing. All dimensions on all devices **shall** be within tolerance for this test to be passed. One dimension on any sample that is out of tolerance **shall** be considered a failure of this test.

**5.2 Environmental Stress Testing (EST)** This section refers to testing and qualification related to the operating environment, such as temperature and humidity; not to environmental requirements such as RoHS.

**5.2.1 EST Purpose** The purpose of the environmental stress testing is to demonstrate a minimum ability of the product to withstand steady-state and changing temperature, humidity, input power and output loading without damage or degradation.

This testing, by itself, cannot assure a minimum reliability or product life as those calculations require detailed knowledge of the product's operating conditions. It is up to each user to use the stresses described here and their knowledge of the end use environment to determine whether a product meeting this standard will perform adequately in the end use.

**5.2.2 Test Sequence for EST** Each of the tests in this section is to be considered stand-alone. The tests may be performed in any order convenient to the supplier.

The supplier is permitted, but not required to use different physical samples for each of the environmental stress tests.

**5.2.3 Highly Accelerated Life Test (HALT)** HALT **shall** be performed on completed standard PCDs. Additional information on HALT may be found in Appendix D.1. Specific HALT test procedures **shall** be AABUS. HALT testing on custom PCDs **shall** be AABUS.

**5.2.3.1 Scope and Purpose** The purpose of HALT is to assure there is some margin to specified stress levels and as a means to find weaknesses in designs for corrective action prior to design release.

It is specifically not the purpose of HALT to predict reliability (failure rate) or service life.

It is strongly recommended that HALT be performed as early in the design cycle as possible. HALT gives the best results when problems that are found, can be corrected well before the rest of the qualification testing.

**5.2.3.2 Sample Size** The minimum sample size for this test **shall** be 12 (see Note 1) per Table 5-1.

**Table 5-1 Minimum Sample Size for HALT Tests**

| | Input Voltage Operating and Destruct Test | Output Load Operating and Destruct Test | Temperature Operating and Destruct Test | Combined Environment (Temperature and Vibration) Operating and Destruct Test |
|---|---|---|---|---|
| All Classes and Categories | 3 | 3 | 3 | 3 |

**Note 1:** For Categories 1 and 3 (Power Supplies/Adapters), users have the option of starting with less than 12 samples and re-using samples which survive a given sequence of testing. Users are cautioned that some HALT failures require extensive repairs after failures during early testing and may not be suited for subsequent testing. Category 2 (BMPM) must begin with 3 new units for each test sequence.

**5.2.3.3 Test Procedure Guidance** In general, the HALT process is to apply increasing levels of stress until the device fails. All failures are analyzed for the root cause. If the failure is not from an unrealistic overstress, such as a semiconductor rated at 150 °C junction temperature failing at a junction temperature of 200 °C, then the design, component or material **shall** be changed to eliminate the observed failure mode. It is acknowledged that there is some engineering judgment involved in determining whether a failure in HALT is due to an unrealistic overstress or requires a change in the design.

Once a failure mode is identified, the corrective action is applied and the HALT continues. This process of test to failure, analyze, correct as appropriate and continue HALT proceeds until all failure modes except those from unreasonable overstress are found and eliminated.

Stresses applied in HALT typically start at the limits of rated operation and increase or decrease beyond the rated operation limits. The stresses that are typically applied during HALT include, but are not limited to:

- Input voltages exceeding the rated maximum.
- Input voltages less than the rated minimum.
- Cycling of the input power on and off.
- Ambient or baseplate temperatures higher than the maximum rated value.
- Ambient or baseplate temperatures less than the minimum rated value.
- Output currents in excess of the maximum rated value.
- Operation with no load on the output.
- Periodic and random application of short circuits to the output.
- Random or swept sine vibration over bandwidths and total accelerations exceeding the rated operation.
- Periodic and random shock at accelerations greater than the maximum rated.

These stresses may be applied one by one but HALT testing typically includes applying multiple stresses simultaneously.

HALT test plans compliant to this document **shall** include simultaneous application of input power cycling, stepping of input voltage, output load, ambient or baseplate temperature and vibration. Stresses should be stepped to failure or to the limits of the test equipment (beyond product specification limits).

HALT is normally performed in an environmental chamber. It **shall** be possible to vary device input and output levels outside of those specified for normal device operation while controlling temperature, and separately and simultaneously applying vibration to the units under test. Repetitive shock or electrodynamic vibration equipment may be used. During HALT, the device **shall** be powered up and operated, and **shall** be monitored continuously to ensure functionality. Test setups **shall** be optimized to maximize functional test coverage. The test setup should also allow for remote operation of the test and product from outside of the environmental chamber.

Suppliers **shall** provide upon request, their specific stress test plans and results to the PCD user as part of the reports required in 3.2. See Appendix D for more detail on HALT.

### 5.2.4 Temperature, Humidity and Bias (THB)

**5.2.4.1 Purpose** The THB test is used to test for moisture induced failures such as conductive anodic filaments (CAF), corrosion and dendrites.

**5.2.4.2 Applicability** This test is applicable to Class II standard products. It is applicable AABUS for Class I standard and Classes I and II custom products.

**5.2.4.3 Sample Size** The minimum sample size for this test **shall** be as per Table 5-2.

**Table 5-2 Minimum Sample Size for THB Tests**

| | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/ Chargers) |
|---|---|---|---|
| Class I | 3 | 5 | 3 |
| Class II | 6 | 30 | 6 |

**5.2.4.4 Test Procedure** The THB test starts with a pre-conditioning soak of all units for 72 hours under the following conditions:

- Unpowered.
- Ambient temperature: 85 °C.
- Relative humidity: 85%.

The THB testing is performed for 1000 hours under the following conditions:

- Input voltage: Rated maximum continuous input voltage.
- Output loading (all outputs): Minimum rated.
- Ambient temperature: The maximum rated ambient temperature or 85 °C, whichever is less.
- Relative Humidity: 85%.

For BMPM, natural convection is preferred, but the minimum forced air cooling is allowed if necessary to prevent the device's specified baseplate or hot spot temperature exceeding rated maximum temperature. If forced air is used, then the device's baseplate or hotspot temperature **shall** be as close to the maximum rating, as possible.

During the testing, the units **shall** be monitored for proper functioning. The monitoring may either be continuous or sampled at a rate no less frequently than once a minute.

**5.2.4.5 Pass Criteria** At the conclusion of the test time, all tested units **shall** be visually inspected and **shall** be free of solder joint cracking, corrosion, dendrites, or other defects.

All tested units **shall** pass a functional test.

It is permitted to remove the units from the test and visually inspect and functionally test them at times less than the 1000 hour minimum. If failures are detected, then corrective action **shall** be implemented and the test restarted from the beginning. No credit is given for any completed unit-hours. Fresh units may be used for the restarted test.

### 5.2.5 High Temperature Operating Bias (HTOB)

**5.2.5.1 Purpose** This test is to find weaknesses that appear only after long operation times (not infant mortality). This test is not intended to test or prove product life.

**5.2.5.2 Applicability** This test is applicable to Class II standard products. It is applicable AABUS for Class I standard and Classes I and II custom products.

**5.2.5.3 Sample Size** The minimum sample size for this test **shall** be as per Table 5-3.

**Table 5-3 Minimum Sample Size for HTOB Tests**

| | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/ Chargers) |
|---|---|---|---|
| Class I | 3 | 5 | 3 |
| Class II | 6 | 30 | 6 |

**5.2.5.4 Procedure** There is no pre-conditioning for this test.

The units under test are operated under the following conditions:

- Input voltage: For devices that operate from ac source power, the input voltage **shall** be equal to the highest rated nominal value (For example, with most ac to dc power supplies, the input voltage will be 240 Vac). For board mounted dc to dc converters, the test **shall** start with the input voltage equal to the highest rated continuous operating voltage. After one hour, for the second cycle, the input voltage **shall** be equal to the minimum rated continuous operating voltage. The input voltage **shall** then alternate every hour between the highest and lowest rated continuous operating voltage until the test is complete.
- Output loading (all outputs): 95% ± 5% of rated maximum.
- Ambient temperature: For packaged power devices, the ambient temperature **shall** be the maximum rated temperature. For board mounted power devices, the ambient temperature **shall** be adjusted so that the device's baseplate or hot spot temperature is at the maximum rated value. For devices with natural convection cooling, they **shall** be oriented in the most unfavorable position (typically horizontal mounting).

- Relative humidity: Not specified.

The input power to the units under test is turned on and off over a one hour cycle as follows:

- On: 42 minutes.
- Off: 1 minute.
- On: 1 minute.
- Off: 1 minute.
- On: 1 minute.
- Off: 1 minute.
- On: 1 minute.
- Off: 1 minute.
- On: 1 minute.
- Off: 10 minutes.

The minimum test time is the same for all product types (BMPM and packaged power) and varies with product class:

- Class I: 500 hours minimum.
- Class II: 1000 hours minimum.

During the testing, the units **shall** be monitored either continuously or **shall** be sampled no less frequently than once every minute.

**5.2.5.5 Pass Criteria** At the conclusion of the test time, all tested units **shall** be visually inspected and **shall** be free of solder joint cracking, corrosion, dendrites, or other defects.

All tested units **shall** pass a functional test.

It is permitted to remove the units from the test and visually inspect and functionally test them at times less than the minimum. If failures are detected, then corrective action **shall** be implemented and the test restarted from the beginning. No credit is given for any completed unit-hours. Fresh units may be used for the restarted test.

### 5.2.6 Temperature Cycling Test

**5.2.6.1 Purpose** The purpose of this test is to find weaknesses in solder joints, glued interfaces and other parts that are stressed by differences in the coefficient of thermal expansion (CTE).

**5.2.6.2 Applicability** This test is applicable to Class II standard products. It is applicable AABUS for Class I standard and Classes I and II custom products.

**5.2.6.3 Sample Size** The minimum sample size for this test **shall** be as per Table 5-4.

**5.2.6.4 Procedure** The temperature cycling test **shall** be performed under the following conditions:

- Units **shall** be unpowered.
- The minimum rate of change of ambient temperature is 20 °C/min.
- The dwell time at either temperature limit for devices with lead-based or lead-free solder **shall** be 30 minutes.
- The minimum number of cycles **shall** be as per Table 5-5.
- The temperature limits **shall** be as per Table 5-6.

**Table 5-4 Sample Sizes for Temperature Cycling Tests**

| | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/ Chargers) |
|---|---|---|---|
| Class I | 3 | 5 | 3 |
| Class II | 6 | 30 | 6 |

**Table 5-5 Minimum Number of Cycles for Temperature Cycling Tests**

| | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/ Chargers) |
|---|---|---|---|
| Class I | 300 | 300 | 300 |
| Class II | 700 | 700 | 700 |

**Table 5-6 Temperature Limits for Temperature Cycling Tests**

| | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/ Chargers) |
|---|---|---|---|
| Class I or Class II | Minimum Rated Storage Temperature to Maximum Rated Storage Temperature | -40 °C ± 3 °C to +125 °C ± 3 °C | Minimum Rated Storage Temperature to Maximum Rated Storage Temperature |

**5.2.6.5 Pass Criteria** All devices under test **shall** pass a visual and functional test after:

- 300 cycles for Class I product.
- 700 cycles for Class II product.

More frequent visual and functional testing, such as after 500 cycles for Class II product, is permitted. If failures are detected, then corrective action **shall** be implemented and the test restarted from the beginning. No credit is given for any completed unit-hours. Fresh units may be used for the restarted test.

### 5.2.7 Power and Temperature Cycling Test

**5.2.7.1 Purpose** The purpose of this test is to detect design weaknesses that are exposed at the corners of the operating conditions.

**5.2.7.2 Applicability** This test is applicable to Class II standard products. It is applicable AABUS for Class I standard and Classes I and II custom products.

**5.2.7.3 Sample Size** The minimum sample size for this test **shall** be per Table 5-7.

Table 5-7 Minimum Sample Size for Power and Temperature Tests

| | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/ Chargers) |
|---|---|---|---|
| Class I or Class II | 3 | 3 | 3 |

**5.2.7.4 Procedure** The power and temperature cycling test **shall** be performed under the following conditions:

- Input voltage: Maximum continuous rated.
- Output load (all outputs): 50% of rated maximum.
- The minimum number of cycles is 15.
- The minimum number of unit-cycles is 300. (One unit-cycle is one unit tested for one temperature and power cycles, as defined below.)

The temperature limits are the same for Class I and Class II product.

The minimum and maximum test temperatures **shall** be the minimum and maximum rated operating temperatures.

Each temperature and power cycle consist of seven steps, as per Table 5-8.

Table 5-8 Steps Required for Power and Temperature Cycling Tests

| Step | Power | Temperature |
|---|---|---|
| 1 | On | Ramp from minimum to maximum |
| 2 | On | Dwell at maximum for 30 minutes |
| 3 | Off/On | Power Cycle once at maximum temperature |
| 4 | Off | Ramp from maximum to minimum |
| 5 | Off | Dwell at minimum for 30 minutes |
| 6 | On | Power up at minimum temperature |
| 7 | Loop back to Step 1 | |

**5.2.7.5 Pass Criteria** At the conclusion of the test time, all tested units **shall** be visually inspected and **shall** be free of solder joint cracking, corrosion, dendrites, or other defects.

All tested units **shall** pass a functional test.

It is permitted to remove the units from the test and visually inspect and functionally test them at times less than the minimum. If failures are detected, then corrective action **shall** be implemented and the test restarted from the beginning. No credit is given for any completed unit-hours. Fresh units may be used for the restarted test.

### 5.2.8 Shock and Vibration

**5.2.8.1 Purpose** Shock and vibration testing is intended to provide some assurance that a device will not be damaged or degraded in the course of normal handling, transportation and use.

**5.2.8.2 Testing Overview** Shock and vibration testing is applied to simulate the following environments for the PCDs:

- A device installed in the end application (operating shock and vibration)..
- A device in its shipping packaging and being handled, such as in a manufacturing process or field service operation (nonoperating)
- A device being handled in its shipping packaging, such as during a loading or unloading operation (nonoperating, drop test).
- A device in its shipping packaging and being transported (nonoperating).

These tests vary from each other both in method and severity.

**5.2.8.3 Test Sequence** Each of the tests in this section is to be considered stand-alone. The tests may be performed in any order convenient to the supplier.

The supplier is permitted, but not required, to use different physical samples for each of the shock and vibration tests.

**5.2.8.4 Pass Criteria** Unless otherwise specified below, all test samples **shall** pass a functional test at the completion of the test. In addition to the functional test at the completion of the test, some tests may require monitoring the device while under test. If monitoring is required, each power and signal output of each unit under test **shall** be monitored continuously during the test. The units under test **shall** operate within specification during the entire test. Sampling at greater than 1 millisecond periods is not permitted.

**5.2.8.5 Test Equipment** All shock and vibration testing will be done with an electrodynamic shaker. The use of a repetitive shock table is not permitted as a substitute.

**5.2.8.6 Device Mounting** Devices **shall** be mounted to the shaker table according the IEC 60068-2-27, *Environmental testing - Part 2-47: Test - Mounting of specimens for vibration, impact and similar dynamic tests.*

### 5.2.9 Random Vibration - Operating

**5.2.9.1 Purpose** The purpose of this test is to provide assurance that the device can operate without interruption or degradation during vibration encountered during normal operation.

**5.2.9.2 Applicability** This test is applicable to all classes and categories of product.

**5.2.9.3 Sample Size** For all product classes and categories, the minimum number of samples **shall** be 3 devices.

**5.2.9.4 Test Method** The devices **shall** be tested per the methods described in IEC 60068-2-64, *Environmental testing - Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance.*

The Accelerated Spectral Density (ASD) **shall** be 0.04 $g^2$/Hz from 20 Hz to 1000 Hz. From 1000 Hz to 2000 Hz, the ASD **shall** decrease by 6 db/octave, to 0.01 $g^2$/Hz (see Figure 5-1).

The total acceleration is approximately 8 g rms.

Each device **shall** be tested in three axes for a minimum of 10 minutes per axis. The device **shall** be powered for the duration of the test at nominal input voltage and no load.

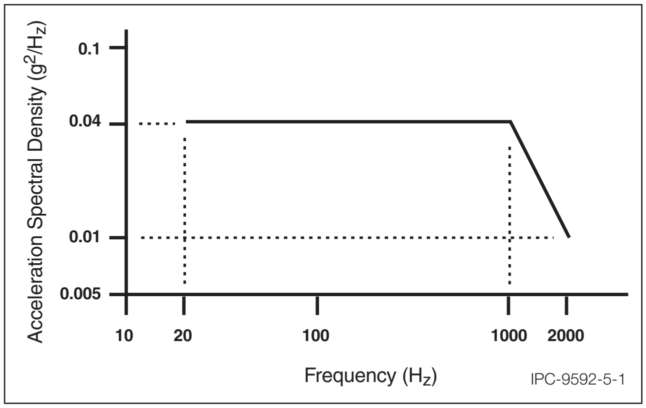


**Figure 5-1 Operating Vibration Test: Acceleration vs. Frequency**

**5.2.9.5 Pass Criteria** Each power and signal output of each unit under test **shall** be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted.

The units under test **shall** operate within specification during the entire test.

### 5.2.10 Random Vibration - Nonoperating

**5.2.10.1 Purpose** The purpose of this test is to provide assurance that products in their shipping package will not suffer damage or degradation during transport.

**5.2.10.2 Applicability** This test is applicable to all classes and categories of product.

**5.2.10.3 Sample Size** For all product categories and product classes, the minimum number of samples **shall** be a minimum of 3 devices packaged in their fully populated, bulk shipping package or individual packages of product.

**5.2.10.4 Test Method** The devices **shall** be tested per the methods described in IEC 60068-2-64, *Environmental testing - Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance.* The products are in the shipping packaging for this test.

Each shipping package **shall** be tested in three axes for a minimum of 10 minutes per axis.

The ASD **shall** be 0.05 $g^2$/Hz from 5 Hz to 1000 Hz. From 1000 Hz to 2000 Hz the ASD **shall** decrease by 6 db/octave, to 0.0125 $g^2$/Hz (see Figure 5-2).

The total acceleration is approximately 9 g rms.

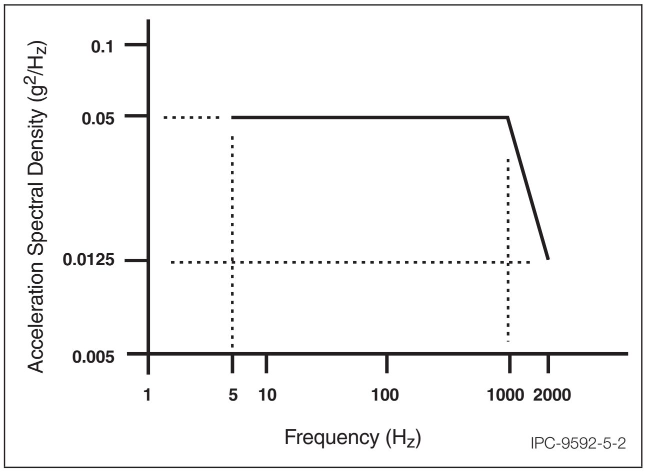


**Figure 5-2 Nonoperating Vibration: Acceleration vs. Frequency**

**5.2.10.5 Pass Criteria** At the conclusion of all three axes of testing, the products **shall** be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed.

All units **shall** also pass a functional test.

There are no requirements on the condition of the shipping package.

### 5.2.11 Shock - Operating

**5.2.11.1 Purpose** The purpose of this test is to provide assurance that the device can operate without interruption or degradation during shock encountered during normal operation.

**5.2.11.2 Applicability** This test is applicable to all classes and categories of product.

**5.2.11.3 Sample Size** For all product types and product classes, the minimum number of samples **shall** be three (3) devices.

**5.2.11.4 Test Method** The devices **shall** be tested per the methods described in IEC 60068-2-27, *Environmental Testing - Part 2.27 Test Ea and guidance: Shock.*

Each tested device **shall** be exposed to three shocks in each of three axes. The amplitude of each shock **shall** be no less than 30 g with a half sine wave shape and a duration of 16 ms.

**5.2.11.5 Pass Criteria** Each power and signal output of each unit under test **shall** be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted.

The units under test **shall** operate within specification during the entire test.

### 5.2.12 Free Fall

**5.2.12.1 Purpose** The purpose of this test is to provide assurance that unpackaged products will not suffer damage or degradation during handling and mishandling.

**5.2.12.2 Applicability** This test is applicable to all classes and categories of product.

**5.2.12.3 Sample Size** For all product types and product classes, the minimum number of samples **shall** be three (3) devices.

**5.2.12.4 Test Method** The devices **shall** be tested per the methods described in IEC 60068-2-32, *Environmental Testing - Part 2.32 Test Ed: Freefall, Procedure 1.*

BMPM devices **shall** be held on one corner of the device before being allowed to fall. Devices **shall** be held with the side that normally faces down, facing down, before being allowed to fall.

The height of the fall varies with the weight of the device, as per Table 5-9.

**Table 5-9 Height of Fall for Free Fall Testing**

| Device Weight (gms) | Fall Height (mm) |
|---|---|
| 0 - 10.0 | 1000 |
| 10.1 - 20.0 | 500 |
| 20.1 - 50.0 | 250 |
| 50.1 - 100.0 | 100 |
| 100.1 - 200 | 50 |
| >200 | 25 |

**5.2.12.5 Pass Criteria** At the conclusion of free fall testing, the device **shall** be visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed.

All units **shall** also pass a functional test.

### 5.2.13 Drop Test

**5.2.13.1 Purpose** The purpose of this test is to provide assurance that products in their shipping package will not suffer damage or degradation during handling or mishandling.

**5.2.13.2 Applicability** This test is applicable to all classes and categories of product.

**5.2.13.3 Sample Size** For all product types and product classes, the minimum number of samples **shall** be one (1) full shipping container. Each sample **shall** consist of the smallest shipping container for that product, completely filled with product.

For example, an ac to dc power supply may have its own shipping carton with foam packing material. In this case, the sample is one power supply in its shipping carton. Smaller products, such as some packaged power products and most board mounted power products, are often shipped in containers containing several products. In this case, the sample is the multi-pack container completely filled with product.

**5.2.13.4 Test Method** The test method is intended to show that a product which is dropped and falls in any possible way will not be damaged. It is specifically not the intent of this test to show that the packaged product can survive without damage or degradation after a large number of drops.

The sample **shall** be dropped once on:

- Each face (6 drops).
- Each edge (12 drops).
- Each corner (8 drops).

The total number of drops is 26.

The drop height is 1 m.

The supplier is permitted to place the product in fresh packaging after 13 drops. This is consistent with the intent to test the various ways the package can fall and not be an endurance test of the packaging.

**5.2.13.5 Pass Criteria** The testing **shall** be stopped if there is any evidence that the product has been damaged. An example of such evidence is the sound of a loose component rattling around inside the package. If the testing is stopped before the 26 drops are completed, a failure analysis of the packaging and the product **shall** be performed and corrective action taken. The test **shall** then be started again from the beginning.

If all 26 drops are completed with no evidence that the product has been damaged, the units are unpackaged and all units in the package are:

- Visually inspected for damage or deformation that would affect the integrity, reliability or safety of the product.
- Given the appropriate hi-pot test.
- Given a functional test.

All units **shall** pass all of these tests for the test to be considered passed.

### 5.2.14 Other Environmental Stress Testing

**5.2.14.1 Corrosion Resistance** This section refers to corrosion testing such as a mixed flowing gas test. Such corrosion testing is not required by this standard. (Note: In a future revision, it is possible that such corrosion testing may be required.)

This specifically does not exclude looking for corrosion induced during any other testing, such as the High Temperature Bias test, required by this document.

**5.2.14.2 Dust Resistance** Dust resistance testing is only required for unpotted Class II products. This test is a type test and need only be performed on one representative sample of a family of products.

Dust resistance testing **shall** be performed according to Telcordia GR-1274-CORE, *Generic Requirements for Reliability Qualification Testing of Printed Wiring Assemblies Exposed to Airborne Hygroscopic Dust.*

### 5.2.14.3 SMT Attachment Reliability

**5.2.14.3.1 Purpose** The purpose of this test is to provide assurance that a surface mounted PCD will not detach or disconnect from the board to which it is mounted during its service life. The solderability and wettability of the PCD's SMT leads are tested per IPC/ECA J-STD-002, as referred in IPC-9701.

It is not the purpose of this test to test the attachment of components used in the construction of the PCD to the PCD's substrate.

**5.2.14.3.2 Applicability** This test applies to all Class I and Class II board mounted power conversion devices that are surface mounted.

This test is a type test. This test need only be performed on one model representative of a family of devices. For the purposes of this test, and only for the purposes of this test, a family is defined as PCDs that have the:

- Same module dimensions.
- Same lead design (material, dimensions, finish).
- Same number of leads and pitch.
- Same substrate material, number of layers, surface finish.
- Same module encapsulation material (if applicable).
- Same solder joint configuration (pad size, solder paste composition, etc.).
- Same manufacturer and assembly process.
- Same package component density (package coverage area/substrate area).

Thermal cycle test results can be extended from the tested module to those within its family, as defined above, and to modules with smaller overall dimensions and/or lower component densities satisfying the remaining family characteristics. Test exemption requirements as defined in IPC-9701, Table 4-3, also apply.

**5.2.14.3.3 Sample Size** The minimum number of samples **shall** be as detailed in IPC-9701.

**5.2.14.3.4 Test Method** The devices **shall** be tested per the methods as detailed in IPC-9701.

The minimum temperature, maximum temperature and number of cycles **shall** be chosen by the supplier from the Temperature Cycling Requirements table of IPC-9701. The temperature limits and number of thermal cycles **shall** be chosen such that the cumulative stress is no less than the preferred limits in the table, TC-1 (Minimum temperature: 0 °C, Maximum temperature: 100 °C) and NTC-E (6000 cycles).

The pins of all devices on one test board **shall** be connected in a daisy-chain manner. During testing the continuity of the daisy chain connection **shall** be continuously monitored. If a connection fails open during the test, information to uniquely identify the connection (such as Device 4, Pin 3) and time to failure **shall** be recorded. The failed connection may be repaired and the test continued until the minimum number of thermal cycles has been completed.

At the conclusion of the thermal cycling, all units **shall** be subjected to a ''dye and pry'' test. The solder joints are to be examined and any evidence of cracking or other degradation **shall** be recorded. There is no pass or fail criteria for the ''dye and pry'' but suppliers are expected to make use of the information to make improvements in design and process where possible.

**5.2.14.3.5 Pass Criteria** All devices **shall** complete 60% of the number of thermal cycles without an open circuit connection. The pass criteria for failures that occur after 60% of the minimum number of thermal cycles **shall** be AABUS.

### 5.2.14.4 Through Hole Pin Solderability

**5.2.14.4.1 Purpose** The purpose of this test is to provide assurance that pins used in board mounted PCDs for through-hole connections will properly solder and attach to the circuit board to which they are to be mounted.

**5.2.14.4.2 Applicability** This test applies to all Category 2 devices with through-hole mounting.

This test is a family test. It is only required for a representative sample (or samples, as necessary) of a given family of devices. It is not required that this test be performed on every model of a family of PCDs.

**5.2.14.4.3 Sample Size** The minimum number of samples for this test is five (5) devices.

**5.2.14.4.4 Test Method** The PCD **shall** be tested per IPC/ECA J-STD-002, Test A (''dip and look'').

**5.2.14.4.5 Pass Criteria** After being dipped in solder, the pins **shall** be visually inspected and **shall** meet the requirements of IPC/ECA J-STD-002.

### 5.3 Electromagnetic Susceptability (EMS) and Other Tests

#### 5.3.1 Conducted Continuous Wave

**5.3.1.1 Purpose** Passing this test offers some assurance that conducted RF interference on input power lines will not disrupt the operation of the device.

**5.3.1.2 Applicable Devices** This test is applicable to all Category 1 (power supplies) and Category 3 (adapters/chargers) devices, but is not applicable to Category 2 (board mounted power module) devices.

**5.3.1.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.1.4 Test Method** The device **shall** be tested according to the methods described in IEC 61000-4-6, *Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques - Section 6: Immunity to conducted disturbances, induced by radio-frequency fields.*

**5.3.1.5 Pass Criteria** The device **shall** meet the performance levels in Table 5-10 when tested with the test severity level listed in the first column.

**Table 5-10 Required Performance Levels for Conducted Continuous Wave Testing**

| Test Severity Level | Performance Level for Product Class | |
|---|---|---|
| | Class I | Class II |
| Level 1 | Perf. Level A | Perf. Level A |
| Level 2 | Perf. Level A | Perf. Level A |
| Level 3 | Perf. Level B | Perf. Level A |

The Performance Level ratings of A through D are considered after the device has been tested and where Level A indicates that the device performs normally after the test, but Level D indicates that the device has been damaged beyond repair after the test exposure (see 2.4 for the definitions of Performance Level ratings A through D).

The test severity levels are defined in IEC-61000-4-6, where Test Severity Level 1 is least severe and Test Severity Level 3 is most severe.

#### 5.3.2 Radiated Immunity

**5.3.2.1 Purpose** Passing this test offers some assurance that ambient RF radiation will not disrupt the operation of the device.

**5.3.2.2 Applicable Devices** This test is applicable to all Category 1 and Category 3 devices.

**5.3.2.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.2.4 Test Method** The device **shall** be tested according to the methods described in IEC 61000-4-3, *Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test.*

**5.3.2.5 Pass Criteria** The device **shall** meet the performance levels in Table 5-11 when tested with the test severity level listed in the first column.

**Table 5-11 Required Performance Levels for Radiated Immunity Testing**

| Test Severity Level | Performance Level for Product Class | |
|---|---|---|
| | Class I | Class II |
| Level 1 | Perf. Level A | Perf. Level A |
| Level 2 | Perf. Level A | Perf. Level A |
| Level 3 | Perf. Level B | Perf. Level A |

#### 5.3.3 Conducted Electrical Fast Transient (EFT)

**5.3.3.1 Purpose** Passing this test offers some assurance that conducted electrical fast transient noise on input power lines will not disrupt the operation of the device.

**5.3.3.2 Applicable Devices** This test is applicable to all Category 1 and Category 3 devices.

**5.3.3.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.3.4 Test Method** The device **shall** be tested according to the methods described in IEC 61000-4-4, *Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques - Section 4: Electrical fast transient/burst immunity test.*

**5.3.3.5 Pass Criteria** The device **shall** meet the performance levels in Table 5-12 when tested with the test severity level listed in the first column.

**Table 5-12 Required Performance Levels for Conducted Electrical Fast Transient Testing**

| Test Severity Level | Performance Level for Product Class | |
|---|---|---|
| | Class I | Class II |
| Level 1 | Perf. Level A | Perf. Level A |
| Level 2 | Perf. Level A | Perf. Level A |
| Level 3 | Perf. Level C | Perf. Level B |
| Level 4 | N/A | N/A |

### 5.3.4 Conducted Surges

**5.3.4.1 Purpose** Passing this test offers some assurance that conducted surges on input power lines will not disrupt the operation of the device.

**5.3.4.2 Applicable Devices** This test is applicable to all Category 1 and Category 3 devices.

**5.3.4.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.4.4 Test Method** The device **shall** be tested according to the methods described in IEC 61000-4-5, *Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques - Section 5: Surge immunity test.*

**5.3.4.5 Pass Criteria** The device **shall** meet the performance levels in Table 5-13 when tested with the test severity level listed in the first column.

**Table 5-13 Required Performance Levels for Conducted Surges Testing**

| Test Severity Level | Performance Level for Product Class | |
|---|---|---|
| | Class I | Class II |
| Level 1 | Perf. Level A | Perf. Level A |
| Level 2 | Perf. Level A | Perf. Level A |
| Level 3 | Perf. Level B | Perf. Level B |
| Level 4 | N/A | Perf. Level C |

### 5.3.5 Ring Waves

**5.3.5.1 Purpose** Passing this test offers some assurance that conducted surges on input power lines will not disrupt the operation of the device.

**5.3.5.2 Applicable Devices** This test is applicable to all Category 1 and Category 3 devices.

**5.3.5.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.5.4 Test Method** The device **shall** be tested according to the methods described in IEC 61000-4-12, *Electromagnetic compatibility (EMC) - Part 4-12: Testing and measurement techniques - Ring wave immunity test.*

**5.3.5.5 Pass Criteria** The device **shall** meet the performance levels in Table 5-14 when tested with the test severity level listed in the first column.

**Table 5-14 Required Performance Levels for Ring Waves Testing**

| Test Severity Level | Performance Level for Product Class | |
|---|---|---|
| | Class I | Class II |
| Level 1 | Perf. Level A | Perf. Level A |
| Level 2 | Perf. Level A | Perf. Level A |
| Level 3 | Perf. Level B | Perf. Level B |
| Level 4 | N/A | Perf. Level C |

### 5.3.6 Electrostatic Discharge - Packaged Power Devices

**5.3.6.1 Purpose** This test is to demonstrate that packaged power devices, when installed in the equipment in which they will be used, will not be disrupted or damaged by electrostatic discharges.

**5.3.6.2 Applicable Devices** This test is applicable to all Category 1 and Category 3 devices.

**5.3.6.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.6.4 Test Method** The devices **shall** be installed in the equipment with which they will be used according to the equipment manufacturer's instructions.

The device **shall** be tested according to IEC 61000-4-2, *Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test.* The discharges **shall** only be applied to exposed surfaces.

**5.3.6.5 Pass Criteria** The device **shall** meet the performance levels in Table 5-15 when tested with the test severity level listed in the first column.

**Table 5-15 Required Performance Levels for Electrostatic Discharge Testing - Packaged Power Devices**

| Test Severity Level | Performance Level for Product Class | |
|---|---|---|
| | Class I | Class II |
| Level 1 | Perf. Level A | Perf. Level A |
| Level 2 | Perf. Level A | Perf. Level A |
| Level 3 | Perf. Level A | Perf. Level A |
| Level 4 | Perf. Level B | Perf. Level B |

### 5.3.7 Electrostatic Discharge - Board Mounted Power Devices

**5.3.7.1 Purpose** This test is to demonstrate that board mounted power devices, when handled outside of the equipment in which they will be used, will not be damaged by electrostatic discharges.

**5.3.7.2 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.7.3 Test Method** The power device **shall** be tested according to the method described in JESD22-A114, *Electrostatic Discharge (ESD), Sensitivity Testing Human Body Model (HBM).*

**5.3.7.4 Pass Criteria** The device **shall** meet the minimum voltage as defined in Table 5-16.

**Table 5-16 Minimum Passing Voltage for Electrostatic Discharge Testing - Board Mounted Power Devices**

| | Class I | Class II |
|---|---|---|
| Test Voltage | 500V | 1 kV |

### 5.3.8 Power Line Disturbance Immunity

### 5.3.8.1 ac Input

**5.3.8.1.1 Purpose** This testing is to provide assurance that the device will operate properly and not be damaged when the input voltage drops out or sags.

**5.3.8.1.2 Applicability** This testing **shall** be applied to all Class I and Class II devices that operate from a single phase ac power source.

Testing of devices that operate from three phase ac power **shall** be AABUS.

**5.3.8.1.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.8.1.4 Conditions for All Tests** The device **shall** be operating with rated output load, an ambient temperature of 25 °C and for devices without self contained cooling, with the supplier's recommended minimum airflow for these operating conditions.

All tests **shall** be performed with the ac input voltage at the minimum and maximum rated nominal (e.g., 115Vac/230Vac).

**5.3.8.1.5 Short Term Input Undervoltage and Overvoltage** The device **shall** meet Performance Level A when the input voltage is changed by the following percentages for the given durations in Table 5-17. One ac line cycle is defined as 16.67 ms for 60Hz; 20ms for 50Hz. Tests in Table 5-17 **shall** be performed at nominal line frequencies of 50Hz and 60Hz using nominal line voltage references of 115Vac and 230Vac. Exception may be made when specified otherwise in the product specification.

**Table 5-17 Minimum Requirements to Meet Performance Level A When Device is Tested for Short Term Input Undervoltage and Overvoltage**

| Input Voltage Variation | Duration |
|---|---|
| -100% | 1/2 ac line cycle (Note 1) |
| -100% | 1 ac line cycle (Note 1) |
| -25% | 2 s |
| +20% | 2 s |

**Note 1:** Performance Level A required unless otherwise stated in data sheet.

**5.3.8.1.6 Input Undervoltage-Performance Level B** The device **shall** meet Performance Level B after the input voltage is reduced for all combinations of the voltage reductions and durations referenced in Table 5-18. Tests **shall** be conducted using nominal line voltage of 115Vac and 230Vac. Tests **shall** be conducted at 50Hz. (2 starting nominal voltages X 7 voltage reductions X 12 durations = 168 tests total).

**Table 5-18 Minimum Requirements to Meet Performance Level B When Device is Tested for Input Undervoltage (perform all combinations of % reduction and duration)**

| Input Voltage Reduction | Duration (ms) |
|---|---|
| 40%, 50%, 60%, 70%, 80%, 90%, 100% | 25, 40, 60, 90, 130, 200, 280, 400, 600, 900, 1300, 2000 |

**5.3.8.1.7 Immunity to Slow Reduction of Input Voltage** In this test, the input voltage is slowly reduced to 50% of the nominal input voltage and then slowly increased back to the nominal input voltage. During this change of input voltage, the device may continue to operate normally or it may shut down for an input undervoltage condition. If the device does shut down for an input undervoltage condition, it **shall** recover automatically to full operation when the input voltage is increased back to the normal operating range.

This test **shall** be performed for the input voltage at the minimum and maximum nominal values (115Vac/230Vac).

The input voltage **shall** be varied as follows:

- Starting at nominal input voltage, the input voltage **shall** be reduced at a rate of 3V per minute until the device shuts down for input undervoltage or the input voltage is equal to 50% of the nominal value.
- If the device shuts down, the input voltage **shall** be reduced at a rate of 12V per minute until the input voltage is equal to 50% of the nominal input voltage.
- The input voltage **shall** be held at 50% of the nominal for 1 minute.
- The input voltage will then be increased at a rate of 3V per minute.
- If the device continued to operate through the low voltage condition, then the voltage increase at 3V per minute will continue until the input voltage is equal to the nominal

value. If the device shut down during the voltage reduction and restarts during the time the voltage is being increased, the rate of increase of the input voltage **shall** be increased to 12V per minute as soon as the device restarts.

#### 5.3.9 Electromagnetic Emissions

**5.3.9.1 Devices with ac Input** This section applies only to devices that operate from an ac source.

AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.9.1.1 Conducted Emissions** The device **shall** be tested according to the methods defined in any referenced conducted emissions standards or specifications to which the device claims compliance in the device's specification and **shall** meet the specified emissions limits.

**5.3.9.1.2 Harmonic Input Current** The device **shall** be tested according to the methods defined in any referenced harmonic current emissions standards or specifications to which the device claims compliance in the device's specification and **shall** meet the specified harmonic current limits.

**5.3.9.1.3 Radiated Emissions** The device **shall** be tested according to the methods defined in any referenced radiated emissions standards or specifications to which the device claims compliance in the device's specification and **shall** meet the specified emissions limits.

**5.3.9.2 Packaged Power Devices with dc Input** This section applies to packaged power devices that operate from a dc source.

AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.9.2.1 Conducted Emissions** The device **shall** be tested according to the methods defined in any referenced conducted emissions standards or specifications to which the device claims compliance in the device's specification and **shall** meet the specified emissions limits.

**5.3.9.2.2 Radiated Emissions** The device **shall** be tested according to the methods defined in any referenced radiated emissions standards or specifications to which the device claims compliance in the device's specification and **shall** meet the specified emissions limits.

**5.3.9.3 Board Mounted Power Devices with dc Input** This section applies to board mounted power devices that operate from a dc source.

AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.9.3.1 Conducted Emissions** The device **shall** be tested according to the methods defined in EN 55022. A test report showing the results **shall** be made available upon customer request.

**5.3.9.3.2 Radiated Emissions** There are no requirements for measuring the radiated emissions of board mounted power devices that operate from a dc source.

#### 5.3.10 Acoustic Noise

**5.3.10.1 Purpose** The purpose of this test is to provide assurance that the device meets its specification for creating acoustic noise.

**5.3.10.2 Applicability** This section is only applicable to all standard and custom product PCDs that include air moving devices with specifications governing acoustic noise.

**5.3.10.3 Sample Size** AABUS, the minimum sample size for this test **shall** be one (1) to three (3) devices.

**5.3.10.4 Test Method** The devices acoustic emissions **shall** be measured according to the methods described in ISO-7779.

The test report **shall** include both:

- Declared A-weighted sound power level ($L_{WAd}$).
- Measured A-weighted sound pressure level ($L_{pAm}$) for each of the following operating modes applicable to the device:
  - Operating
  - Standby
  - Sleep

For the testing itself, the devices **shall** be placed on the floor of the hemi-anechoic chamber, raised by small elastic mounts as described for hard drives in ISO 7779 and/or ECMA 74. The device being tested **shall** be connected to the appropriate loads so as to be driven in a manner that maximizes the acoustic noise in each operational state. Any peripheral equipment used for this purpose should be outside of the measurement area (or outside of the chamber itself) so as not to corrupt the measurement with its own noise.

**5.3.11 Product Safety** The device **shall** be tested according to the methods defined in any product safety standards or specifications to which the device claims compliance.

Test reports from the appropriate agencies verifying compliance to the specified product safety standard or specifications **shall** be supplied upon request.

**5.3.12 Regulatory: "Green"** There are no requirements at this time.

## 6 QUALITY PROCESSES

This section addresses the requirements for quality processes at the supplier and sub-tier supplier facilities.

**6.1 Quality Management Systems** The PCD Supplier **shall** implement and maintain a Quality Program that **shall** assure design and manufacture of products is consistent with the requirements of ISO 9001 (TL9000 is also desired) Quality Management System Requirements. The Supplier **shall** assure that these requirements are implemented during the design phase and the manufacturing of the product. The supplier **shall** notify the customer of any changes in its quality program prior to implementation. The supplier's quality plan **shall** include:

- Locations where product will be manufactured/assembled; user will qualify and approve these locations at its option.
- Implementation and corrective action results for PFMEA (Process Failure Modes and Effects Analysis).
- Supplier's plan to support user's Line Reject Rate (LRR), Initial Field Incident Rate (IFIR) and long term reliability goals (LTR).
- Statistical Process Control plans with required data collection and quality metrics.
- Process capability assessment.
- Measurement capability assessment.
- Corrective Action Process.
- Design for reliability methods as described in Section 4 of this document.
- Development methods and testing for improving and verifying product design as described in Section 5 of this document.
- Manufacturing Process Flow Chart, operating procedures, process control points, quality goals by stage.
- Manufacturing conformance testing methods as described in Section 7 of this document.
- In Circuit Test (ICT), Automated Optical Inspection (AOI) or X-ray plan(s) as described in 7.2 of this document.
- Maverick control/Rework/screening process plans for all components and subassemblies.
- Supply Chain Management Process - potential problem control.
- Out of Box Audit (OBA) plans as described in 7.3.5.1 of this document.
- Ongoing Reliability Test (ORT) AABUS. When ORT is performed, it should follow the plans as described in Appendix E.2.3 of this document.
- Supplier Failure Analysis and reporting plan for user's return of verified failed product/components.
- Change/Revision Control.
- Product Identification and Lot Traceability.
- Documentation development.
- Production Test Equipment Calibration Process.
- Continuous Improvement Process.
- Providing regular reports of Quality Metrics defined in the Quality Plan.

See J-STD-001 and IPC-A-610 for additional workmanship details.

**6.1.1 Process Failure Modes and Effects Analysis** The supplier **shall** use Process Failure Modes and Effects Analysis (PFMEA) to optimize its processes, and **shall** provide documentation of issues resolved to the user upon request. A PFMEA examines potential failures at each ***process stage*** and determines the effect on downstream process stages (defect rate, rework and scrap). However, PFMEA applies to an assembly process and does not need to be applied to each product produced. PFMEA uses the same RPN measure of relative importance for addressing each potential failure type (see 4.4 of this document). PFMEA is a systemized group of activities intended to:

1. Recognize and evaluate the potential failure of an activity in a process step, and its effect on other stages of the process.
2. Identify actions which could eliminate or reduce the occurrence, or improve detectability, of the potential failure.
3. Document the process changes to reduce impact of failure.
4. Track process changes incorporated to avoid potential failures and their results on the process.

**6.1.2 Statistical Process Control** The supplier **shall** use appropriate Statistical Process Control methods such as the use of Shewhart control charts, custom charts, moving averages, sampling theory and other statistical techniques to assess the stability of processes in order to take appropriate action to reduce defects, and to determine the quality level of components, assemblies and products. Data to be monitored and recorded includes all critical parameters measured in ICT and all critical parameters measured in ATE testing -see 7.2 and 7.3. Those parameters considered to be critical are Efficiency and Output Voltage Regulation and these **shall** be monitored and analyzed. Other data that may be of use for improving process yield and eliminating defects, such as stress test data, should also be recorded and analyzed.

Control charts **shall** monitor key process variables. Control charting **shall** be accomplished on a real time basis in order to provide a dynamic feedback loop to the process that is being monitored. When an out-of-control condition is present in the process, manufacturing engineering **shall** identify the assignable cause responsible for the out-of-control condition. Once the assignable cause is determined corrective action **shall** be taken to prevent the problem from recurring. Verification that the corrective action mitigated the assignable cause is required to allow the process to continue normal operation and eliminate the out-of-control point from the chart plot.

The supplier **shall** keep records of all SPC measures and provide summaries and reports to the user on request.

**6.1.3 Process Capability Assessment** After assuring stability of a process (using methods such as control charts, 6.1.2) the capability of the process **shall** be assessed. A Cpk capability index will be calculated for all processes deemed to be in statistical control. Cpk relates the process mean to the nominal value of the specification. Cpk values **shall** be greater than or equal to 1.33 to indicate that a process is capable and is to be considered acceptable.

The calculations that are required to calculate Cpk are shown below. Note that USL is Upper Spec Limit and LSL is Lower Spec Limit, the process mean is determined from SPC methods such as a variable control chart, and $Z_{min}$ is calculated as shown. Cpk is simply $Z_{min}$ divided by 3. This metric takes into account any noncentered process, that is, if the process mean is not at the specification center.

$$Z_{USL} = \frac{USL - \mu_x}{\sigma_x}, Z_{LSL} = \frac{LSL - \mu_x}{\sigma_x}$$

*let,* $\mu_x$ *= process mean or* $\overline{\overline{X}}$ *(centerline from control chart);*

$$\sigma_x = \frac{\overline{R}}{d_2}$$

*Select the mininum of the following values:*

$$Z_{minimum} = minimum\ [Z_{USL}, -Z_{LSL}]$$

*The Cpk index is found by dividing this minimum value by 3:*

$$C_{pk} = \frac{Z_{minimum}}{3}$$

The supplier **shall** keep records of all process capability studies and provide summaries and reports to the user on request.

**6.1.4 Measurement Capability Assessment** All measurement equipment and gages utilized for inspection that deal with the determination of conformance to engineering specifications will require a measurement system evaluation. Suppliers **shall** conduct a Gage R&R for every critical measurement device. The supplier **shall** keep records of all measurement capability studies and provide summaries and reports to the user on request.

**6.1.5 Corrective Action Process** The supplier **shall** develop and implement a corrective action process that utilizes structured problem solving techniques to:

- Investigate the root causes of nonconforming product and identify the corrective actions needed to prevent a recurrence.
- Analyze all processes, work operations, quality records, service reports and user complaints to detect and eliminate potential causes of nonconforming product.
- Apply controls to ensure that corrective actions are taken and that they are effective.
- Implement and record change in procedures as a result of corrective actions taken.
- Corrective actions **shall** take into consideration all potential processes and products; not just the specific nonconforming product.

Additionally, the supplier's corrective action process **shall** provide for documentation that identifies the following:

- Specific defect.
- Technical investigation/analysis.
- Root cause.
- Containment for defect.
- Corrective action plan.
- Preventive actions to preclude a recurrence.
- Verification of effectiveness of actions.

The supplier **shall** keep records of all corrective action issues and provide summaries and reports to the user on request.

**6.1.6 Calibration** The supplier **shall** develop and maintain a system to assure all equipment used for the acceptance of product is calibrated with traceability to an internationally/nationally recognized Standards Institute such as the National Institute of Standards and Technology. Paragraph 4.10 of ISO 9002 may be used as a reference in developing a calibration system. Where appropriate, this should also include formal measurement capability studies. These records **shall** be made available for the user to review upon request.

- ***Calibration Procedures*** Calibration procedures **shall** be established that define the measurements to be made, accuracy required, temperature/humidity required and test equipment to be used in performing metrology verifications.
- ***Recalibration List*** The supplier **shall** maintain a listing of all equipment requiring recalibration and **shall** identify them by assigned tracking number, location and recalibration frequency. As a minimum, the recall system **shall** provide for early notification that an instrument is due for recalibration.

- ***Calibration Records*** The supplier **shall** maintain records of all calibrations performed. Calibration records **shall** as a minimum address the calibration procedure used, personnel performing the calibration, results, calibration status and traceability to a Primary or Secondary Standard. These records **shall** be made available for the user to review upon request.
- ***Out of Tolerance (Calibration) Notices*** In the event that tools or equipment used for product manufacturing, testing, or inspection are found to be out of tolerance or out of calibration, the supplier **shall** implement a system that will provide for the review of all product produced and accepted by the defective instrument. The supplier **shall** also implement a plan to repair/replace the equipment. The user **shall** be notified of the results of any such review and determination will be made at that time as to status and disposition of products built for the user.

**6.1.7 Continuous Improvement** The supplier **shall** develop and implement a Continuous Improvement Process (CIP) that will provide for a cost-effective reduction in process-related excursions. The program at a minimum **shall** include:

- A documented, systematic approach for identifying CIP focus areas.
- Design for quality initiative (i.e., HALT, FMEA, Margin Analysis, Tolerance Stack-up Analysis).
- Supplier management strategy.
- Manufacturing process controls.
- LRR (Line Reject Rate) and IFIR (Initial Field Incident Rate) reduction plans to achieve user requirements.

The supplier **shall** provide status of the implementation and results to the user upon request.

**6.1.8 Process Quality Metrics** The supplier **shall** use quality metrics as a basis to monitor the quality of its products and processes. Additionally, the supplier's quality program **shall** define the metrics for a stop ship and/or stop build action. Quality metrics, as a minimum, **shall** include:

- Manufacturing Yields.
- Test Station Yields.
- Inspection Yields.
- FIT demonstration data.
- Out of Box Audits (OBA) results.
- Annualized Failure Rate (AFR)/Annualized Return Rate (ARR) performance.
- Reliability test results.
- Initial Field Incident Rate (IFIR) and Line Reject Rate (LRR).

The supplier **shall** provide reports on its process quality metrics to the user upon request.

**6.2 Sub-Tier Supplier** The supplier **shall** develop and implement a system that will define quality and technical requirements to their component suppliers (sub-tier suppliers), AABUS. Quality and technical requirements are defined as quality programs, engineering drawings, specifications and functions to be performed by sub-tier suppliers. The PCD supplier may elect to use a contract, purchase order or other suitable means in defining these requirements, as long as the quality and technical requirements are fully documented and that the sub-tier suppliers verify understanding and implementation of such requirements.

The supplier **shall** perform a quality review of all proposed sub-tier suppliers prior to awarding business to a sub-tier supplier. The approval **shall** be based on review of the sub-tier suppliers' quality programs and ability to meet the supplier's expectations. The following factors appropriate to the products to be supplied **shall** be evaluated during the review:

- Manufacturing facilities.
- Inspection planning to assure that appropriate levels of inspections are implemented.
- Inspection controls including sampling plans and work instructions.
- Inspection capabilities including in-process and incoming inspections.
- Supplier's defect prevention programs.
- Past experience with the type of hardware to be supplied.
- Capability and condition of manufacturing equipment.
- Control of engineering drawings, specifications and changes.
- Change/Revision control.
- Control and maintenance of inspection equipment and production tooling.
- Employee training and certifications.
- Material storage and handling.
- Test and measurement equipment calibration program.
- Control of nonconforming hardware and materials.
- Corrective and Preventive action program.
- Ability to perform FMEAs (Design and Process).
- Experience in implementing Continuous Improvement Programs.
- Experience and implementation of Statistical Process Control.

Records of Sub-tier Supplier approvals including survey results **shall** be maintained and made available for the PCD user to review upon request.

- The supplier **shall** define reliability requirements to their critical component, sub-tier suppliers. These requirements **shall** align with those of the PCD user. The supplier **shall** implement testing as required to verify performance and reliability of components, or **shall** assure that the sub-tier supplier implement and report on such testing. These tests should include (as a minimum) functional testing of all critical parameters, measurement and monitoring of Statistical Process Control variables and ongoing reliability (ORT). Test reports should be provided on a regular basis.

- The PCD supplier **shall** adequately monitor component supplier's quality systems and performance for all components used in a design. This includes assuring a sub-tier quality management program that **shall** provide for quality goals, the performance of site surveys and audits, quality program requirements, change or revision control requirements, tests and inspections and component qualification before production in the case of new components.

**6.3 Materials Traceability Requirements** The supplier **shall** ensure a material traceability system is built into the standard operating practices on the shop floor and linked to the finished goods serial or batch numbers. This system should be capable of providing the following information:

- What raw material lot was used?
- When the raw material was received?
- Which supplier provided the material?
- When did the supplier perform the internal QC on the outgoing material?
- Which production line of the supplier was used?
- What engineering change notices (if any) were applied to the product?

**6.4 Change Authorization** Change authorization **shall** apply to custom products and may apply AABUS to standard products. After first article approval of a PCD design by the user, there **shall** be no design, process or material changes that may affect form, fit, function, reliability or Agency compliance without written approval of the user prior to implementation. User **shall** be notified via a change request notice. Change requests **shall** be accompanied by a reproducible set of documentation that fully describes the planned change. At the user's discretion, changes may require submittal of new first article samples for evaluation. Users **shall** accept or reject the change no later than 90 days after notification or 60 days after receipt of samples, whichever is later. (For further detail on change authorization, see JESD46.)

Suppliers **shall** provide notification of any change, with examples such as: end of life, quality alerts or security alerts. The ability to manage this process is seen as an integral part of the supplier's quality system, and necessary to ensure accurate and efficient tracking of changes and end-of-life changes.

With the use of a sub-tier supplier, the process **shall** continue to meet all of the criteria set forth in this document and the sub-tier supplier **shall** conform to the same requirements. Any failure by the sub-tier supplier **shall** be seen as a quality issue adversely impacting the supplier's rating, as the supplier **shall** remain responsible for the sub-tier supplier's compliance to requirements. The supplier **shall** have a process that demonstrates that their sub-tier supplier(s) are under change control.

**6.5 Qualification of Change** Suppliers **shall** provide data to support the change. Upon request, the supplier **shall** provide, a reasonable number of pieces indicated as necessary in order to qualify the new revision of the supplier product. Also, the supplier **shall** provide qualification and characterization information for each PCN as applicable. If this information is not available at the time the PCN is issued, the supplier **shall** provide a qualification plan and timeline with the initial PCN, and the final test report once it is available.

Suppliers **shall** provide samples for qualification upon request. Such samples **shall** be representative for the normal production of product to be supplied.

**6.5.1 Content of each Product Change Notice (PCN)/ End of Life (EOL)/Product Alert (PA)** This information **shall** include the following minimum information:

- Data Supporting Change.
- Internal Tracking Number.
- Name of Supplier.
- Contact Names (address, telephone/fax numbers).
- Planned Implementation Date.
- Product Identification.
- Detailed Description of Change/Reason.
- Quantifiable Impact on Quality (positive or negative).
- Impact on Reliability.
- Supporting Data and/or Qualification Date/Plan.
- Identification Method for Product Ordering Code Changes, if known.
- Application Changes, Enhancements and/or Work-Arounds.

**6.5.1.1 Product Alerts (PA)** The Alert timeline notification **shall** be within 72 hours of detection of the issue and the supplier **shall** issue a written alert upon the detection of any issue adversely affecting the safety, security and/or reliability of the supplier's product. If correction of the issue requires a change to the product or related processes, the supplier **shall** issue a related PCN and explicitly note the issue being corrected as well as its impact on the safety and/or reliability of the supplier's product. The purpose of this type of notification is to provide enough information to initially ascertain the severity of an issue and involve the appropriate people, and be able to contain/quarantine the affected products.

The content requirements for a PA **shall** be the same as a PCN, except that the PA **shall** also include the shipping quantities, shipping locations and the P.O. numbers.

**6.5.1.2 End of Life** Suppliers **shall** accept orders up to 12 months after notification of product discontinuation. Users **shall** accept delivery within 6 months of order date.

#### 6.5.1.3 Examples of Changes Requiring a PCN:

- Mechanical specification changes - Internal dimensions and associated tolerance changes.
- Environmental changes (MSL, Dry pack requirements, shelf life, storage temperature).
- Package Label (p/n name conventions, change to physical product identification markings).
- Electrical characteristics (Enhancements, bug or errata fixes ''firmware or software, parameter changes, reduction in test coverage, Flammability/ESD rating, Test site and or process).
- Mechanical/Material characteristics (Internal dimensions and associated tolerance changes including shape/ terminal finish ''lead base materials''/plating/solder ball composition/tolerance changes/molding compounds/ substrate material).
- Manufacturing/Assembly change (Mask, Manufacturing location, assembly site or process, Injection mold or tooling changes).
- Thermal characteristics.
- Performance characteristics.
- Firmware changes, UL-impacting hardware changes (BOM changes, new power supply revision).
- Regulatory approval changes (e.g., UL to CUL or VDE to TUV, etc.).
- Part Number or product Tracking (Ordering part numbering/series changes).
- Burn In (BI) or HASS process changes such as test time reduction/transition to audit (Note: BI/HASS process **shall** be reset to initial levels for a manufacturing location change - see Appendix E.2.4).

## 7 MANUFACTURING CONFORMANCE TESTING

This section defines the minimum test requirements for suppliers once the PCD is released to Manufacturing.

**7.1 Manufacturing Conformance Tests** The PCD supplier **shall** test every parameter specified in the Manufacturing Test Plan AABUS during the manufacturing of all PCDs. The Manufacturing Test Requirement (MTR) **shall** contain at a minimum the tests listed in the ''Production MTR'' Column of Appendix C-1 through C-3 as appropriate. At each test stage, data will be collected as described in 7.3 that follows. This data will be used for statistical process control and included in the Quality Yield Data provided to the PCD user upon request.

The flowchart represented in Figure 7-1 shows various types of manufacturing conformance tests to be conducted. The exact flow detail may vary from supplier to supplier based on product and the line layout. These tests (except ORT, BIA/HASA and QA Sampling Tests) should be performed on every unit fabricated in manufacturing (100% test). ORT, BIA/HASA and some QA audits are performed on a sample of the total manufacturing output, often for statistical process control (SPC) feedback. Note that a just-in-time manufacturing process is assumed, without 100% incoming inspection of individual components.

AABUS, HASS or HASA may be substituted for a 100% BI requirement. In addition, sample BI or BI audit (BIA) may be implemented AABUS. When BIA or HASA is in place, ATE1 can be a subset of ATE2. ATE1 need not be performed on units not subject to the audit.

**7.2 Early Manufacturing Conformance Test Requirements** Referring to the test flow chart in Figure 7-1, the first tests made on any subassembly is In-Circuit Tests (ICT) and/or Automated Optical and/or high resolution X-Ray testing. These procedures are required before final assembly and functional testing in most fabrication processes. The PCD supplier **shall** provide the test plan and fault coverage information for all in-circuit test (ICT) and automatic optical/x-ray inspection to the PCD user at the time of the Manufacturing Readiness Review.

In-Circuit test, Optical or X-ray inspection **shall** be performed on 100% of fabricated printed wiring board assemblies to assure workmanship quality and detect any soldering or component-placement faults. Data from these tests **shall** be collected, electronically if possible, and used for Statistical Process Control (SPC) calculations as described in 6.1.2 of this document.

**7.3 Final Assembly Test Requirements** As shown in Figure 7.1, there are several types of tests that may be applied to the final PCD. These tests fall into four categories:

- Functional Tests.
- Stress/Reliability Tests.
- Safety Tests.
- Quality Assurance Audit.

**7.3.1 Functional Tests** The PCD supplier **shall** test every parameter specified in the supplier's MTR on 100% of manufactured units using bench tests or, preferably, ATE (Automated Test Equipment). While in some cases the functionality may be tested at a single stage, the flow chart of Figure 7-1 shows two ATE stages: one prior to stress and safety tests, and one afterward. The method used by the

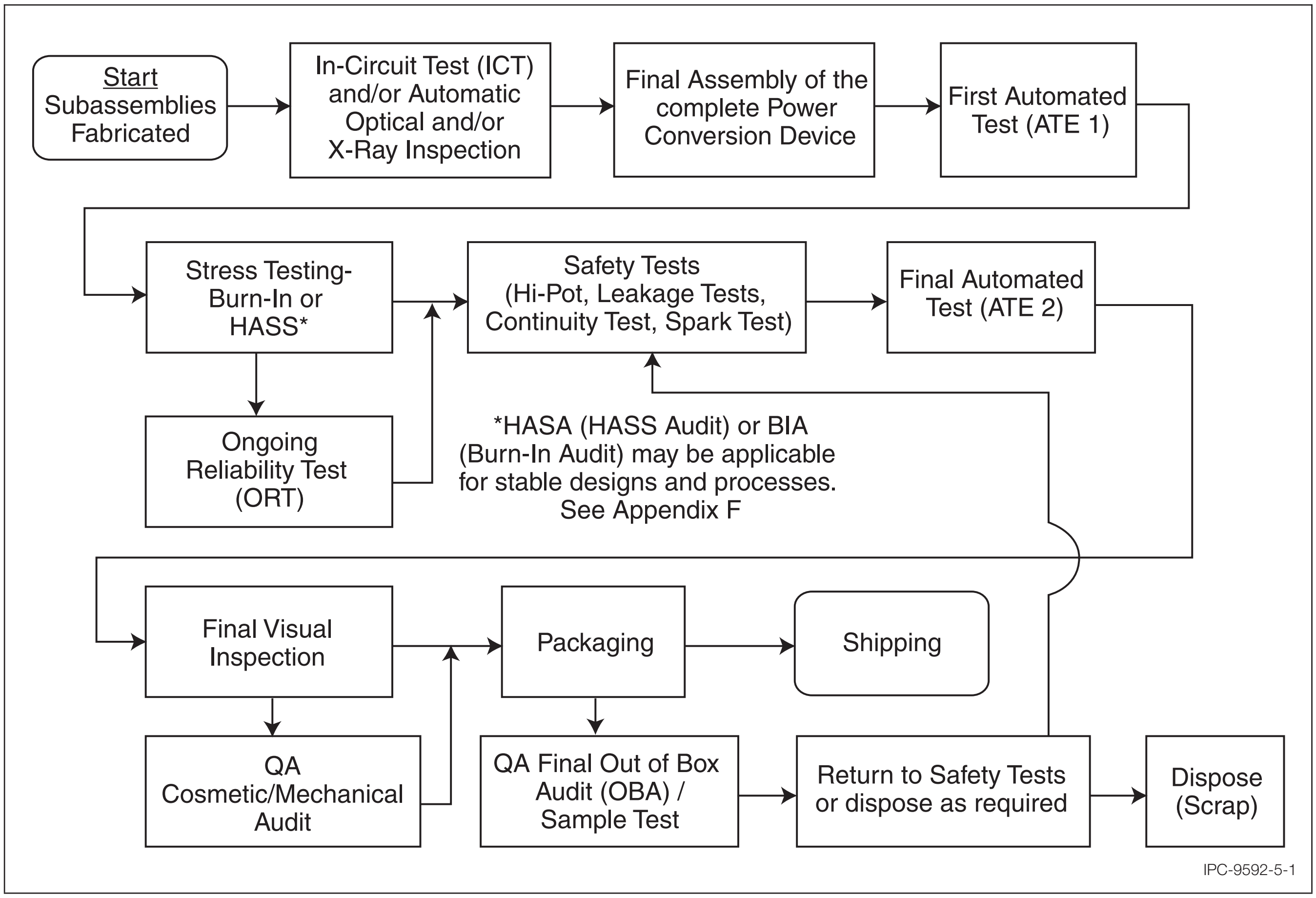


**Figure 7-1 Typical Manufacturing Conformance Test Flow**

PCD supplier depends on the systems in place at the manufacturing and test facilities. ATE 1 maybe a subset of tests at the suppliers discretion, however ATE 2 must be 100% coverage of all parameters per the MTR as specified in Appendix C. Data from these tests **shall** be collected, electronically if possible, and used for yield monitoring and failure analysis.

**7.3.2 Stress Tests (Short Term Reliability Tests - BI/HASS)** The PCD supplier **shall** initially provide in-line (for 100% of units) Burn-In or HASS (Highly Accelerated Stress Screen) at the PCD supplier's option as specified in Appendix E. An efficient manufacturing organization can often transition from 100% BI or HASS to a sample BIA/HASA stress test shortly after full production is in operation. Data from BI/BIA, HASS/HASA testing **shall** be collected, electronically if possible, and used for yield monitoring and failure analysis.

**7.3.3 Ongoing Reliability Testing (ORT)** Ongoing Reliability Testing (ORT) as specified in Appendix E **shall** be performed on a sample of product families (''product family'' is defined in 2.4). This testing is to assure no process or component degradation has affected the early life reliability of the product. ORT **shall** be performed ***only after*** *any final mechanical assembly such as frames or heat sinks have been attached.* ORT may subject a given unit to weeks of operation, often at increased stress levels and as such, can handle only a small percentage of production units. Individual units that complete a short-term ORT may be cycled back though a reconditioning and re-testing process and sold as new if the combined stress level and time effects do not degrade the long-term reliability. Use of reconditioned short-term ORT units must be agreed upon by the PCD customer.

**7.3.4 Safety Tests** All PCDs (100% of units) **shall** be subjected to required safety tests as defined by applicable regulatory documents and by the PCD user functional specifications. Safety tests include Hi-Pot, leakage tests, continuity and other tests to assure no electrical hazards exist in a PCD unit. Safety tests **shall** be performed after any final mechanical assembly such as heat sink attachment. Data from safety testing **shall** be collected and retained as required by the appropriate safety agencies. Yield data from safety testing **shall** be collected and retained.

**7.3.5 Final QA Cosmetic/Mechanical Audit** Quality Assurance Cosmetic/Mechanical Audit **shall** be performed to assure cosmetic requirements such as labels and markings; critical form, fit and function dimensions such as pin length; inspection for scratch free finish, etc. In addition, auditor **shall** confirm the existence of appropriate test records for samples being audited. QA inspection audits **shall** be performed ***only after*** any final mechanical assembly such as frames or heat sinks have been attached.

**7.3.5.1 QA Out of Box Audit (OBA)** QA Functional Tests will usually require ATE, but may be a subset of total functional testing as agreed upon with the PCD user. Data from these tests **shall** be collected, electronically if possible, and used for Statistical Process Control (SPC) calculations as described in 6.1.2. Additional Outgoing Quality Sampling Tests, often termed Out of Box Audit (OBA), **shall** be made on samples of units after packaging for shipment to assure proper handling, packaging and documentation has been supplied. Data from these audits **shall** be collected, electronically if possible, and used for SPC calculations as described in 6.1.2.

# APPENDIX A
# Derating Guidelines

The intent of this appendix is to provide a standard derating factor for worst-case conditions to be applied to each class of component. Worst-case conditions include maximum and minimum rated input conditions, environmental conditions and output load; or any combination of these conditions. For power assemblies required to operate in stand-by mode, this case must also be tested. Some derating parameters must be tested under worst-case transient conditions applied to the input or by an external load. Worst-case transient conditions **shall** include fault conditions that the assembly is designed to withstand, such as a short circuit for example.

Typically, measurements are taken at one extreme condition where the assembly is operating under worst-case stress with regard to that condition, for example maximum load. The other conditions are set to some nominal value. For custom PCDs, the classes, environmental and loading conditions and reporting requirements **shall** be AABUS. For standard (noncustom) PCDs, it is acceptable to use data taken under nominal conditions to show that the derating guidelines are met under all conditions if the method used to determine acceptability is documented and available for review. Unless required by the specification, the component derating guidelines do not need to be met when a continuous external fault is applied to the power assembly. It is expected that all components operate within their specified limits and that the assembly not be damaged if the fault condition is removed in a reasonable amount of time.

As part of the design process, a bill-of-materials (BOM) analysis **shall** be performed to ensure that every component of the design conforms to this standard. Any deviations from this standard **shall** be documented, along with an analysis of the risk of the deviation. Any derating curves provided in product data-sheets themselves **shall** always be followed or improved upon. The *Stress Factor* term is defined in Note 1 below each table. For voltage, current and power derating, this factor is used, with the design goal to be at or below this factor. Notes on specific component application issues appear below each table.

**Table A-1 Derating Guidelines for Capacitors[3]**

| Device Type | Parameter | Class II Stress Factor[1] | Class I Stress Factor[1] |
|---|---|---|---|
| **Capacitors** | | | |
| Fixed Ceramic - MLCC<br>Note: A surface mount part larger than a 1210 body size is not recommended due to potential for cracking | dc Voltage | ≤80% | ≤80% |
| | Temperature below Maximum Limit | ≥10 °C | ≥10 °C |
| Fixed Solid Tantalum<br>Note: Series resistance may be needed to assure that when the capacitor short circuits there will be no more than 6 amps of current through the cap. Investigate the use of tantalum polymer caps instead. | dc Voltage | ≤40% | ≤60% |
| | Ripple Current | ≤60% | N/A |
| | Reverse Voltage - Peak | ≤2% | ≤2% |
| | Temperature below Maximum Limit | ≥20 °C | ≥20 °C |
| Fixed Plastic | dc to ac Voltage Nominal | ≤70% | ≤70% |
| | Temperature below Maximum Limit | ≥10 °C | ≥10 °C |
| | Power Supply X-Y cap Voltage | Note 2 | Note 2 |
| Fixed Aluminum Electrolytic | dc Voltage | ≤80% | ≤80% |
| | dc Voltage (≥250V) | ≤90% | ≤90% |
| | Life/Endurance (using life cap equations) | ≥10 years at 40 °C 80% Load | ≥5 years at 40 °C 80% Load |
| Fixed Conductive Polymer Tantalum or Aluminum | dc Voltage | ≤70% | ≤85% |
| | Ripple Current | ≤80% | N/A |
| | Temperature below Maximum Limit | ≥10 °C | N/A |
| | Life/Endurance (using life cap equations) | ≥10 years at 40 °C 80% Load | ≥5 years at 40 °C 80% Load |
| Fixed Organic Semi-conductive Electrolytic Type | dc Voltage | ≤80% | ≤85% |
| | Ripple Current | ≤80% | N/A |
| | Temperature below Maximum Limit | ≥20 °C | N/A |
| | Life/Endurance (using life cap equations) | ≥10 years at 40 °C 80% Load | ≥5 years at 40 °C 80% Load |
| Fixed Mica, Glass<br>Not recommended - Fragile | dc Voltage | ≤70% | ≤70% |
| | Temperature below Maximum Limit | ≥10 °C | ≥10 °C |
| Variable Capacitors<br>Not recommended - Unreliable | N/A | N/A | N/A |

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Components with certified safety agency approvals may be used at up to 100% of their approved ratings.
3. PCD derating analysis **shall** be conducted using a 40 °C ambient air temperature. Capacitor life calculations **shall** be performed using localized ambient temperature for each capacitor with a PCD ambient air temperature of 40 °C.

***Capacitor Design Guidelines:***

- Electrolytic capacitors fail due to excess voltage, reverse voltage and the evaporation of electrolyte (which is a function of the core temperature resultant from the ambient temperature plus the temperature rise due to the square of the ripple current times the ESR of the capacitor).
- The life/endurance calculation **shall** be performed using the equation provided by the specific capacitor manufacturer.
- The breakdown voltage of an electrolytic is not at an abrupt voltage, but rather it is related to the thickness of a chemically generated oxide on the electrodes. If the working voltage slowly increases, the oxide thickness, and therefore the voltage capability of the capacitor, increases. Similarly the reverse is true if the working voltage reduces. The dc voltage + low frequency ac ripple **shall not** exceed the rated DC voltage.
- Aluminum electrolytic types are used for bulk low frequency filtering.
- Care must be taken when placing capacitors, especially electrolytic, in the vicinity of high temperature components.
- Capacitors must have a temperature rating of at least 105 °C and **shall** have 5,000 hour load life ratings when possible.
- Solid tantalum capacitors have been observed to fail short if they are not slowly charged to a voltage greater than the circuit requirements after the solder reflow. Heavy derating on the voltage might reduce the failure rates. However, see next item.

- Solid tantalum capacitors, when they fail as a short, can ignite and burn due to use of $MnO_2$, the material used in pyrotechnic mixtures, causing serious damage to printed wiring boards and nearby components. Solid tantalum capacitors **shall not** be used in high current or high power applications. Use polymer tantalum or polymer aluminum capacitors instead.
- Solid tantalum capacitors have been identified to have potential for influencing Electromagnetic characteristics of a system. Change in component type **shall** be reviewed for EMC impact.
- Polymer capacitors like OsCon, Poscap, Ta polymers and Al polymers are observed to have fewer failures in the field than solid tantalum and electrolytics.
- 0805 and larger size SMD ceramic capacitors can develop cracks during the assembly process. Certain series of ceramic capacitors from some manufacturers contain a safety margin in their internal plate construction. Capacitor designs with a safety-designed part do develop cracks but these cracks usually do not lead to shorting.
- All SMD ceramic capacitors 50V and above used across a power bus **shall** be of Fail-Open (or equivalent) type. SMD capacitors should not be used in 400 volt or higher applications.
- Z5U and Y5V types are not recommended due to higher temperature coefficient, lower temperature range and weak structure.
- SMD ceramic capacitors **shall not** be located on the PWB in areas that are subject to board flexing such as along the edge of a board or in a location where mating of connectors, mating of test fixtures, or transportation induced vibration causes board flexing.
- SMD ceramic capacitors of sizes larger than 1210 should only be used when special precautions are taken to mitigate the risk of cracking.
- Solid Niobium capacitors have unstable leakage characteristics and are flammable like solid Tantalum capacitors, and several manufacturers have recently discontinued production of these devices. Solid Niobium capacitors **shall not** be used in PCDs where high current or high energy is applied to the capacitor.
- Niobium Oxide capacitors have better stability and require far more energy to cause ignition than solid Tantalum or solid Niobium devices. However, their long-term reliability is unknown at this time since the technology is emerging. They **shall** be used with caution, only in low energy circuits.

**Table A-2 Derating Guidelines for Resistors**

| Device Type | Parameter | Class II Stress Factor[1] | Class I Stress Factor[1] |
|---|---|---|---|
| **Resistors** | | | |
| Fixed Film (Discrete and SMD Thin-Film, Thick-Film and Metal Oxide) | Power Dissipation | ≤60% | ≤70% |
| | Maximum Working Voltage | ≤70% | ≤70% |
| | Below Maximum Temperature Limit | ≥25 °C | ≥25 °C |
| | SMD Maximum Body Temperature | 100 °C | N/A |
| Zero Ohm | Current | ≤85% | ≤85% |
| Carbon Composition | Power Dissipation | ≤60% | ≤70% |
| | Maximum Working Voltage | ≤60% | N/A |
| | Below Maximum Temperature Limit | ≥25 °C | ≥25 °C |
| Wirewound Power | Power Dissipation | ≤70% | ≤70% |
| | Maximum Working Voltage | ≤60% | N/A |
| | Below Maximum Temperature Limit | ≥6 °C below | ≥6 °C |
| Variable | Power Dissipation | ≤40% | ≤70% |
| | Maximum Working Voltage | ≤50% | ≤50% |
| | Wirewound Below Maximum Temperature Limit | ≥20 °C below | ≥20 °C |
| | Nonwirewound Below Maximum Temperature Limit | ≥30 °C below | ≥30 °C |
| Thermistor | Power Dissipation | ≤50% | ≤50% |
| | Maximum Working Voltage | ≤80% | N/A |
| | Below Maximum Temperature Limit | ≥50 °C | ≥50 °C |
| | Hot Spot Temperature | ≤130 °C | N/A |
| Metal Oxide Varistors | Power Dissipation | ≤60% | ≤60% |
| | Operating Voltage/Clamping Voltage | 30% | 30% |
| | Maximum Current | ≤90% | ≤90% |
| | Rated RMS Voltage | ≤90% | ≤90% |
| | Maximum Energy for All Timings | ≤90% | ≤90% |
| Thick Film Network | Power Dissipation | ≤70% | ≤70% |
| | Below Maximum Temperature Limit | ≥24 °C | ≥24 °C |
| | SMD Maximum Body Temperature | ≤100 °C | N/A |

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.

***Resistor Design Guidelines:***

- Failures in resistors are caused by excessive power dissipation, high ambient temperature, or excessive joules in pulsed in applications.
- All film resistors and to a lesser extent other types of resistors have a limited capability to handle high peak power pulses even though the average power dissipation may be within rating. Refer to the manufacturer's data sheet for peak powers versus time and duty cycle. If high pulse powers are expected, a solid element composition, ceramic-carbon or wire wound resistor may be more appropriate.
- Leaded film resistors are trimmed to their final value by cutting a helix in the film. High value resistors used in line voltage, 400V bus and snubber applications are subject to a number of reliability issues. These resistors have a high spiral turns count that leads to a very narrow element width and hot-spot problems. The laser cut is very narrow leading to high voltage field levels and ionization between turns.
- Chip film resistors are trimmed by making a cut or series of cuts across the resistor. Excessive trimming will lead to narrow sections that will develop into hot spots.
- Metal film resistors are recommended over carbon types. Since carbon is less stable over humidity and life, they are not recommended where drift may be an issue.
- Wire wound resistors are recommended for dissipation greater than 2 Watts, for stability and reliability reasons.
- Potentiometers are to be avoided, if possible, due to the need for adjustability in manufacturing and low reliability. Where two terminals of the potentiometer are normally connected for potentiometer operation, the variation effect could be made small and may not affect reliability. Device ratings are to be met for low or zero resistance adjustment.

- Considerations **shall** be given to low inductance resistor types whenever necessary.
- Follow the guidelines for resistor mounting to be properly spaced from the PCB surface.
- The maximum stress on any resistor due to line transients, safety testing etc. **shall not** exceed the manufacturer's 'Maximum Overload Voltage' or equivalent specification.
- Thermistors used for surge limiting have a specific capability to absorb a single power pulse when charging large bulk capacitors, particularly in off line power supplies. The rating may be in the form of maximum capacitance.
- Varistors are used for shunt regulators and for transient protection:
  - Shunt regulator: working voltage is limited by power dissipation.
  - Transient protection: working voltage is limited by power dissipation over the normal voltage range and by Energy or Amps-Seconds for transients.
- Beware of SMD thick film resistor construction in regard to the method of inner layer nickel deposition and the silver termination. The dipped type methods are inferior to the plated methods. The dipped types allow gaps that will expose inner silver substrates to atmospheric sulphur compounds which can lead to corrosion and long term failures (opens). In addition, the silver plating should be doped with palladium to retard the silver sulfide crystal growth. It is recommended that thick film resistors of an anti-sulfuration design be used in potted applications.

**Table A-3 Derating Guidelines for Diodes and Transistors**

| Device Type | Parameter | Classes I and II Stress Factors[1,2] |
|---|---|---|
| **Diodes** | | |
| General Purpose (Signal or Switching - Junction, PiN, Schottky) | Forward Current | ≤90% |
| | Reverse Voltage | ≤70% |
| | Power | ≤75% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Power Rectifier (Schottky and Non-Schottky) | Avg. Forward Current | ≤90% |
| | Reverse Voltage | ≤80% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| | Power | ≤70% |
| Silicon Carbide<br>Power Rectifier<br>Do Not Avalanche SiC Diodes | Forward Current | ≤80% |
| | Reverse Voltage | ≤80% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Transient Voltage Suppressor | Power Dissipation | ≤90% |
| | Average Current | ≤90% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Voltage Regulator/Reference (including Zener) | Power Dissipation | ≤50% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Thyristor, SCR and Triac | Transient Energy | ≤80% |
| | On-State Current (It) | ≤90% |
| | Off-State Voltage (Vr) | ≤70% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Microwave | Power | ≤90% |
| | Reverse Voltage | ≤70% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| LED<br>GaAs GaP GaN-SiC<br>GaAsP AlGaAs | Power | ≤70% |
| | Forward Current | ≤90% |
| | Reverse Voltage Peak | ≤80% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Photo Diode | Power Dissipation | 80% |
| | Current | 75% |
| | Voltage | 75% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Injection Laser Diode | Power Output | 75% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| Silicon Bipolar - Small Signal or Power | Power | 75% |
| | Collector-Emitter Voltage | 80% |
| | Emitter-Base Voltage | 80% |
| | Collector Current | 60% |
| | Maximum Junction Temperature ($T_j$) | $T_j$ maximum - 25 °C |
| Silicon FET - Small Signal | Drain - Source Breakdown Voltage | 80% |
| | Gate - Source Voltage | 80% |
| | Drain Current | 80% |
| | Maximum Junction Temperature ($T_j$) | $T_j$ maximum - 25 °C |
| | ESD Rating | >1000V |
| | Power PD | ≤75% |

| Device Type | Parameter | Classes I and II Stress Factors[1,2] |
|---|---|---|
| **Diodes** | | |
| Power MOSFET and IGBT | Drain Current/Collector Current | ≤75%/≤ 60% |
| | Drain - Source/Collector- Emitter Voltage | ≤80%/≤ 80% |
| | Gate - Source Voltage | ≤80% |
| | Maximum Junction Temperature ($T_j$) | $T_j$ maximum - 25 °C |
| | Avalanche Energy EAS | ≤50% |
| | Power Dissipation | 80% |
| Photo Transistor | Current | 75% |
| | Voltage | 75% |
| | Maximum $T_j$ | $T_j$ maximum - 25 °C |
| FET GaAs | Power Dissipation | 90% |
| | Maximum Channel Temperature | $T_j$ maximum - 25 °C |
| Hetro Junction Bipolar GaAs | Power Dissipation | 90% |
| | Maximum Channel Temperature | $T_j$ maximum - 25 °C |
| High Mobility GaAs | Power Dissipation | 90% |
| | Maximum Channel Temperature | $T_j$ maximum - 25 °C |

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Semiconductor devices do not wear out like many other component types under normal operating conditions, therefore only one stress level is defined.

***Diode Design Guidelines:***

- In bridge rectifiers, typical failures are due to excessive surge current and reverse voltage conditions. In universal power supplies, a minimum of 600 Volts Peak-Inverse-Voltage is recommended for the diodes.
- Switching losses and conduction losses contribute to the total power dissipation for diodes in switching circuits. When determining the rating, the PIV of the diodes at high temperatures of operation **shall** be taken into account.
- Extreme precaution needs to be taken for assembly of diodes into a heat sink. Insulation and torque of the screws need to be properly specified to avoid any failures of the diodes.
- If diodes are in series, then, to share the break down voltage, a resistor and a capacitor **shall** be used in parallel to each diode. The maximum junction temperature for this particular case **shall** be reduced to 100 °C.
- The power dissipation in a Schottky rectifier will come from RMS current losses + average current losses + leakage current losses. There are significant components of each.
- Excessive power dissipation is the primary reason for failure of the zener diodes.
- A series resistor **shall** be used to limit the current (power dissipation) through the zener.
- A capacitor across the zener stabilizes the zener voltage and reduces high frequency noise.
- Zeners that have a voltage rating close to 5V have the lowest temperature coefficient for the voltage.
- Biasing the zeners at the manufacturer's test level of current provides an accurate value for the zener voltage in circuit.

***Transistor Design Guidelines:***

- The main causes of failure in transistors are elevated junction temperatures and voltages exceeding the rated breakdown voltage of the device. The measured voltage **shall** include all transient conditions (dynamic loading or starting conditions).
- Usage of TO220 devices is to be avoided whenever possible. If it is found necessary to use TO220 devices the leads must have insulating sleeves and an insulation coating **shall** be applied at the intersection of the leads and the body of the device and also where the leads intersect the PCB.
- For transistors, the supplier **shall** allow for the degradation of parameters over time:
  - Gain (± 50%).
  - Leakage Current - $I_{CBO}$ or $I_{CEO}$ (+100%).
  - Switching times (± 20%).
  - Saturation Voltage (± 20%).
- The supplier **shall** use base to emitter resistors to reduce false turn on due to leakage.
- Extreme precaution needs to be taken for assembly of semiconductors into a heat sink. Insulation and torquing for the screws need to be properly specified to avoid any failures of the semiconductors. Gap fillers should be used where appropriate. Gang type mounting should be scrutinized to avoid unequal mounting forces.

- Static electricity can damage or destroy a MOSFET, especially gate to source voltages. Handling and design **shall** minimize the possibility of ESD events on the gate.
- To prevent oscillations, the supplier **shall** use gate resistors when FETS are paralleled. The resistor provides damping to dampen the ringing due to parasitic inductance and gate capacitances.
- MOSFET device **shall not** be avalanched on any repetitive basis, and possibility of avalanching **shall** be minimized even during worst-case (such as start-up or shut-down) or fault conditions.
- Be wary of power ratings - they are usually specified at a case temperature of 25 °C. Apply the appropriate derating curve for higher case/ambient temperatures (provided by supplier).
- Use GaAs FETs for high temperature and for very high frequency (microwave) applications.

**Table A-4 Derating Guidelines for Magnetics**

| Device Type | Parameter | Class II Stress Factor[1] | Class I Stress Factor[1] |
|---|---|---|---|
| **Magnetics** | | | |
| Pulse - Transformers | Peak Voltage | 90% | 90% |
| | Current | 60% | 90% |
| | Maximum Hot Spot Temperature (Below Insulation Rating) [2] | 25 °C | 25 °C |
| Power - Transformers | Power Per Winding | 80% | N/A |
| | Maximum Hot Spot Temperature (Below Insulation Rating) [2] | 25 °C | 25 °C |
| | Temperature below specified Fuse temperature | 15 °C | 15 °C |
| | Surge Voltage | 90% | 90% |
| | Surge Current | 90% | 90% |
| | Continuous Current | 80% | 80% |
| Coil (RF) | Power | 80% | 80% |
| | Current dc | 90% | 90% |
| | Voltage Surge | 90% | 90% |
| | Maximum Hot Spot Temperature (Below Insulation Rating) [2] | 25 °C | 25 °C |
| Ferrite Material Core (Incl: dc Chokes)<br>Note: Designs utilizing powdered iron cores must use proper thermal derating to prevent thermal aging, which can lead to overheated insulation on transformer wires that may result in fire. | Maximum Hot Spot Temperature (Below Insulation Rating) [2] | 25 °C | 25 °C |

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Insulation Ratings: Class A - 105 °C Class B - 130 °C Class F - 155 °C Class H - 180 °C.

### *Magnetics Design Guidelines:*

- In general, for linear operation, the flux density of operation **shall** be far below the saturation flux density of the device core. The flux density of operation is a design limit which is highly dependent on the temperature characteristics of the specific core used. For example, 4500 Gauss (450mT) at 10 Oersteds (800A/M) may be the core specification saturation flux density but a practical design limit might be 2850 Gauss at 2 Oersteds. Given the saturation flux density roll off at 100 °C, the usable flux density may be from 2600 Gauss to 3200 Gauss.
- Exceeding the rated hot spot temperature of the insulation will reduce the life of a device.
- Structural parts of a magnetics assembly **shall not** be operated at temperatures above the temperature rating of the materials used.
- Adhesives used in SMD or other magnetic parts should be evaluated at maximum hot and cold temperatures to ensure there is no ‘‘cold flow’’ or cracking resulting in loose construction and gap changes.
- Winding specifications should include tension monitoring to prevent wire stretching and insulation cracking.

### *Transformers:*

- Power transformer operation at low frequencies may result in overheating, due to lower reactance allowing large currents.
- Some power transformers generate large magnetic fields, which can couple ac signals into nearby circuits. Use appropriately shielded transformers, separate shielding and adequate spacing where needed.
- Transformers have been identified to have potential for influencing Electromagnetic characteristics of system. Change in component type **shall** be reviewed for EMC impact.

### *Inductors:*

- Ensure that power inductor core binder material does not contain stearic acid, octadecanoic acid, hexadecanoic acid or other long-chain acids that may break down over time. Use of such materials with internal spot temperatures over 130 °C can lead to rapid failure after a short-to-moderate time of apparently normal operation.
- Be careful that dc current does not saturate the magnetic core, which will drastically change inductor characteristics.

- SMT inductors and filters are susceptible to damage by soldering heat. Keep temperature ramp less than 4 °C/second by gradual preheating, to avoid cracking of the internal layers.
- SMD or through-hole components with large numbers of ferrite layers are most susceptible to thermal shock and impact stresses.
- Open circuits can occur due to mechanical damage to component body or body-termination bond from vibration, shock or overload during service life; and from flexure, vibration or shock during assembly.
- Through-hole inductors may fail due to weakening of internal low temperature solder connections by assembly soldering heat. Welded internal connections avoid this risk.
- Provide conductive heat transfer paths and locate inductors for best cooling.
- Make sure that circuits driving inductive loads are characterized for their Safe Operating Area or employ appropriate transient suppression.
- Inductors have been identified to have potential for influencing Electromagnetic characteristics of system. Change in component type **shall** be reviewed for EMC impact.

**Table A-5 Derating Guidelines for Microcircuits and Hybrid Microcircuits**

| Device Type | Parameter | Class II Stress Factor[1] | Class I Stress Factor[1] |
|---|---|---|---|
| **Microcircuits** | | | |
| Silicon Digital (MOS and Bipolar) | Output Current | 80% | N/A |
| | Frequency | 90% | N/A |
| | Maximum Junction Temperature | 100 °C (20 years EOL)<br>115 °C (5 years EOL)<br>115 °C (But No Higher than Manufacturer's $T_j$ Maximum ) | 115 °C |
| Silicon Linear ICs (Bipolar) | Input Voltage | 85% | N/A |
| | Output Voltage[2] | 80% | 80% |
| | Output Current | 80% | 90% |
| | Maximum Junction Temperature | 100 °C (20 years EOL)<br>115 °C (5 years EOL)<br>115 °C (But No Higher than Manufacturer's $T_j$ Maximum ) | 115 °C |
| Silicon Linear ICs (JFET and MOS) | Input Voltage | 70% | N/A |
| | Output Voltage[2] | 80% | 80% |
| | Output Current | 90% | 90% |
| | Maximum Junction Temperature | 100 °C (20 years EOL)<br>115 °C (5 years EOL)<br>115 °C (But No Higher than Manufacturer's $T_j$ Maximum ) | 115 °C |
| **Hybrid Microcircuits** | | | |
| Thick Film Resistor | Power Dissipation | 70% | 70% |
| Thin Film Resistor | Power Dissipation | 70% | 70% |
| Chip Resistor | Power Dissipation | 70% | 70% |
| Chip Capacitor | Voltage | 70% | 70% |
| Gen Purpose Diode | Forward Current | 90% | 90% |
| | Reverse Voltage | 80% | 80% |
| Microwave Diode | Power Dissipation | 90% | 90% |
| | Reverse Voltage | 80% | 80% |
| Bipolar Transistor | Power Dissipation | 90% | 90% |
| | Voltage (Vce) | 80% | 80% |
| FET | Power Dissipation | 90% | 90% |
| | Breakdown Voltage | 90% | 90% |
| Hybrid Package | Maximum $T_j$ | $T_j$ maximum - 25 °C | $T_j$ maximum - 25 °C |

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Output voltage derating does not apply to fixed voltage regulator ICs.

***Monolithic and Hybrid Microcircuit Design Guidelines:***

- Continuous Power needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual power above the maximum recommended operating power given by the device specifications or Datasheet.
- Maximum Core Voltage needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual Core Voltage above the maximum recommended operating Core Voltage.
- Minimum Core Voltage needs to be Derated such that any Tolerance or errors in design, other components, or operating conditions never bring the actual Core Voltage below the minimum recommended operating Core Voltage.
- Maximum IO Voltage needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual IO Voltage above the maximum recommended operating IO Voltage.
- Minimum IO Voltage needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual IO Voltage below the minimum recommended operating IO Voltage.
- Maximum Operating Frequency needs to be derated to below the specified Maximum Operating Frequency to

allow for device performance degradation over time due to Hot Carrier Injection (HCI) and Negative Bias Transistor Instability (NBTI) effects. HCI and NBTI effects degrade MPU performance by causing core transistor VT to drift upwards with the passage of time; (absolute value of VT for PMOS transistors). This especially affects processors and DRAMs.

- Be aware of minimum operating frequency problems. Do not operate dynamic circuits below the minimum specified clock frequency; or they will ''forget'' data, particularly at high temperatures!
- The Turn-on sequence (of input signals, output loads, clocks and PCD voltages) is often crucial. The wrong Turn-on sequence (such as input voltages higher than or present before supply voltages) can result in latch-up, with permanent damage to the IC. Input clamping diodes to supply and ground may be necessary at interfaces between separately powered circuits.
- *Follow IC manufacturer's recommendations for terminating unused inputs; in general, they* ***shall not*** *be left floating.* To minimize component count, several inputs may be terminated by the same resistor(s).
- Linear ICs, both bipolar and MOS, are generally very susceptible to ESD damage. *Sub-catastrophic ESD* damage can increase noise and shift DC operating parameters, and lead to erratic operation and functional failure over time.
- The slew rate of a linear circuit may be limited by available current so that full scale output is not possible over its full bandwidth. For example, an amplifier may have a small signal bandwidth of 1 MHz and be capable of an output of 20 volts peak to peak, but to do both at once without distortion requires a slew rate capability of more than 63 volts/μsec.
- Linear ICs usually have parasitic thermal feedback. For example, the zero offset of the input stage of an operational amplifier or comparator will change as the output changes amplitude or polarity, because temperature changes of the output stage affect the input state on the same die. Thermally induced offset shifts, of 50 μV to 1 mV (referred to input) are common, unless the IC layout has been designed to minimize this effect.

**Table A-6 Derating Guidelines for Miscellaneous Electricals and Electronics**

| Device Type | Parameter | Class II Stress Factor[1] | Class I Stress Factor[1] |
|---|---|---|---|
| **Miscellaneous** | | | |
| Circuit Breakers (Note 2) | Current | ≤60% | ≤80% |
| | Voltage | ≤60% | N/A |
| Fuses (Metal Element) | Current (Normal Blow) | ≤90% | ≤90% |
| | Current (Time Delay - Slow Blow) | ≤85% | ≤85% |
| | Operating Control/$I_{Holding}$ | | N/A |
| | $I^2t$ Rating | ≤70% | ≤70% |
| Fuses (Resetable Poly-Element Fuses) Note these Degrade over Time | Operating Current/$I_{Holding}$ | ≤50% | ≤80% |
| | Fault Current of $I_{Max}$ | ≤50% | ≤80% |
| | Voltage | ≤70% | ≤80% |
| Fans - See IPC-9591 Performance Parameters for Air Moving Devices | RPM Average | 90% to 100% Maximum | N/A |
| | Bearing Load | See Supplier Specs | See Supplier Specs |
| | Temperature Below Maximum Limit | ≥25 °C | N/A |
| Connectors (Circular/PWB/Coaxial) (Connectors - Power) (Connectors, Relays and Switches with oxidizing contacts) | Voltage | ≤70% | ≤70% |
| | Current | ≤70% | ≤70% |
| | Insert Temperature below Maximum Limit | ≥25 °C | ≥25 °C |
| | For Primary Voltages | Note 2 | Note 2 |
| | Minimum Dry Circuit Voltage | 12V | 12V |
| | Minimum Dry Circuit Current | 100mA | 100mA |
| Relays | Resistive Load Current | ≤75% | ≤75% |
| | Capacitive Load Current | ≤75% | ≤75% |
| | Inductive Load Current (Non-clamped) | ≤40% | ≤40% |
| | Inductive Load Current (Clamped) | ≤75% | ≤75% |
| | Motor Load Current | ≤20% | ≤20% |
| | Filament (Lamp) Current | ≤10% | ≤10% |
| | Contact Voltage (ac or dc) | ≤50% | N/A |
| | Contact Power | ≤50% | ≤50% |
| | Drive Voltage Minimum/Rated Minimum V | ≥110% | N/A |
| | Drive Voltage Maximum/Rated Maximum | 100% Maximum | N/A |
| | Coil Dropout Voltage/Rated | ≤90% | N/A |
| | Temperature Below Maximum Limit | ≥20 °C | N/A |
| Switches (General Purpose) | Contact Current - Resistive Load | ≤75% | ≤90% |
| | Contact Current - Capacitive Load | ≤75% | ≤90% |
| | Contact Current - Inductive Load | ≤40% | ≤75% |
| | Inductive Load Current (Clamped) | ≤75% | ≤75% |
| | Contact Current - Motor Load | ≤20% | ≤30% |
| | Contact Current - Filament (Lamp) Load | ≤10% | ≤20% |
| | Contact Power | ≤50% | ≤70% |
| | Contact Voltage (ac or dc) | ≤50% | N/A |
| | Contact Surge Current | ≤80% | ≤80% |
| | Temperature below Maximum Limit | ≥20 °C | ≥20 °C |
| Crystals (incl. Oscillators) | Current | ≤70% | Follow Manufacturer's Spec |
| | Drive Level Power | 33% | Follow Manufacturer's Spec |
| | Voltage | Follow Manufacturer's Spec | Follow Manufacturer's Spec |
| | Temperature below Maximum Limit | ≥30 °C | Follow Manufacturer's Spec |

| Device Type | Parameter | Class II Stress Factor[1] | Class I Stress Factor[1] |
|---|---|---|---|
| **Miscellaneous** | | | |
| Opto-Isolators | Peak Voltage | ≤75% | ≤75% |
| | Current | ≤70% | ≤70% |
| | Power | ≤80% | ≤80% |
| | Junction Temperature | 0.75 ($T_j$ maximum - 25 °C) + 20 °C | 0.75 ($T_j$ maximum - 25 °C) + 20 °C |
| | CTR | ≤75% | ≤75% |
| Fiber Cable | Isolation Voltage | ≤80% | ≤80% |
| | Bend Radius (% Minimum Rating) | ≥200% | ≥200% |
| | Cable Tension (% Rated Strength) | ≤50% | ≤50% |
| | Fiber Tension (% Proof Test) | ≤20% | ≤20% |
| Coax Cable | Bend Radius (% Minimum Rating ) | ≥110% | ≥110% |
| Lamp - Incandescent | Voltage | ≤94% | ≤94% |
| | Temperature | ≤175 °C | ≤175 °C |
| Lamp - Neon | Current | ≤98% | ≤98% |
| | Temperature | ≤150 °C | ≤150 °C |
| Printed Wiring (Circuit) Board | Absolute Maximum Temperature | 10 °C less than UL rating specification of the laminate materials | UL rating specification of the laminate materials |
| | Minimum Creepage and Clearance | Safety Agency Mandated | Safety Agency Mandated |

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Components with certified safety agency approvals may be used up to 100% of their approved ratings.

### *Miscellaneous Design Guidelines:*

### *Circuit Breakers and Fuses:*

- Both circuit breakers and fuses used in primary (line-voltage) circuits need to meet appropriate regulatory (safety) standards - see your product regulations engineer before specifying parts.
- Action of both circuit breakers and fuses is temperature dependent - be sure to review manufacturer's data sheet for effect of temperature.
- Circuit breakers come in many styles with varied trip mechanisms - use supplier specifications to determine appropriate types for your application, including current rating, voltage rating, breaking capacity, trip speed versus current level and temperature sensitivity.
- Circuit breakers have been identified to have potential for influencing Electromagnetic characteristics of system. Change in component type **shall** be reviewed for EMC impact.
- Never use a fuse to directly protect an electronic component (such as a fuse in series with the output of a power transistor). The electronic component can be destroyed much faster than a fuse can react.
- Keep in mind that a fuse or circuit breaker takes time to operate with overcurrent situations; the higher the overcurrent level, the faster the reaction time. There are specifications for each type of fuse and circuit breaker that describe the time to open under a given condition. Very high overloads can open a fuse in a fraction of a second, but your circuitry must not be damaged by these conditions or the fuse is offering no real protection.
- Fuses are NOT all rated and tested the same - be wary of differences from one manufacturer to another.
- SMT versions of fuses may have poorer heat dissipating capability than otherwise identical thru-hole or clip-mount versions and may require additional temperature derating. See manufacturer's data sheet.
- Resetable Poly-Element Fuses do not provide fuse-like resistance when operating at normal currents - resistance may be less than 0.1 ohm for some devices, but may be as high as tens of ohms. Check device data sheet.
- Resetable Poly-Element Fuses do not provide an ''open'' circuit when tripped - their resistance increases a few orders of magnitude from their ''on'' state (a factor of 1,000 to 10,000 times typically).
- Avoid operating Resetable Poly-Element Fuses without current limiting in a fault case - currents over their maximum current ratings can cause arcing, burning and destruction.
- Polymer Resetable Fuses do not provide stable ''on'' or ''off'' resistances with repeated use - take this into account in your circuit design. There are Ceramic Resetable Fuses that provide more stable ''on'' resistance with repeated operation and repeatable ''off'' resistance at constant ambient temperatures, but Ceramic Resetable Fuses cost more than Polymer Resetable Fuses.

***Fans:***

- Modern DC fans are complex devices with both mechanical and electronic components. See IPC-9591, *Performance Parameters (Mechanical, Electrical, Environmental and Quality/Reliability) for Air Moving Devices* for comprehensive details on fan applications.
- Fans have been identified to have potential for influencing Electromagnetic characteristics of systems and acoustic levels that may impact use in many environments. Change in component type **shall** be reviewed for impact.

***Connectors:***

- Connector pins required to handle low currents (<3Amps steady state) **shall** have a minimum of 30 µin of Au over 50 µin Ni in the contact area. Refer to 4.2 for exception handling.
- Connector pins can be connected in parallel to increase the current capacity. Allow an additional 10% derating for multiple pins in parallel. Airflow through the connector **shall** help in lowering the hot spot temperature.
- High current pins can be positioned to be at the ends of the connector rather than the middle for better heat transfer.
- Smaller width and multiple connectors may be preferred rather than one longer width connector for radiated emissions reduction.
- Temperature, moisture, excessive contact currents and vibration may cause connector failures. Fretting corrosion can cause intermittent connections. Contacts can also be welded because of surge currents in the circuit.
- Consideration should be given to potential mating cycles anticipated, as this could affect contact mating forces and plating abrasion, resulting in higher contact resistance (with all approved sources).

***Relays:***

- The use of a diode across the relay coil to clamp the turn-off voltage is recommended to avoid damaging transistors driving the coil from inductive voltage spikes.
- Paralleling the relays and contacts for increasing the current capacity of contacts is not recommended because one may close or open before the other.
- The number of cycles of operation **shall not** exceed the rated number.
- Vibration testing needs to be done to ensure reliable operation. For environments with vibration or temperature cycling, contacts must be prevented from microscopically moving. Displacements on the order of 100 µm will cause fretting which can lead to corrosion and failure.
- Test processes for testing of relay functionality **shall** consider the design requirements for the relay. As an example, certain relays can be damaged if they are opened when current is passing through the relay.

***Switches:***

- Extreme care **shall** be taken to look into specifications to differentiate ac and dc inputs. A switch that is rated for ac applications may not be suited for dc inputs and must be evaluated accordingly. The derating **shall** be applied to the appropriate rated ac input or the dc input rating.
- High surge currents can weld the contacts of a switch.
- Use of Agency ratings is acceptable.
- For environments with vibration or temperature cycling, contacts must be prevented from microscopically moving. Displacements on the order of 100 µm will cause fretting which can lead to corrosion and failure.

***Crystals and Oscillators:***

- Use crystals and oscillators ''ruggedized'' for shock and vibration. This will help both in handling bare parts during assembly and in long term reliability by protecting against shock and vibration during shipping, installation and operation.
- Be careful with crystal and oscillator packages, especially in SMT designs. They are brittle and can be cracked by excessive board flexing.
- Take ESD precautions when handing and assembling boards with crystals and oscillators.

***Opto-Isolators:***

- Opto-isolators are used for providing isolation between primary and secondary circuits either in the feedback loop area or for passing status information across the isolation boundary.
- Failures can occur due to excessive voltage ratings or junction temperatures.
- The CTR (Current Transfer Ratio) can vary wildly (6 to 1) and the design **shall** take this into account to meet the stability (Higher CTR) and the transient response requirements (Lower CTR). Design should also take into account degradation of CTR over time, due to increased ambient temperature, increased LED current and increased radiation exposure when operating at higher altitudes. Design should also take into account low temperature (storage) conditions that may affect opto-isolator performance characteristics. This requires working with the opto-isolator manufacturer to determine the applicable sensitivities.
- The diode current can be specified at the lowest possible level but still **shall** be close to one of the specified operating points.
- If the base connection is available, use a resistor across the base to emitter of the output transistor to reduce the noise pick-up.
- Use a resistor in series with LED to limit the current through the diode. Proper circuit layout **shall** be considered to reduce stray capacitance coupling.

# APPENDIX A-1
# Reliability Terms and Definitions

- **AFR –** Annualized Failure Rate - The average failure rate of a population of products normalized to one year.
- **MTBF –** Mean Time Between Failure (Hours)
  - MTBF (measured) = Σ Operating Hours ÷ Σ Failures.
  - Applied to a population of products, this term applies *during* useful life when failure rates are relatively constant.
  - MTBF *is not* a measure of how long a power supply can be expected to survive.
- **FIT –** Failures in Ten to the Ninth ($10^9$) hours of operation - This term is commonly used to define individual component reliability failure rates but can also be applied to power supplies.
  - 1 FIT = 1 Failure/1,000,000,000 devices hours.
  - FIT rate (measured) = Σ Failures ≈ Σ Operating Hours x $10^9$.
  - MTBF = $10^9$/Σ FIT.
- **Useful Life** (see Service Life definition in 2.4) – Minimum time, specified in years, during which failure rates are constant or decreasing and cumulative failures for a single wearout failure mechanism do not exceed 1%.

Table A-1-1 demonstrates how the terms MTBF, AFR and FIT can be used interchangeably with appropriate scaling factors. All of these terms apply to the period of time from initial installation up to the end of the product's useful life (onset of wearout). These terms only apply to populations of products used over long periods of time (typically 1 year minimum). The terms do not apply to an individual unit or to instantaneous failure rates. None of the terms in Table A-1-1 specify how long a single unit or population of products will operate before onset of wearout or end of Useful Life.

Useful life is determined by identifying the failure mechanism(s) which is (are) associated with end of life. Examples of these mechanisms include Electrolytic capacitors (electrolyte evaporation); Fans (bearing/grease wear); solder joints (cyclic fatigue) and ceramic capacitors (Oxygen Vacancy Migration), just to name a few. To determine useful life, a product should be analyzed to determine all possible wearout mechanisms that might occur during the product specified useful life. Each of the potential contributors to wearout should be tested or modeled to determine which mechanism dominates under anticipated worst case customer use conditions.

Table A-1-1 can be used in spreadsheet format. The shaded cells are used to enter the number to be converted. The white cells contain conversion formulas based on the shaded cell in the same row. For example, a user has a measured AFR of 1%/year. Entering 1.0 into the shaded cell under "**%def/yr**" yields **MTBF** = 876000; **FIT** = 1142.

**Table A-1-1 Conversions Between MTBF, AFR and FIT**

| MTBF | AFR | | FIT |
|---|---|---|---|
| (Hours) | % def/yr | ppm/yr | failures/ $10^9$ hrs |
| 1,752,000 | 0.5 | 5,000 | 571 |
| 876,000 | 1.0 | 10,000 | 1,142 |
| 438,000 | 2.0 | 20,000 | 2,283 |
| 219,000 | 4.0 | 40,000 | 4,566 |
| = $10^9$/FIT | = 876,000/MTBF | = 87.6/MTBF | = $10^9$/MTBF |

**Example:**

Customer installs 100 power supplies which operate 24 hours/day, 365 days/year (8760 hours/year). Calculate reliability as **MTBF**, **AFR** and **FIT** rate.

- First year: 2 out of 100 units failed (note - assume failures repaired and immediately put back into service).

$$\mathbf{MTBF} = \frac{\Sigma \text{Operating Hours}}{\Sigma \text{Failures}}$$

$$\mathbf{Hours/Year} = \frac{365\ days}{year} \times \frac{24\ hours}{day} = 8{,}760\ hours/year$$

$$\mathbf{MTBF} = \frac{100\ units \times 8{,}760\ hours/year}{2\ failures/year} = 438{,}000\ hours/failure$$

$$\mathbf{AFR} = \frac{2\ failures/year}{100\ units} \times 100 = 2\%/year$$

$$\mathbf{FIT} = \frac{2\ failures/year}{8{,}760\ hours/year} \times 10^9\ hours = 2{,}283\ FITs$$

- Second year: 1 out of 100 units failed.

$$\mathbf{MTBF} = \frac{100\ units \times 8{,}760\ hours/year}{1\ failure/year} = 876{,}000\ hours/failure$$

$$\mathbf{AFR} = \frac{1\ failure/year}{100\ units} \times 100 = 1\%/year$$

$$\mathbf{FIT} = \frac{1\ failure/year}{8{,}760\ hours/year} \times 10^9\ hours = 1{,}142\ FITs$$

- Year 1 + Year 2: 3 out of 100 units failed.

$$\mathbf{MTBF} = \frac{100\ units \times 17{,}520\ hours/2\ years}{3\ failures/2\ years} = 584{,}000\ hours/failure$$

$$\mathbf{AFR} = \frac{3\ failures/2\ years}{100\ units} \times 100 = 1.5\%/year$$

$$\mathbf{FIT} = \frac{3\ failures/2\ years}{17{,}520\ hours/2\ years} \times 10^9\ hours = 1{,}712\ FITs$$

In this last example, **MTBF** = 584k hours = 67 years. This *does not* represent Useful Life; i.e., it does not mean that any given power supply can survive 67 years. In fact, most power supplies have Useful Life of 5 to 20 years, depending on design and customer use conditions.

# APPENDIX B
## Typical Comprehensive Data Sheets

The datasheet **shall** be dated and have its revision level marked. An example of typical data sheet information is shown below. Values in examples are realistic but hypothetical. The first example is for an ac to dc power supply with multiple dc outputs:

**IPC-9592 - Class 1**

***Input Specifications:***

| | |
|---|---|
| Input voltage | 85-265 Vac |
| Frequency | 47-440 Hz |
| Inrush current | 25 A peak maximum |
| Efficiency | 75% minimum @ full load |
| Power factor | 0.99 typ. meets EN61000-3-2 |
| Turn-on time | ac on 1.0 sec typ., 1.8 sec maximum Inhibit/Enable 150 ms typ., 200 ms maximum |
| Conducted EMI | CISPR 22 EN55022 Level "B" |
| Radiated EMI | CISPR 22 EN55022 Level "B" |
| Harmonic distortion | Meets IEC 61000-3-2 |
| Isolation | Meets IEC 60950 |
| Leakage current | 2.0 mA maximum @ 240 Vac |
| Holdover storage | 20 ms minimum (independent of input Vac) |
| ac OK | >5 ms early warning before outputs lose regulation. Full cycle ride thru (50 Hz) |
| Global Inhibit/Enable | TTL, Logic "1" and Logic "0" |
| Input fuse (internal) | 20A |
| Warranty | 3 years |

***Output Specifications:***

| | |
|---|---|
| Number of Outputs | Three |
| Nominal Output Voltages | +5 Vdc, -15 Vdc, +15 Vdc |
| Adjustment range | ± 5% minimum all outputs |
| Margining | ± 2-3% nominal |
| Overall regulation | 0.25% or 15 mV maximum |
| Ripple | RMS: 0.1% or 10 mV, whichever is greater - bandwidth limited to 20 MHz<br>Pk-Pk: 1.0% or 50mV, whichever is greater - bandwidth limited to 20 MHz |
| Dynamic response | <2% or 100 mV, with 25% load step |
| Recovery time | To within 1% in <200 µsec |
| Overcurrent protection | 105-120% of rated output current |
| Short circuit protection | Protected for continuous short circuit, automatic recovery |
| Overvoltage protection | Separate, each output |
| Reverse voltage protection | 100% of rated output current |
| Thermal protection | All outputs disabled when internal temperature exceeds safe operating range |
| Remote sense | Up to 0.5V total drop |
| Single wire parallel | Current share to within 2% of total rated current |
| dc OK | -2% to -8% of nominal for any monitored output |
| Minimum load | Not required |
| Module inhibit | TTL, isolated |
| Switching frequency | 250 kHz |
| Output/Output isolation | >1 Megohm |

***Environmental Specifications:***

| | |
|---|---|
| Storage temperature | -40 °C to +85 °C |
| Operating temperature | -20 °C to 50 °C (start @ 0 °C) (derate power of each output linearly starting at 50 °C to 50% power at 70 °C) |
| Thermal shock (nonoperating) | -40 (± 5) to +70 (± 5) degrees Celsius, transition time not to exceed 5 minutes. |
| Storage vibration | 2.2 Grms, 5-500Hz, 15 minutes per side |
| Operating vibration | 0.5 Grms, 5-800Hz, 30 minutes per side |
| Nonoperating shock | 142 G ± 5% with pulse duration of 2 msec ± 10% |
| Operating shock | 82 G ± 5% with pulse duration of 2 msec ± 10% |
| Humidity | 95% noncondensing |
| Temperature coefficient | 0.02% per °C |
| Cooling | Internal dc fan |

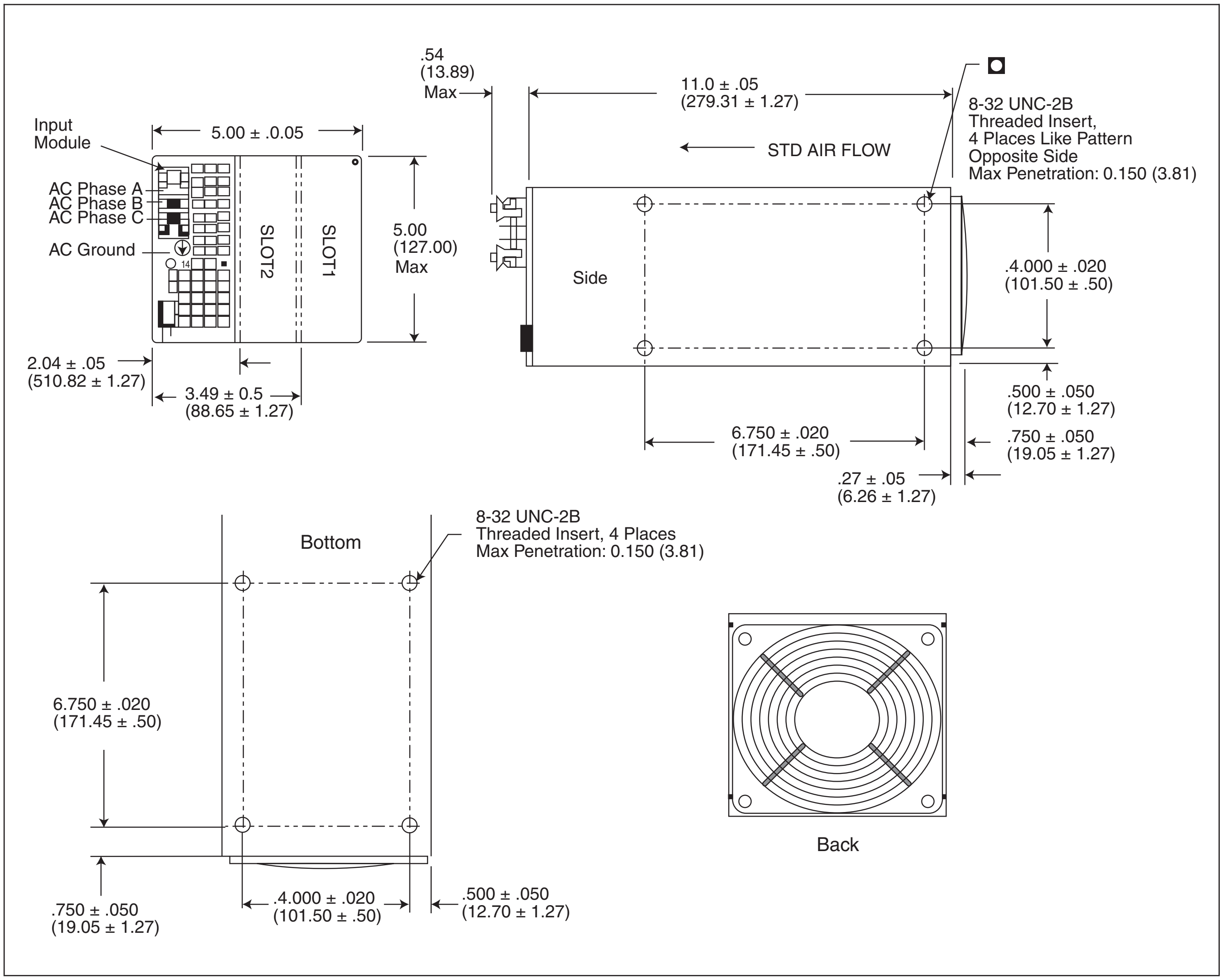
***Reliability:***

| | |
|---|---|
| FIT | 2500 FITS, 100% duty cycle at 40 °C ambient, 45% RH ± 10%, 90% total output load, any specified input voltage, sea level operation per Telcordia Technologies, SR-332 |
| Service Life | 5 years |

***Safety & Regulatory:***

| | |
|---|---|
| UL | UL 60950 |
| CSA | CSA22.2 No. 234 Level 5 |
| IEC | IEC 60950-1 Class 1 |
| VDE | IEC 60950-1 |
| BABT | Compliance to IEC 60950-1, BS 7002 |
| CB | Certificate and report |
| CE | Mark |
| EMI/EMC Characteristics | IEC 61000-4-5 level 2, EN 55022, class B |
| ESDIEC | 61000-4-2 level 4 |

***Physical Dimensions and Electrical Connections:***



**Weight: 5 kg/11 pounds**

**(These drawings were originally published by Aztec/Emerson in their literature.)**

The following example is for a dc to dc power converter with multiple dc outputs:

**IPC-9592 - Class 2**

### *Input Specifications:*

| | |
|---|---|
| Input voltage range | 10.8 - 13.2 Vdc |
| Input reverse voltage protection | Fuse recommended |
| Input filter | Capacitor Low ESR |
| Efficiency | 60-80% typical; 55% minimum |

### *Output Specifications:*

| | |
|---|---|
| Number of outputs | 2 |
| Output 1 voltage | -12 Vdc |
| Output 2 voltage | +12 Vdc |
| Voltage tolerance, each output | ± 2.0% |
| Line regulation, each output | ± 1.0% |
| Load regulation | ± 0.5% |
| Noise/ripple | 1% mV P-P (20 MHz bandwidth). Note: An external 0.1µf ceramic Capacitor is recommended to be placed from +V out to -V out. |
| Short circuit protection | 20 Second Duration |
| Transient response | 200 µsec max (50% load change to within 1% VO Nom) |
| Switching frequency | 25kHz typ |
| Temperature coefficient | ± 0.025%/°C |

### *Isolation:*

| | |
|---|---|
| I/O isolation | >500 Vdc |
| Isolation resistance | >1 x $10^9$ ohms |

### *Environmental:*

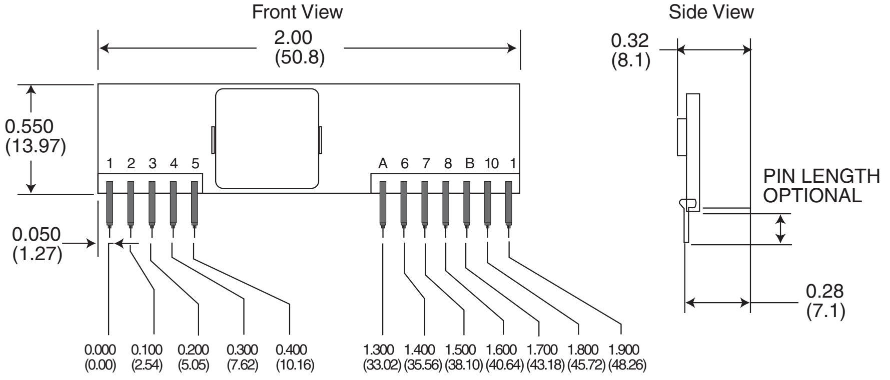
| | |
|---|---|
| Operating ambient temperature | -25 °C to +85 °C (full load) |
| Auto-shutdown temperature | 95 °C minimum |
| Storage temperature | -55 °C to +105 °C |
| Thermal shock (nonoperating) | -40 (± 5) to +85 (± 5) degrees Celsius, transition time not to exceed 2.5 minutes |
| Operating humidity | 5% to 95% (noncondensing) |
| Cooling method | Convection |
| Storage vibration | 2.5 Grms, 5-500Hz, 15 minutes per side |
| Operating vibration | 0.75 Grms, 5-800Hz, 30 minutes per side |
| Nonoperating shock | 175 G ± 5% with pulse duration of 2 msec ± 10% |
| Operating shock | 90 G ± 5% with pulse duration of 2 msec ± 10% |
| Reliability | 1000 FITS, 100% duty cycle at 30 °C ambient, 45% RH ± 10%, 100% total output load, any specified input voltage, sea level operation per Telcordia Technologies, SR-332 |
| Service Life | 15 years |

### *Agency Approvals:*

| | |
|---|---|
| Safety | UL1604, IEC 60950-1 CE Marked Low Voltage Directive |
| EMI/EMC Characteristics | IEC 61000-4-5 level 2, British Telecom BTR 2511- Issue 2, EN 55022, class B |
| ESD | IEC 61000-4-2 level 4 |

### *Physical Dimensions and Electrical Connections:*

SIP (Single In-Line Through Hole Package) Mechanical Drawing Pin Dimensions:
Through Hole: Pin diameters are 0.025 in (0.64 mm)
Dimensions are in inches and (millimeters)
Tolerances: x.xx in ± 0.02 in (x.x mm ± 0.5 mm)
x.xxx in ± 0.010 in (x.xx mm ± 0.25 mm)



| Pin | Function |
|---|---|
| 1 | $V_{out}$ |
| 2 | $V_{out}$ |
| 3 | SENSE |
| 4 | $V_{out}$ |
| 5 | GND |
| A | I Share |
| 6 | GND |
| 7 | $V_{in}$ |
| 8 | $V_{in}$ |
| B | SEQ |
| 9 | TRIM |
| 10 | ON/OFF |

**Weight: 12 grams/0.45 oz**
**Case Material: XXX plastic**

**(This drawing was originally published by DOSA in their literature.)**

# APPENDIX C

The PCD manufacturer **shall** conduct a functional test on samples of products during Development (Design Verification Test - DVT) and 100% of products during manufacturing (Manufacturing Test Requirement - MTR). All test results **shall** be compliant with the product specification.

All tests listed **shall** be performed on DVT samples. Manufacturing testing **shall** be performed as shown under the ‘‘Production MTR’’ column. All references to minimum and maximum values refer to the parameters defined in the Electrical Requirements Specification. Any exception requires documented approval from the user. The general test items for power supply testing include, but are not limited to, the following items listed in the tables below (Tables C-1 through C-3). Some parameters, such as logic timing and logic signals, are product specific. Other tests may not be applicable. Always reference the Electrical Requirements Document.

All DVT tests are conducted at *both* ***Mininum Temperature*** *and* ***Maximum Temperature*** as defined in the product specification unless specifically stated otherwise. ‘‘Start Up’’ and ‘‘Steady State’’ in the table below refer to whether the test is conducted when the unit is first turned on (Start Up) or after it has thermally stabilized (Steady State). *All* MTR tests are at room ambient *RA* and Start Up.

# APPENDIX C-1 for Category 1

## ac to dc and dc Input PSU Functional Test Requirements

| Test Name | Test Condition<br>All tests to be performed on DVT samples | Units | Production MTR |
|---|---|---|---|
| Inrush Current (first test in Production MTR) | Maximum input voltage, maximum dc load, Start Up | Amps | Yes |
| | Minimum input voltage, maximum dc load, Start Up | | No |
| | Maximum input voltage, maximum dc load, Steady State | | |
| PSU Turn-On Voltage | Minimum and maximum dc load | Vac | Note 1 |
| PSU Turn-Off Voltage | Minimum and maximum dc load | Vac | Note 1 |
| Efficiency | Minimum input voltage, maximum dc load, Start Up | % | Yes |
| | Maximum input voltage, maximum dc load, Steady State | | No |
| | Minimum input voltage, maximum dc load, Steady State, maximum temperature | | |
| | Other defined energy efficiency requirements (example: Energy Star) | | As Required |
| Standby Input Power | Maximum input voltage, minimum dc load, Start Up | W | As Required |
| | Maximum input voltage, maximum dc load, Start Up | | |
| | Other defined energy measurement requirements (example: Blue Angel) | | |
| Auto-Restart Test | Maximum and minimum input voltage, minimum and maximum dc load, For 25ms, 40ms, 60ms, 90ms, 130ms, 1.3S, 2.0S dropout | Pass/ Fail | No |
| Hold-Up Time (Note 3) | Maximum input voltage, minimum and maximum dc load, Start Up | ms | No |
| | Minimum input voltage, minimum dc load, Start Up | | |
| | Minimum input voltage, maximum dc load, Start Up | | Yes |
| PFC (not applicable for dc Input) | Maximum ac input voltage, Start Up, for 20% dc load | unitless | Note 1 |
| | Maximum ac input voltage, 50% and 90% dc load, Start Up | | |
| | Minimum ac input voltage, 20% and 50% dc load, Start Up | | |
| | Minimum ac input voltage, 90% dc load, Start Up | | |
| Output Load Regulation | Minimum and maximum input voltage, minimum and maximum dc load (various loading combinations need to be considered for multiple output supplies to assure there are no cross-regulation issues) | V | No |
| dc Output Monotonic | Minimum and maximum input voltage, minimum and maximum dc load | Pass/ Fail | No |
| Remote Sense Regulation | Minimum and maximum input voltage, minimum and maximum dc load | mV | Note 1 |
| Output Ripple | Minimum and maximum input voltage, minimum and maximum dc load | mV pk-pk | Note 1 |
| Output Transient | Maximum and minimum input voltage, Start Up | mV pk-pk | Note 1 |
| | Maximum and minimum input voltage, Steady State | | No |
| Output Overcurrent | Minimum and maximum input voltage | A | Note 1 |
| Overvoltage Protection | Minimum and maximum input voltage, minimum and maximum dc load | V | Note 1 & Note 2 |
| Undervoltage Protection | Minimum and maximum input voltage, minimum and maximum dc load | V | No |
| Logic Timings | Minimum and maximum input voltage, minimum and maximum dc load | ms | Note 1 |
| Current Sharing (if applicable - requires 2 or more power supplies) | Minimum and maximum input voltage, minimum and maximum dc load, Start Up | % | Note 1 |
| | Minimum and maximum input voltage, minimum and maximum dc load, Steady State | | No |
| Fan Speed Test (if applicable) (second *test in Production MTR*) | Minimum and maximum input voltage, minimum dc load, Start Up | rpm | Note 1 |
| | Maximum input voltage, minimum dc load, Start Up, RA | | |
| | Minimum input voltage, maximum dc load, Steady State, RA | | |
| | Maximum input voltage, minimum dc load, Start Up | | |
| | Minimum input voltage, maximum dc load, Steady State | | |

| Test Name | Test Condition<br>All tests to be performed on DVT samples | Units | Production MTR |
|---|---|---|---|
| Output Sequencing | Test per Electrical Requirements Document | Pass/ Fail | Note 1 |
| Thermal Protection | Test per Electrical Requirements Document | Pass/ Fail | No |
| Logic Signals (voltage and current levels) | Test per Electrical Requirements Document | Pass/ Fail | Note 1 |
| LED Indicators | Test per Electrical Requirements Document | Pass/ Fail | Yes |
| EEPROM contents | Test per Electrical Requirements Document | Pass/ Fail | Yes |

**Note 1:** After supplier completes required DVT test matrix, the supplier identifies and selects the worst case condition for the Production MTR. It is not required that all test conditions be tested.
[Example: If worst case condition for OVP (Overvoltage Protection) is maximum input voltage and minimum dc load, then that is the test condition to be used.]

**Note 2:** Where feasible.

**Note 3:** When testing at minimum specified operating conditions, allow sufficient time for unit to self heat before making measurement.

# APPENDIX C-2 for Category 2

### dc to dc BMP and POL Functional Test Requirements

| Test Name | Test Condition All tests to be performed on DVT samples | Units | Production MTR |
|---|---|---|---|
| Start up Input Current | Maximum input voltage, minimum dc load, Start Up | Amps | Yes |
| Worst Case Input Current | Minimum input voltage, maximum dc load | Amps | No |
| PSU Turn-On Voltage | Minimum and maximum input voltage, minimum and maximum dc load | Vdc | No |
| PSU Turn-Off Voltage | Minimum and maximum input voltage, minimum and maximum dc load | Vdc | No |
| Efficiency | Minimum and maximum input voltage, maximum dc load, Start Up/hot | % | Note 1,2 |
| | Other defined energy efficiency requirement (example: Energy Star) | | As Required |
| Output Load Regulation | Nominal input voltage, minimum and maximum dc load<br>(various loading combinations need to be considered for multiple output supplies to assure there are no cross-regulation issues) | % | Yes |
| Line Regulation | Minimum and maximum input voltage, maximum dc load | % | Yes |
| Vout adjustment Range - Trim Up/Trim Down (as applicable) | Nominal input voltage, open, trim low, trim high | Pass/ Fail | Yes |
| dc Output Startup Monotonic | Minimum and maximum input voltage, minimum and maximum dc load, minimum and maximum output capacitance | Pass/ Fail | No |
| Output Ripple | Minimum and maximum input voltage, minimum and maximum dc load | mV pk-pk & mV rms | Note 1 |
| Transient Response | Nominal input voltage, step load from 50% to 100%, minimum and maximum capacitance | Pass/ Fail | No |
| Output Overcurrent (Current Limit Inception) | Minimum and maximum input voltage, Start Up/Steady State | A | Note 1 |
| Output Short Circuit | Minimum and maximum input voltage, minimum and maximum load | Pass/ Fail | Note 1 |
| Output Overvoltage Protection (OVP) | Minimum and maximum input voltage, minimum and maximum dc load | V | Note 1 & Note 3 |
| Output Sequencing (as applicable) | Test per Electrical Requirements Document | Pass/ Fail | No |
| Thermal Protection | Test per Electrical Requirements Document | Pass/ Fail | No |
| Logic Signals | Test per Electrical Requirements Document | Pass/ Fail | Yes |

**Note 1:** After supplier completes required DVT test matrix, the supplier identifies and selects the worst case condition for the Production MTR. It is not required that all conditions be tested in production.

Example: If worst case condition for OVP (Overvoltage Protection) is maximum input voltage and minimum dc load, then that is the test condition to be used.

**Note 2:** Use Nominal Input Voltage if Maximum/Minimum input voltage not specified.

**Note 3:** Where feasible.

# APPENDIX C-3 for Category 3

## ac to dc Adapter Functional Test Requirements

| Test Name | Test Condition | Units | Production MTR |
|---|---|---|---|
| Inrush Current (*first test in Production MTR*) | Minimum and Maximum input voltage, maximum dc load, Start Up | Amps | Note 1 |
| | Maximum input voltage, maximum dc load, Steady State | | No |
| PSU Turn-On Voltage | Minimum and maximum input voltage, minimum and maximum dc load | Vac | Note 1 |
| PSU Turn-Off Voltage | Minimum and maximum input voltage, minimum and maximum dc load | Vac | Note 1 |
| Efficiency | Minimum input voltage, maximum dc load, Start Up | % | Yes |
| | Maximum input voltage, maximum dc load, Steady State | | No |
| | Minimum input voltage, maximum dc load, hot, maximum temperature | | No |
| | Other defined energy efficiency requirements (example: Energy Star) | | As Required |
| Standby Input Power | Maximum input voltage, minimum and maximum dc load, Start Up | W | As Required |
| | Other defined energy measurement requirements (example: Blue Angel) | | As Required |
| Auto-Restart Test | Maximum and minimum input voltage, minimum and maximum dc load, For 25ms, 40ms, 60, ms, 90ms, 130ms, 1.3S, 2.0S dropout | Pass/ Fail | No |
| Hold-Up Time | Maximum input voltage, minimum and maximum dc load, Start Up | ms | No |
| | Minimum input voltage, Minimum and Maximum dc load, Start Up | | Note 1 |
| PFC (not applicable for dc Input) | Maximum ac input voltage, Start Up, for 20% dc load | unitless | Note 1 |
| | Maximum ac input voltage, 50% and 90% dc load, Start Up | | |
| | Minimum ac input voltage, 20% and 50% dc load, Start Up | | |
| | Minimum ac input voltage, 90% dc load, Start Up | | |
| Output Load Regulation | Minimum and maximum input voltage, minimum and maximum dc load (various loading combinations need to be considered for multiple output supplies to assure there are no cross-regulation issues) | V | Note 1 |
| dc Output Monotonic | Minimum and maximum input voltage, minimum and maximum dc load | Pass/ Fail | Note 1 |
| Remote Sense Regulation | Minimum and maximum input voltage, minimum and maximum dc load | mV | Note 1 |
| Output Ripple | Minimum and maximum input voltage, minimum and maximum dc load | mV pk-pk | Note 1 |
| Output Transient | Maximum and minimum input voltage, Start Up | mV pk-pk | Note 1 |
| | Maximum and minimum input voltage, Steady State | | No |
| Output Overcurrent | Minimum and maximum input voltage | A | Note 1 |
| Output Short Circuit | Minimum and maximum input voltage | Pass/ Fail | Note 1 |
| Overvoltage Protection | Minimum and maximum input voltage, minimum and maximum dc load | V | Note 1 |
| Undervoltage Protection | Minimum and maximum input voltage, minimum and maximum dc load | V | No |
| Logic Timings | Minimum and maximum input voltage, minimum and maximum dc load | ms | Note 1 |
| Current Sharing (if applicable - requires 2 or more power supplies) | Minimum and maximum input voltage, minimum and maximum dc load, Start Up | % | Note 1 |
| | Minimum and maximum input voltage, minimum and maximum dc load, Steady State | | No |
| Fan Speed Test (if applicable) (second *test in Production MTR*) | Minimum and maximum input voltage, minimum dc load, Start Up | rpm | Note 1 |
| | Maximum input voltage, minimum dc load, Start Up, RA | | |
| | Minimum input voltage, maximum dc load, Steady State, RA | | |
| | Maximum input voltage, minimum dc load, Start Up | | |
| | Minimum input voltage, maximum dc load, Steady State | | |

| Test Name | Test Condition | Units | Production MTR |
|---|---|---|---|
| Output Sequencing | Test per Electrical Requirements Document | Pass/ Fail | Note 1 |
| Thermal Protection | Test per Electrical Requirements Document | Pass/ Fail | No |
| Logic Signals (voltage and current levels) | Test per Electrical Requirements Document | Pass/ Fail | Note 1 |
| LED Indicators | Test per Electrical Requirements Document | Pass/ Fail | Yes |
| EEPROM contents | Test per Electrical Requirements Document | Pass/ Fail | Yes |

**Note 1:** After supplier completes required DVT test matrix, the supplier identifies and selects the worst case condition for the Production MTR. It is not required that all test conditions be tested.

Example: If worst case condition for OVP (Overvoltage Protection) is maximum input voltage and minimum dc load, then that is the test condition to be used.

# APPENDIX C-4

## DESCRIPTION OF FUNCTIONAL TESTS

The ac or dc source mentioned in this section must be a programmable source to supply input power to the PCD. E-load must be a programmable load. E-load set in constant current mode serves as a dc load to the PCD.

**C-4.1 Inrush Current Test** This test is to verify that when input power is applied to the PCD, any current surge or spike of input current should not exceed the limit defined by the specifications. The inrush current due to EMI filter capacitors can be ignored.

### C-4.1.1 Test Condition

Perform the test with minimum and maximum Vin.

Perform the test with maximum load (note: inrush is not normally dependant on load. PFC Turn-on current is load dependant to some extent.).

### C-4.1.2 Test Setup

Set source output to maximum Vin specified by the specification.

Set E-loads to maximum load which is full load of PCD but not to exceed total power supply watts.

Enable PS_ON.

Enable source output at 90° or 270° phase angle.

Enable E-load.

Verify PCD input peak current within 300ms after source output enable meets specification.

Disable source output, E-loads and PS_ON.

### C-4.1.3 Application Note

Make sure the inrush current is not limited by capacity/setting of source.

Put inrush current test as the first test in test sequence to get cold inrush value.

In case of the PCD failed test and a retest required, production must make sure the capacitors of the PCD are fully discharged and relative components return to room temperature in order to ensure that the measurement value is cold inrush current.

**C-4.2 Overshoot at Turn-On** This test is to verify that the voltage overshoot of each dc output meets the specification.

### C-4.2.1 Test Condition

Perform the test for normal Vin with specified frequency.

Perform the test with minimum and maximum load.

### C-4.2.2 Test Setup

Set source output with specified Vin voltage.

Set E-load of each output rail according to the specification.

Enable PS_ON.

Enable source output and E-loads.

Verify overshoot of each output rail meets the specification.

Repeat test with all conditions.

Disable source output, E-loads and PS_ON.

**C-4.3 Turn-On/Turn-Off Voltage Test** This test is to verify the hysteresis of Turn-on and Turn-off voltage.

### C-4.3.1 Test Condition

Perform the test with maximum load.

Use ac cord of <1 meter and 14GA wire.

### C-4.3.2 Test Setup

Set source voltage below the lower spec of Turn-on with specified frequency.

Set E-loads to maximum which is full load of PCD but not exceeding total power supply watts.

Enable PS_ON.

Enable source and E-load.

Verify the PCD does NOT Turn-on by monitoring the selected dc output and the P-OK signal if applicable to the selected output.

Increment source in steps (steps should be less than 20% of the minimum to maximum spec for Turn-on) until a level is reached above the upper limit of Turn-on, preferably 5 increments beyond Turn-on (to check for power supply stability over this range).

Verify the PCD Turn-on point by monitoring that the selected dc output is within regulation and P-OK signal is true, if applicable.

Set source output to a voltage above the upper limit of Turn-off with specified frequency.

Verify PCD does NOT Turn-off by monitoring the selected dc output and P-OK signal.

Decrement source in steps (steps should be less than 20% of the minimum to maximum spec for Turn-off) until a level is reached below the lower limit of Turn-off, preferably 5 increments beyond Turn-off (to ensure that unit does not come back on).

Verify the PCD Turn-off point by monitoring all applicable dc outputs and P-OK signal if applicable.

**C-4.4 Efficiency** This test is to verify PCD meets or exceeds the minimum efficiency and power dissipation meets or does not exceed maximum dissipation per the specification. Normally low line input is considered as worst case of efficiency and full load is the worst case of power dissipation except claimed by design.

### C-4.4.1 Test Condition

Perform the test with minimum Vin.

Perform the test with maximum Load.

### C-4.4.2 Test Setup

Set source output to minimal Vin specified by the specification.

Set E-loads to maximum which is full load of PCD but not to exceed total power supply watts.

Enable PS_ON.

Enable source output and E-load.

Measure PCD Pout by power meter or equivalent after P-OK signal valid.

Measure PCD Pin by power meter or source.

Calculate Pout/Pin as efficiency, Pin-Pout as maximum power dissipation and verify they meet the specification.

Disable source output, E-loads and PS_ON.

**C-4.5 Standby Input Power and 1W Maximum Power Requirement** This test is to verify the PCD stand by power dissipation does not exceed the specification

### C-4.5.1 Test Setup

Set source output to specified Vin.

Set E-load to specified load.

Disable PS_ON.

Enable source output and E-load.

Verify PCD input power does not exceed spec.

Disable source output, E-loads and PS_ON.

**C-4.5.2 Application Note** Power meter is preferred to conduct this test when source does not have sufficient precision.

**C-4.6 Auto Restart** When source dropoff time is longer than holdup time, power supply is capable of restarting after the input line disturbance.

### C-4.6.1 Test Condition

Perform the test with minimum Vin and maximum Vin.

Perform the test with maximum load.

### C-4.6.2 Test Setup

Set source output with specified Vin voltage.

Set source line disturbance to -100%, time interval to specified value.

Set E-load to specified load.

Enable PS_ON.

Enable source output and E-load.

Verify PCD Turn-off during input disturbance and Turn-on after input resumes by monitoring all dc output and POK.

Repeat test with all test conditions.

Disable source output, E-loads and PS_ON.

**C-4.6.3 Application Note** When input disturbance time is not defined by the specification, factory needs to conduct experiment to pick up the minimum value that can get PCD Turn-off from the following time intervals: 25ms, 40ms, 60ms, 90ms, 130ms, 1.3s, 2.0s.

**C-4.7 Source Dropout** This test is to verify that when dropoff time is shorter than holdup time, all dc output will keep within regulation.

### C-4.7.1 Test Condition

Perform the test with minimum Vin and at zero crossing of the sine wave or AABUS.

Perform the test with maximum load.

### C-4.7.2 Test Setup

Set source output with specified Vin voltage.

Set source line disturbance to -100%, time interval to specified value.

Set E-load to specified load.

Enable PS_ON.

Enable source output and E-load.

Verify all dc outputs keep in regulation during source disturbance.

Disable source output, E-loads and PS_ON.

**C-4.8 PFC - Power Factor Correction Test (only for PCD having PFC)** In case PCD has PFC circuitry, this test is to verify the PFC meets the specification.

### C-4.8.1 Test Condition

Perform the test for minimum and maximum Vin with specified frequency.

Perform the test at 20%, 50% and 90% loads.

### C-4.8.2 Test Setup

Set source output with specified Vin voltage.

Set E-load to specified load.

Enable PS_ON.

Enable source output and E-loads.

Verify the PCD PF meets specification by ac analyzer or equivalent (valid only for PSU with PFC).

Repeat test with all conditions.

Disable source output, E-loads and PS_ON.

**C-4.9 Regulation Test** The power supply dc output must keep in regulation range at output connectors when load condition is within range covered by the specification.

### C-4.9.1 Test Condition

Perform the test for minimum and maximum Vin with specified frequency.

Perform the test for all load conditions defined by the specification.

### C-4.9.2 Test Setup

Set source output with specified Vin voltage.

Set E-load of each output rail according to the specification.

Enable PS_ON.

Enable source output and E-loads.

Verify PCD all output regulation voltage at PCD output connector end meets the specification.

Repeat test with all test conditions.

Disable source output, E-loads and PS_ON.

**C-4.10 Ripple Test** Ripple level of each dc output terminal with all working conditions must not exceed limit described in the specification.

### C-4.10.1 Test Condition

Perform the test for minimum and maximum Vin with specified frequency.

Perform the test with minimum and maximum load.

### C-4.10.2 Test Setup

Set source output with specified Vin voltage.

Set E-load of each output rail according to the specification.

Enable PS_ON.

Enable source output and E-loads.

Verify ripple of all PCD output channel by O-scope or equivalent with BW set to 20MHz while monitoring the dc output voltage meets the specification.

Repeat test with all conditions.

Disable source output, E-loads and PS_ON.

**C-4.10.3 Application Note** The PCD outputs will be bypassed with one 0.1μF multilayer (type X7R) and one 10μF (low ESR) capacitors. Outputs will be tested per the setup in Figure C-4-1.

**C-4.11 Transient Load Test** Transient load test is to verify the PCD outputs can still be in regulation when applying transient load to each dc output terminal. Output voltage undulation must not exceed the specification.

**C-4.11.1 Test Condition** Perform the test for minimum and maximum Vin with specified frequency.

### C-4.11.2 Test Setup

Verify proper output capacitance is on test fixture per Electrical Requirements Document.

Set source output with specified voltage.

Setup transient load (Starting Load, Load Step, current slew rate, Frequency and duty cycle per specification) for one of the output channels while keeping the load in specification for all other channels.

Enable PS_ON.

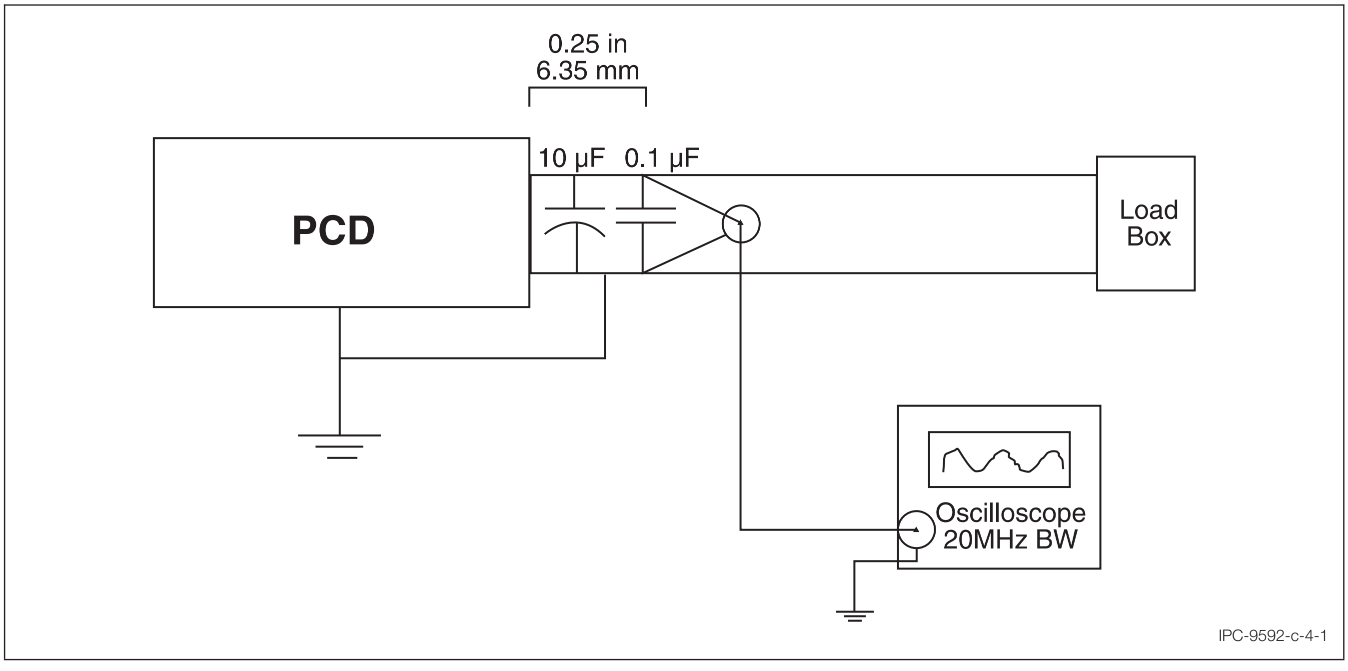


**Figure C-4-1 Ripple Test Setup for dc Output Measurement** (Alternate circuit or method may be used - Test setup **shall** specify output capacitance and type of capacitor used)

Enable source output and E-loads.

Verify the overshoot and undershoot of channel which transient load added meets specification while monitoring all other output channel voltage in regulation specification.

Repeat test with all conditions.

Disable source output, E-loads and PS_ON.

**C-4.11.3 Application Note** Set the transient load to 1kHz with 50% duty cycle except where the specification calls for other values.

**C-4.12 Overcurrent Protection** This test is to verify the function of overcurrent protection circuit.

### C-4.12.1 Test Condition

Perform the test for minimum and maximum Vin with specified frequency.

### C-4.12.2 Test Setup

Set source output with specified Vin voltage.

Set one dc output rail to maximum load and other dc output set to 50% load.

Enable PS_ON.

Enable source output and E-load.

Verify PCD Turn-on by monitoring dc output and POK.

Increase full load channel current to a value that is 1% below the lower limit of OCP with a 10A/s slew rate.

Verify that PCD is not in overcurrent protection mode by monitoring all dc output and P-OK signal.

Increase load of full load channel to the upper limit of OCP with 10A/s slew rate.

Verify PCD in overcurrent protection mode by monitoring all dc output and P-OK signal.

Repeat the test for all specified dc output channels with all test conditions.

Disable source output, E-loads and PS_ON.

**C-4.13 Short Circuit Protection** To verify the short circuit on any dc output terminal will trigger the short circuit protection function.

### C-4.13.1 Test Condition

Perform this test with any voltage within normal Vin range.

Perform this test at minimum load.

### C-4.13.2 Test Setup

Set source output with specified Vin voltage.

Set E-load according to the specification.

Enable PS_ON.

Enable source output and E-load.

Short one of the output channels (except Vsb) by an impedance less than 0.1 Ω.

Verify all other outputs of PCD latch off except Vsb.

Remove short.

Reset PCD by source or PS-ON.

Repeat test for all output channels except Vsb.

Short Vsb channel by impedance less than 0.1 Ω.

Verify PCD all other output channels shut down.

Remove short on Vsb.

Verify Vsb resume.

Disable source output, E-loads and PS_ON.

**C-4.13.3 Application Note** If OCP and UVP circuits are separate, verify that OCP functions during a short before the UVP circuit activates. An OCP circuit must meet any delay spec required to prevent false triggering during load transients. OCP must meet any $I^2t$ spec for maximum power dissipation during short.

**C-4.14 Overvoltage Protection** This test is to verify the function of overvoltage protection circuit

**C-4.14.1 Application Note** The OVP test should be run at the finished goods level. The test should verify that the PCD does not trigger the OVP mode at LSL, but does trigger the OVP at USL. In case the product design does not allow an OVP test at the finished goods level, a board level OVP test **shall** be run, instead.

**C-4.15 Undervoltage Protection** This test is to verify the function of undervoltage protection circuit

**C-4.15.1 Application Note** The OVP test should be run at the finished goods level. The test should verify that the PCD does not trigger the OVP mode at LSL, but does trigger the OVP at USL. In case the product design does not allow an OVP test at the finished goods level, a board level OVP test **shall** be run, instead.

**C-4.16 Power Time Test** This test is to verify the logic sequence and timing between each electrical event during PCD power-up and power-down stage. The following diagram (Figure C-4-2) is a guide of timing definition only. Refer to the specification for actual timing requirement.

### C-4.16.1 Test Condition

Perform test with minimum and maximum Vin.

Perform test with minimum and maximum load.

### C-4.16.2 Test Setup

Set source output to specified Vin.

Set E-loads according to the specification.

Enable PS_ON.

Enable source output and E-load.

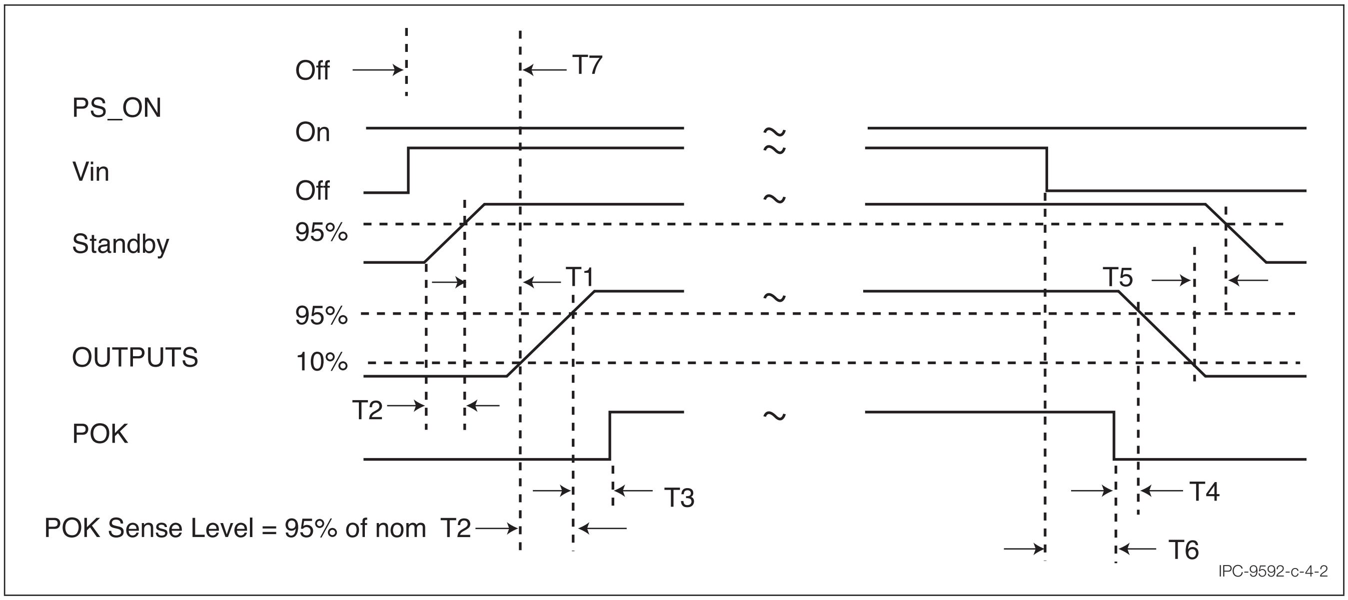


**Figure C-4-2 Timing Definition Guideline**
Above is an example of Turn-on timing signals. And below is an example of Turn-off timing signals.

Verify T1, T2, T3, T7 meet specifications.

Disable source output.

Verify T4, T5, T6 meet specifications.

Disable PS-ON.

Enable source output.

Enable PS_ON.

Verify T2, T3, T9 meet specifications.

Disable PS_ON.

Verify T4, T8 meet specifications.

Repeat test for all test conditions.

Disable source output, E-loads and PS_ON.

**C-4.17 Current Sharing** This test is to verify the redundant power supply current sharing accuracy meets the specification.

Current sharing testing **shall** be performed on at least three different pairs of the sample devices. For example, if three devices labeled A, B and C are being tested, then the current sharing tests **shall** be performed with A and B in parallel, A and C in parallel and B and C in parallel.

If, for example, five devices (A, B, C, D, E) were being tested because that was the maximum number that could be paralleled, then any three of the ten possible combinations would be acceptable as long as one particular device was not used in each of the three combinations. That is, the combinations AB, AC and AD would not be acceptable but the combinations AB, BC and DE would be acceptable.

Current sharing testing **shall** also be performed on a test setup with the maximum number of samples operating in parallel permitted by the product's specification.

Each pair of the sample units **shall** be configured per the supplier's instructions for current sharing operation. Measurements of the output current of each device and the total load current **shall** be taken as the total load current varies from the minimum load current of one device to, for example, 120% of the maximum rated output current of the combined devices.

The output voltage of the combined output **shall** meet the same requirements as the output voltage of a single device.

The maximum difference in the output current of the two devices **shall not** exceed a value equal to 10% of the rated output current of a single device. Note that, when the total output load current is less than 10% of the maximum rating of a single device, it is permissible for one device to supply no output current and the other device to supply the total load current.

With the combined output load set to the maximum rated output current of one device, one of the two devices **shall** be turned off or disabled such that it stops transmitting power to its output. The output voltage of the combined devices **shall** be monitored with an oscilloscope and **shall** stay within the total regulation band of one device during and after the shutdown of the disabled device.

With the combined output load set to the maximum rated output current of one device, one device **shall** be operating and one device **shall** be disabled. The disabled device **shall** be activated so that it starts transmitting power to its output. The output voltage of the combined devices **shall** be monitored with and oscilloscope and **shall** stay within the total regulation band of one device during and after the newly activated device is turned on.

While the output of the two samples is operating at the maximum rated combined output of the two devices, a short circuit sufficient to reduce the output voltage to less than 10% of the nominal output voltage **shall** be applied for 10 ms. The short circuit **shall** be removed and the output voltage observed with an oscilloscope. The output voltage **shall** not overshoot such that an output overvoltage protection feature is activated. The output voltage may not ring or oscillate in such a manner as to become less than the lower limit of the regulation band once it has increased above that value.

The following test **shall** be applied to devices with a current sharing signal line or lines that connect the units being paralleled. With the output current set to the maximum rated value of the combined devices, the signal line or lines **shall** be connected to their signal return. The output voltage of the combined devices **shall** stay within the total regulation band during and after the connection of the signal line or lines to signal return.

### C-4.17.1 Test Condition

Perform the test for normal Vin with specified frequency.

Perform the test with specific load.

### C-4.17.2 Test Setup

Connect a known good PCD to PDB (power distribution board) which can parallel multiple PCDs accurately.

Set source output with specified Vin voltage for the known good PCDs.

Set E-load of PDB according to the specification.

Enable PS_ON.

Enable source output and E-loads.

Connect PCD output to PDB.

Verify the PCD output current meets the specification.

On/Off source of known good PCDs for 2 times each.

Monitor dc output PG such that it has no 'glitch.'

Set E-load of PDB to transient mode per spec.

Verify both known good PCDs must not go into protection mode.

Repeat test with all conditions.

Disable source output, E-loads and PS_ON.

**C-4.18 Hot Swap Test** This test is to verify the performance of the PCD when plugged/unplugged while power and load is applied. Note the term ''Hot'' refers to the fact that the test is performed while energized and has nothing to do with product temperature.

### C-4.18.1 Test Condition

Perform this test with nominal Vin.

Perform the test with maximum load.

**C-4.18.2 Test Setup** One unit is put into the fixture and the output load is set to the maximum rated output load of the device. For custom applications, the customer chassis **shall** be used instead of a test set for Hot Swap testing. The customer chassis **shall** be at maximum loading.

A second device is inserted into the test fixture as recommended by the manufacturer. If the second device includes any kind of insertion level or rate limiting mechanism, these **shall** be in place and used according to the manufacturer's instructions. During and after the insertion into the energized system, the combined output voltage and all device output signals **shall** be monitored with an oscilloscope. With two units inserted into the test fixture and the total output current set to the maximum rated of one device, one of the two units is removed according to the manufacturer's instructions. Any handles, levers or rate limiting mechanisms **shall** be used. After the removal from the energized system, the output voltage and all device output signals **shall** be monitored with an oscilloscope and **shall** stay within the device's specified regulation band. All PCD output signals and indicators **shall** remain valid and problem-free during and after the insertion.

The tests described above **shall** be repeated for at least three combinations of two different sample devices. For devices that specify a maximum number of devices that can have the outputs connected in parallel, the insertion and removal tests **shall** be repeated with at least one configuration of sample devices equal to the maximum specified number.

**C-4.19 Remote Sense Test** This test is to verify that the remote sense is able to compensate for a specified voltage drop between the output connector and the remote sense point. This is often referred to as the distribution loss.

### C-4.19.1 Test Condition

Perform this test with nominal Vin.

Perform the test with maximum load.

### C-4.19.2 Test Setup

Set the source output to nominal Vin.

Set E-loads to the maximum output current for each of the PCD outputs, but do not exceed the PCD output power rating.

Put a resistor in series with the dc output. The voltage drop across the resistor **shall** be greater than or equal to the specified distribution loss.

Float the PCD sense line.

Enable the source output and E-load and power on the PCD.

Verify the output under test meets regulation requirements.

Connect the sense line to the remote sense point.

Verify the output under test meets regulation requirements.

Repeat the test for each output which uses remote sense.

Power off the PCD and disable the source output and E-loads.

**Note:** This test method is primarily a design verification test and it may not be possible to implement into a production test sequence. Alternate test methods are acceptable.

**C-4.19.3 Application Note** If the E-load has a voltage sense line, it may be required to float the load sense during this test. Please refer to the instrument manual for specific requirements.

**C-4.20 PS_ON Threshold Test** This test is to verify the threshold of enable and disable signals while measuring the draw current from system.

#### C-4.20.1 Test Condition

Perform this test at both minimum and maximum input voltage.

Perform the test with maximum load.

#### C-4.20.2 Test Setup

Set source to nominal input voltage per specification.

Set E-load according to the specification.

Enable source output and E-load.

For positive-enabled PCDs, set PS_ON to a voltage lower than Turn-on threshold.

Increment PS_ON voltage in <10mV steps to a level that is higher than where the PCD turns on. (Perform opposite test for negative-enabled PCDs).

Verify PCD has turned on by monitoring P-OK signal (or similar) and that all outputs are within regulation while PS_ON input current does not exceed the specification.

For positive-enabled PCDs, set PS_ON to a voltage that is higher than Turn-off threshold.

Decrement PS_ON voltage in <10mV steps to a level that is lower than where the PCD turns off (perform opposite test for negative-enabled PCDs).

Verify PCD is turned off by monitoring P-OK signal and all outputs while draw current does not exceed the specification.

Disable source output, E-loads and PS_ON.

**C-4.21 Fan Speed Test** This test is to verify fan RPM or flow meets product specification. When possible, both hi/low speeds need to be verified.

**C-4.22 LED Indicator** To verify the function of LED indicator, please refer to PCD specification for test requirement.

**C-4.23 Capacitive Loading** To verify power supply will be able to power up and operate normally with the capacitance defined in the PCD specification.

#### C-4.23.1 Test Condition

Perform this test with any voltage within normal Vin range.

Perform the test with maximum load.

#### C-4.23.2 Test Setup

Add capacitive load to PCD output according to the specification.

Set source output to nominal input voltage per the specification.

Set E-loads to the maximum output current for each of the PCD outputs, but do not exceed the PCD output power rating.

Enable PS_ON.

Enable source output and E-load.

Verify PCD Turn-on by monitoring the P-OK signal and all voltage outputs.

Disable source output, E-loads and PS_ON.

**C-4.24 dc Output Monotonic Start Up** This test is to verify that all dc outputs ramp up monotonically during the Turn-on phase

**C-4.24.1 Test Condition** Perform this test at both minimum and maximum input voltage; perform the test with maximum load

#### C-4.24.2 Test Setup

Set source output to nominal voltage.

Set E-loads to the maximum output current for each of the PCD outputs, but do not exceed the PCD output power rating.

Enable PS_ON.

Enable source output and E-load.

Verify the PCD's dc output voltage ramps up, monotonically with an oscilloscope or differentiator.

Disable source output, E-loads and PS_ON.

**C-4.25 I$^2$C Device Validation** This test is to verify the I$^2$C functionality. Please refer to PCD product specification for test requirement.

**C-4.26 POK Sink Current Test** This test is to verify the PCD can hold POK lower than 0.4Vdc when the POK signal line sinks the maximum current defined by the PCD product specification.

**C-4.27 Vin Good Sink Current Test (Server PSU Only)** This test is to verify the PCD can hold Vin_Good lower than 0.4Vdc when the Vin Good signal line sinks the maximum current defined by the PCD product specification.

**C-4.28 PS On Draw Current Test** This test is to verify the PCD PS_On will not source more than maximum current defined by PCD product specification when PS_On is 0.8V.

**C-4.29 PS Kill Draw Current Test (Server PSU Only)** This test is to verify the PCD PS_Kill will not source more than maximum current defined by PCD product specification when PS_Kill is 0.8V.

**C-4.30 Vin Good Logic Timing Test (Server PSU Only)** This test is to verify VIN_GOOD must be in the correct state (high or low) within 20mS of the Standby output going into regulation.

**C-4.31 Fan Fault Logic Timing Test (Server PSU Only)** This test is to verify the FAN_FAULT signal must be driven low before or at the same time that POK is driven low.

**C-4.32 OTP Logic Timing Test (Server PSU Only)** This test is to verify the OTP signal must be driven low before or at the same time that POK is driven low.

**C-4.33 OTP Test** This test is to verify the function of OTP. It is acceptable to trigger the OTP circuit by simulating an overtemperature condition. One way to do this is to connect a pre-defined resistor in parallel with the NTC resistor.

**C-4.34 Restart After Shutdown** This test is to check for proper operation, if the PCD enters into latch mode. This test checks to see if during latch mode, cycling the PS_On signal to Off and then back to On will reset the PCD. Set the pulse width of the PS_On signal according to the minimum cycle time defined by the product specification.

**C-4.35 No Load Power On Test** This test is to verify PCD can power up without any load. Refer to PCD product spec for output voltage regulation.

**C-4.36 5V, 3.3V Sequencing Test** This test is to verify the 5V output rail stays higher than 3.3V during PCD Turn-on phase. 5V maximum load and 3.3V minimum load are the worst case test conditions.

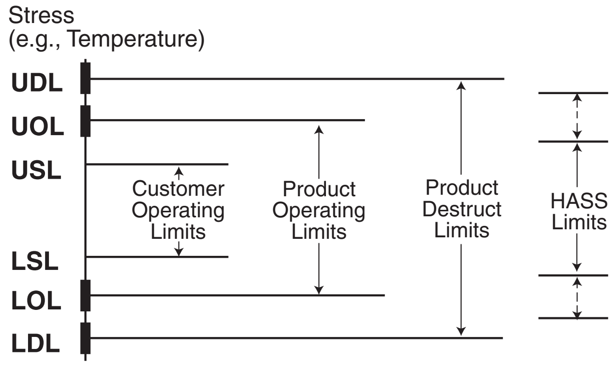
**C-4.37 Vibration Test** Vibration test is intended to detect the weak soldering, solder ball, intermittent connection etc. See Environmental Test requirement.

**C-4.38 Cable Test** This test is to verify the correctness of output cable. Connection of each individual functional pin(s) of output connector is required.

# APPENDIX D
# Stress Testing (HALT/HASS/HASA)

**D.1 Highly Accelerated Life Testing (HALT)** HALT is a requirement of IPC-9592 and is performed early in the development cycle. HALT consists of applying environmental and electrical stresses beyond specification limits. These stresses are increased until the PCD fails. The purpose of HALT is to identify weaknesses that may point to insufficient margin in the design. This method is also referred to as STRIFE, however HALT is the generally accepted term. HALT may be repeated throughout the design cycle and even after introduction to manufacturing as required by design changes. HALT is considered a destructive test. HALT samples should never be shipped to customers.

Limits are often referenced in HALT as follows: Upper/Lower Specification limits (USL/LSL, e.g., Temperature), Upper and Lower Operating Limits (UOL/LOL), and Upper and Lower Destruct Limits (UDL/UOL) - see Figure D-1. Specification Limits are those limits within which the product is guaranteed to function. Operating Limits are the point at which the product may fail to meet specification but recovers once returned to USL/LSL. The Destruct Limits represent that point where the PCD fails catastrophically and does not recover functionality. Companies should establish target stress levels which they feel must be exceeded to insure product margin.



- USL/LSL — Upper/Lower Specification Limits. Limits to which you guarantee operation of your product.
- UOL/LOL — Upper/Lower Operating Limits. Limits to which product ceases to function, however can be returned to USL/LSL and begin working again.
- UDL/LDL — Upper/Lower Destruct Limits. Limits at which product fails catastrophically.

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**Figure D-1 Graphical Display of Typical HALT**

HALT testing is performed in an environmental chamber that can simultaneously provide temperature and vibration to a device under test. It must be possible to apply incremental increases (and decreases) in temperature and vibration to levels in excess of those specified for normal product operation. During testing, it is essential to exercise product operation and ensure functionality. Test setups should be optimized to maximize functional test coverage. The test setup should also allow for remote operation of the test and product from outside of the environmental chamber.

***Considerations*** (Stress Application Ordering):

The ordering in which stresses are applied is governed by their likelihood of precipitating catastrophic failures. The following order is recommended:

- Decreasing temperature.
- Increasing temperature.
- Increasing vibration.

***Stress Step Increment Size*** Stresses are increased in an incremental or stepwise fashion. The size of each step is determined based upon the accuracy required for failure point definition and the time available for testing. It is usual to vary step sizes as appropriate, in particular, reducing step size as failure point is reached, which allows a fine definition without compromising test duration.

***Functionality Restrictions*** It is sometimes the case that specific designs incorporate circuitry that changes functionality dependant upon stress level. In particular, there is often protection circuitry such as current protection, overtemperature, etc., that will limit functionality at the stresses applied during HALT. In such cases it is necessary to test the product twice. First, the product is tested with the circuitry enabled to ensure correct operation up to and beyond its trigger point. Then, the product is tested with the circuitry disabled to quantify failure modes and headroom.

***Time to Failure*** One complex aspect of HALT testing is the time to failure. At stresses above normal operation it is often the case that the product will fail eventually if left in the overstressed environment. For HALT however, it is immediate failures that are of interest. A thermal stress level should be set and the product monitored until it achieves this stress level. Once achieved for thermal test, the functional test should be executed immediately and any failures noted. For the vibration stepped stress process, fatigue damage is accumulated rapidly and the duration of the dwell time for each vibration step and for each sample should be adhered to for equal comparisons of fatigue strength limits between samples. Once achieved, the functional test should be immediately and any failures noted.

***Testing Beyond the Failure Point*** The HALT test should not stop when a failure is encountered. If possible, the failure mode should be analyzed and fixed to allow the test to continue beyond the stress level at which the failure occurred. If a fix is not possible, then testing should allow for and accommodate the known failure mode during further testing. Only if a fix is not possible, and functionality of the product is degraded to the point where functionality is not testable, should testing cease early. In general, HALT stresses will be increased until the Target stress or a Physical limit is reached.

***Recording Failures*** For each failure identified during testing, the following information should be recorded:

- Environmental and Electrical test conditions and time to failure.
- Failure description.
- Root cause of failure mode.
- Type of failure (catastrophic or recoverable).

***Documented Report*** For each HALT experiment conducted, a report should be generated. Each report should contain the following:

- Description of product and its stage of development.
- Specific goals for testing including target stress goals if defined.
- Serial number(s) for product under test.
- Test equipment list including serial numbers and software revision levels.
- Functional test description and procedure.
- Document any special arrangements or product alterations made for testing.
- Table of failures encountered with attributes, listed in order of increasing stress.
- Test conclusions including performance against stated target or prior product.

**D.2 Highly Accelerated Stress Screening (HASS); HASS Audit (HASA)** Stress testing when applied to 100% of production is referred to as HASS. When stress testing is applied to samples of production, the process is referred to as HASS Audit or HASA. HASS is considered a non destructive test and samples may be shipped to customers.

***Purpose*** This document is to serve as a general guideline and a reference for the power supply (dc to dc and ac to dc) suppliers to perform HASS/HASA testing as required by power supply users. Since it is only a general guideline, suppliers are required to generate their own testing profile based on their actual product performance and physical characteristics.

***Pre-Work*** It is assumed that the supplier has performed HALT testing on the product during the development process and has determined the Operation Limits and Destruct Limits of the product based on HALT testing results. If the supplier did not perform HALT for the product, a HALT **shall** be run before designing the HASS/HASA testing profile. HALT should be performed on no less than two manufacturing samples, in this case.

***HASS/HASA Equipment*** HASS/HASA testing must be performed in industry standard HALT/HASS chambers. These chambers should have the capability of doing combined 6 degrees-of-freedom random vibration plus rapid thermal cycling with ambient transition rates greater than 30 °C/min.

***Fixture Design and Qualification*** HASS/HASA fixture should be designed and fabricated to support the product throughput testing and provide proper vibration transmissibility, thermal uniformity and a balanced thermal rate of change.

***Profile Design*** The HASS/HASA testing profile should be based on the HALT results, along with other product-related variables such as functional test duration, thermal long-term degradation effects, product-specific stresses and production throughput test requirements. Stresses in a typical HASS include combinations of input voltage, output load, power cycling, random vibration and rapid thermal cycling. A sample testing profile is as follows in Figure D-2 which shows the thermal cycling and vibrations combination.

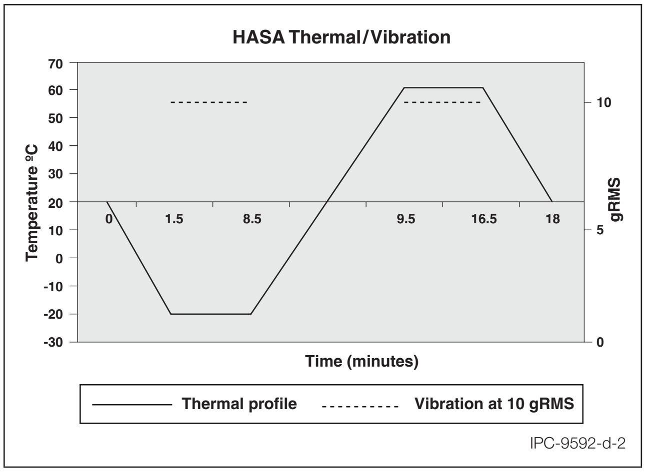

Figure D-2 Example Showing HASA Thermal Plus Vibration Test Profile

***Temperature Range for Thermal Cycling*** At a minimum, this range should be the minimum and maximum specified operating temperature (Note: a maximum limiting reference temperature, also called ‘‘hot spot temperature’’ may be used for maximum operating limit).

***Vibration Level*** The vibration should be modulated throughout during HASS/HASA, beginning at 3 to 5 Grms (depending on product) and slowly ramped to the maximum level. This process should be repeated in reverse, from the maximum level to 3 to 5 Grms. As a rule-of-thumb, the initial maximum vibration level of HASS/HASA should be at 50% of the vibration destruct limit (DL) but not exceed its operation limit (OL) found during HALT.

***Testing Duration*** The dwell time at each temperature extreme depends on the size and weight of the product to be tested and the time needed to run a functional test or diagnostic test profile. The minimum dwell time should be no less than 5 minutes. The dwell time began after the product reached its desired stable temperature. The minimum requirement for vibration is at least 5 minutes at the maximum vibration level plus slow ramped vibration modulation.

***Cycle Times*** As a rule-of-thumb, the thermal cycling plus vibration should be running for 5 cycles as an initial testing profile. The cycle times **shall** be adjusted based on the actual products and the test effectiveness.

***Other Stresses*** The product function test routine should be performed throughout the profile. This includes supplying a variable input voltage to the units and a variable load on the outputs. Power cycling should be performed at the thermal extremes.

***Proof-of-Screen*** A proof-of-screen testing must be run before determining the final HASS/HASA testing profile for use in manufacturing. Proof-of-screen is a two-step process: 1) to determine if the initial profile is effective to detect manufacturing flaws, and 2) to prove that the profile has not removed too much of a product's useful life or will not damage a good part.

Since units having passed through HASS/HASA will be customer shippable, the rule-of-thumb for the safety of HASS/HASA profile is that the test should not remove more than 10% of the total product's useful life. To do this, a test needs to run *at least* 10 times of the initial profile, for example, to run 50 cycles (10x5 cycles) of the above testing profile. No failure after this many cycles will indicate the initial testing profile is not too strong to remove too much useful life, or the profile is relatively safe. If it fails, the process is repeated at lower stress levels to modify the initial testing profile.

To show if the initial testing profile is effective in detecting manufacturing flaws, some ‘‘seeded’’ samples, such as samples with known defects or field returned NTF parts, should go through the testing profile to see if these known defects can be detected. This part of testing is voluntary and not mandatory.

If the proof-of-screen test show that samples can stand at least 10 times of the initial or modified HASS/HASA test profile, the profile will be accepted as formal HASS/HASA testing profile to be used in the manufacturing process.

***HASA Testing Sample Size*** During initial production, HASS **shall** be performed on 100% of the production units, assuming the supplier chooses HASS in lieu of BI, as discussed in Appendix E. After the production process has matured and most of the early failures and defects have been fixed, the power supply suppliers could consider to switch from 100% HASS to sampling HASA, with power supply users' approval. Refer to Appendix E.2.2.3 for details of HASA sample requirements.

***Other Requirements for HASS/HASA***

1) The PCD of HASS/HASA must be turned on during testing and functional test should be run at each temperature extreme.
2) The PCD **shall** be continuously monitored during HASS/HASA.
3) Monitoring with very good coverage is essential to success for HASS/HASA. During HALT/HASS/HASA, more than one-half of the failures are intermittent failures and most failures are temperature and vibration dependent. If the product is not monitored during the test, these failures will skip the test without detection.
4) HASS/HASA is different than traditional quality tests, such as AQL or LTPD testing. All failures during HASS/HASA must be analyzed to root causes. Corrective action is required.

# APPENDIX E
# Manufacturing Reliability Testing - BI/HASS/ORT

**E.1 Introduction** Manufacturing tests are typically conducted at room ambient (~25 °C) and are often only a few seconds in duration. These tests are useful for identifying obvious manufacturing and component defects that are easily detected and corrected. Additional testing may be required to identify product weaknesses that pass initial 25 °C testing but fail under more stressful conditions such as at temperature extremes or during the first few hours of operation.

Failures that occur early in the life of a product are referred to as infant mortality. If undetected in factory testing, these failures may occur in the first year and often within the first month of operation in the field. While it is not practical to test for periods equivalent to one year in a manufacturing test, it is possible to test under accelerated stress conditions that allow detection of failures with just a few hours of exposure to those stresses.

**E.1.1 Overview of Test Options** Manufacturing tests **shall** be put in place that apply stresses beyond 25 °C and for durations greater than those seen during standard functional test. Historically companies have used Burn-In (BI) to serve this purpose. BI is typically done at elevated temperatures (40 °C to 50 °C) while product is powered, loaded and periodically monitored for functionality. BI test duration may range from one hour to several days.

An alternate method to accelerate failures is Highly Accelerated Stress Screening (HASS) and HASS Audit (HASA). This approach is more effective at identifying product weaknesses because it uses additional stressful environments such as thermal cycling and vibration, as well as input voltage (line) and load variation. While HASS is more effective at identifying infant mortality failures, it is also more difficult and expensive to implement in manufacturing due to added complexities of environmental chambers, test equipment and fixturing. However, due to the value HASS offers, it is strongly recommended that manufacturers have some HASS capability. Other tests of longer duration may be required on a sample basis. These tests are referred to as Ongoing Reliability Testing (ORT).

**E.1.2 Reliability Test Implementation - Best Practices** Manufacturing reliability tests *should not* be viewed as effective screens for poor reliability. It is rare to be able to screen out all infant mortality failures. Failures in Burn-in, HASS and ORT should be viewed as early warnings of possible similar undetected failure mechanisms in a population of products. Failures representative of a given failure mechanism are often distributed in stress and/or time and may be undetectable with the stress-time limitations seen in production reliability tests. The most effective way to eliminate these failures is to rapidly diagnose the root cause of any failure identified during reliability testing and correct it.

For this reason, it is strongly recommended that Power Supply manufacturers have the ability to perform rapid detailed failure analysis including same day access to laboratory facilities that support materials failure analysis (cross section, decap, SEM/EDX, etc.). These resources should prioritize any reliability test failures ahead of standard production yield improvement activities. In addition, it is recommended that manufacturers create an internal Failure Review Board (FRB) to review all failures for accurate root cause analysis and effectiveness of corrective action.

As products mature, failures identified during manufacturing reliability tests should be rare. At some point it is no longer cost effective to continue performing reliability tests on 100% of manufactured products. The processes described in the following sections require products to start out with a 100% BI **or** HASS but allow for reduction in test time and a migration to sampling when failure rates are demonstrated to be low or zero, except in cases where parametric stability is required through BI/HASS on 100% of Product.

It should be noted that HASS is effective at identifying more failure modes than traditional BI, however, in some cases it also may *overstate* the absolute risk of field failure. In other words, for some failure mechanisms HASS may identify failures with a low risk of appearing in the field. For example, HASS may identify a failure that only occurs with a power cycle between -20 °C and 40 °C and does not degrade with time. While this condition may be within specification, its probability of occurrence in normal field operation is low. *Most* failure mechanisms seen in HASS will eventually show up in the field, just possibly at a lower rate.

When field failures indicate a reliability issue that has escaped detection in the factory, a frequent reaction is to increase burn-in time or HASS stresses. Just like the goal of all manufacturing tests should be to use test results to identify and correct defects, the same is true for field failures. The objective should be to identify the root cause of the failure and correct it, not to add a screen which may only be partially effective at best.

**E.2 Manufacturing Reliability Test Requirements** All PCDs **shall** follow one of two reliability test options on *initial* manufactured products:

**Option 1:** 100% BI

**OR**

**Option 2:** 100% HASS

For both options, 100% of products produced **shall** be exposed to the reliability test for the duration specified. Test times may be reduced and sampling implemented when failure rates demonstrate that the manufacturing process is in control. As noted in Figure 7-1, all products which go into a reliability test **shall** first pass a room ambient functional test.

Auxiliary power products such as cabinets, backplanes, distribution panels, etc. may be excluded from these requirements unless other arrangements are made AABUS.

When a power supply undergoes a major design change or a change in manufacturing location, the product **shall** begin the BI or HASS process over as specified below for Initial Production. This is in addition to the re-qualification required for such changes as specified in Section 5.

For products that are part of a Product Family as defined in Section 2, quantities from all product family members may be combined to meet the requirements specified in Appendix E.

The following sections have provisions for reducing BI/HASS test time and in cases of mature, high yield processes, sampling is allowed. Before reducing test time or transitioning to sampling, manufacturing must demonstrate a minimum acceptable yield. These yields vary by product complexity, power level and process being evaluated. It is not possible to capture all levels of complexity in this document however, as a general benchmark, the following categories of products are identified:

- ***Low Power dc to dc Products and SMT POLs:*** Defined as dc to dc converters ≤50W for Vout ≥2V or ≤40A for Vout ≤2V or any SMT POL.
- ***ac to dc Adapters and Medium to High Power dc to dc Converters:*** Small ac to dc Adapters (external adapters such as those used in printer and PC applications) and dc to dc converters >50W.
- ***Low Power ac to dc Category 1 PCDs:*** Includes ac to dc and dc input Field Replaceable Units (FRUs) and Category 1 PCDs ≤1kW.
- ***High Power ac to dc Category 1 PCDs:*** Includes ac to dc and dc input FRUs and Category 1 PCDs >1kW.

Table E-1 contains a lookup table that will be referenced in the following sections. Refer to the row appropriate to the section referenced and the column associated with the product in question.

### E.2.1 Burn-In (BI) Requirements (Option 1)

**E.2.1.1 BI Requirements for Initial Production** For manufacturers who choose BI (**Option 1**), the following conditions **shall** be required on initial production:

- BI **shall** be performed on 100% of initial production (see **Note 1** below). Minimum starting BI duration **shall** be 24 hours. Allowance for BI time reductions are discussed in E.2.1.2. Provisions for BI sample testing are discussed in E.2.1.3.
- Input Voltage for ac products: 110 Volts and 220 Volts (Lots split so that half are tested at 110V, half at 220V). Input voltage for dc products **shall** be nominal input voltage.
- Ambient Temperature Burn-In chamber: 40 °C to 50 °C ± 5 °C (Note, even lower BI temperatures may be required to prevent unnecessary Overtemperature Protection (OTP) trips or when hot spot temperatures exceed maximum rated.)
- Output Load (per output): 90% ± 10% of maximum rating for all outputs **or** worst case load based on stress analysis as determined by the manufacturer **or** that load required such that the hot spot temperature does not exceed maximum specified in the data sheet (Load can be Resistive or Electronic type).
- Power Cycle a minimum of two times per hour. While not a requirement, a preferred approach is to follow the profile outlined in Figure E-1.

**Table E-1 Acceptable Failure Rates for Test Time Reduction/Sampling/Elimination**

| Row | Affected Test | Section | dc to dc ≤50W & SMT POLs | ac to dc Adapters & dc to dc >50W | Category 1 PCD ≤1kW | Category 1 PCD >1kW |
|---|---|---|---|---|---|---|
| A | BI Test Time Reduction | E.2.1.2 | 250 ppm or * | 500 ppm | 750 ppm | 1500 ppm |
| B | BI Audit | E.2.1.3 | 100 ppm or * | 200 ppm | 400 ppm | 800 ppm |
| C | BIA Elimination | E.2.1.4 | 0 ppm or * | 100 ppm | 200 ppm | 400 ppm |
| D | HASS Cycle Count Reduction | E.2.2.2 | 500 ppm or * | 1000 ppm | 1500 ppm | 3000 ppm |
| E | HASS Audit | E.2.2.3 | 250 ppm or * | 400 ppm | 750 ppm | 1500 ppm |
| F | HASA Elimination | E.2.2.4 | 100 ppm or * | 200 ppm | 400 ppm | 800 ppm |

* Apply Note 1, E.2.1.1

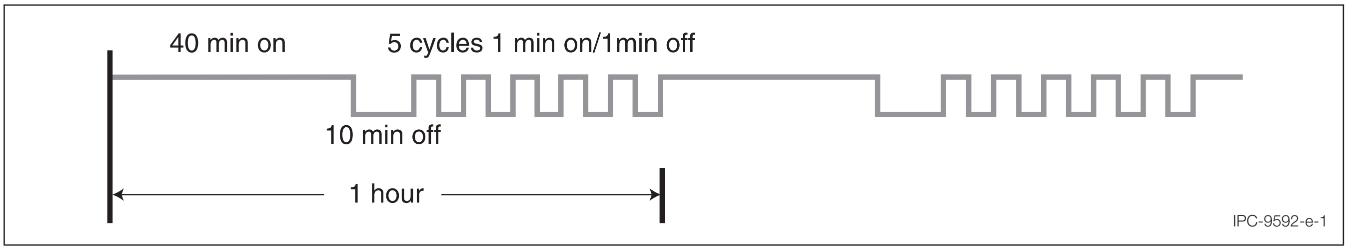

**Figure E-1 Input Power Cycling Diagram**

- Monitoring and Failure Reporting: Real time automated monitoring of output voltage regulation **shall** be required (scan outputs at least every five minutes and a minimum of once per power cycle). Time to failure data as well as the condition at time of failure **shall** be maintained for each BI failure.

**Note 1:** Low power Point of Load (POL) converters, especially surface mounted modules, typically have low infant mortality failure rates and are very difficult to Burn-In. It is especially difficult to design BI fixturing with sufficiently rugged sockets to prevent risk of thermal damage to modules under test after repeated socket use. In some cases there may be a greater risk of inducing as opposed to detecting failures. In cases of all surface mounted POLs and through hole modules with maximum power ≤50 Watts for Vout ≥2V or ≤40A for Vout <2V, BI may be replaced by unpowered thermal cycling. This consists of two unpowered thermal cycles from the minimum to maximum specified storage temperature of the module (see Figure E-2) followed by functional test. Provision for eliminating this test will be discussed in E.2.2.5. When this approach is taken, it **shall** be required that samples from each product family that elects this option will go through a separate Ongoing Reliability Audit consistent with E.2.2.3. This is to occur in parallel with the unpowered thermal cycle process.

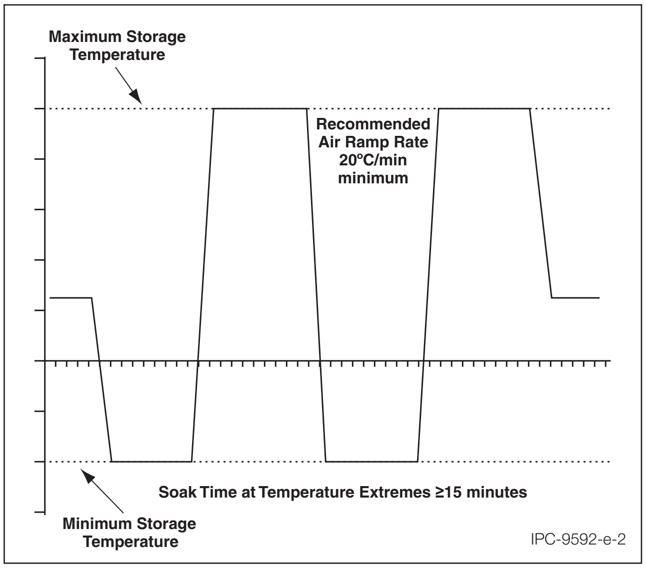

**Figure E-2 Unpowered Thermal Cycle Profile**

**E.2.1.2 BI Test Time Reduction** As products are tested in BI for 24 hours, total test hours are accumulated and should demonstrate with increasing confidence that initial production has acceptable low levels of infant mortality risk. Increments of unit-hours of BI will be used to periodically review BI results and determine suitability to step to shorter BI test duration. Total unit-hours are calculated by multiplying the quantity of units tested by the number of hours of each unit on test. For example:

**100 units x 24 hours/unit = 2400 unit-hours**

The following provision for BI test time reduction **shall** use increments of *6000* units-hours for evaluation. Test time reduction will be made as shown in Table E-2.

**Table E-2 BI Time Reduction Requirements**

| Reduction Interval | BI Duration | Minimum Qty of Units |
|---|---|---|
| Initial time | 24 hours | 250 |
| Reduction 1 | 6 hours | 500 |
| Reduction 2 | 6 hours | 1000 |
| Reduction 3 | 3 hours | 2000 |
| Reduction 4 | 2 hours | 3000 |

The following requirements **shall** be met before qualifying for BI test time reduction:

- A minimum of 6000 unit-hours at the current interval, **and**
- A minimum of three production lots at the current interval, **and**
- Defect free at current interval **or** acceptable failure rate during current interval (see Table E-1, Row A) **and** Root Cause Failure Analysis (FA)/Corrective Action (CA) for all failures at current interval.

Failure to identify and correct any BI failure root cause will prevent progression to the next reduction interval. Even when all failures have been corrected, failure rates in excess of that specified in Table E-1 prevent progression. When this occurs, the first failure must be cleared by running the required minimum quantity of units at the current interval and still meet the requirement. See examples that follow.

***Example 1:*** A 3kW ac to dc rectifier had 1000 units go through 6 hours of BI with one failure (1 defect/1000 units = 1000 ppm). The root cause of that defect has been corrected. The product may proceed to 3 hours of BI (1kW, 1500 ppm allowed).

***Example 2:*** A 500W dc to dc converter has had 2000 units go through 3 hours of BI. There have been two failures identified (different failure modes; two failures/2000 units tested = 1000 ppm). The failures occurred in the 500th sample and the 800th sample. The last 1200 units tested were defect free. Both defects have had corrective action taken, however due to the failure rate exceeding 750 ppm, the product cannot proceed to the next reduction interval until the first failure has cleared. This will require an additional 667 units be run, defect free, to clear the first failure.

**E.2.1.3 Sample BI** Once 6000 unit-hours are completed for 2 hours of BI, manufacturing will have accumulated a minimum of 30,000 unit-hours for all BI performed to date. At this time manufacturing may transition to BI Audit or BIA **only if** Table E-1, Row B is satisfied for the current two hour interval **and** additional reliability audit procedures are in place (see E.2.3). Requirements for BIA:

- Sample size = 10% of production.
- Duration = two hours.
- Failures that occur in a sample population require immediate Root Cause FA/CA and risk assessment to determine if the population that did not go through BI audit is at risk **or** revert back to 100% BI. Note, single failures generally will not require reverting to 100% BI unless the manufacturer deems the risk of continuing to perform BIA to be unacceptable. Two or more failures resulting in a defect rate in excess of Table E-1 Row B require production stop or revert to 100% BI until corrective action is taken.

### E.2.1.4 Elimination of BIA Requirement

- Following a period of one year **or** 30,000 unit-hours accumulated during BIA, manufacturing may request to eliminate BIA. Elimination requires Table E-1, Row C be satisfied.

### E.2.2 Highly Accelerated Stress Screen (HASS) Requirements (Option 2)

**E.2.2.1 HASS Requirements for Initial Production** For manufacturers who choose HASS (**Option 2**), the following conditions **shall** be required on initial production:

- HASS **shall** be performed on 100% of initial production (see **Note 1** below). Minimum starting HASS duration **shall** consist of five thermal cycles, at least one cycle with vibration (see **Note 2** below). Allowance for HASS cycle reductions are discussed in E.2.2.2. Provisions for HASS sample testing are discussed in E.2.2.3.
- Input Voltage for ac to dc and dc to dc products: Minimum and Maximum specified input voltage.
- Temperature Range of thermal cycle: At least minimum and maximum specified operating temperature ± 5 °C (see Appendix D for additional information).
- Output Load (per output): Multiple load conditions (including minimum and maximum) such that hot spot temperature does not exceed maximum specified in data sheet (Loads **shall** be Electronic type to facilitate applying multiple loads).
- Power Cycle a minimum of one time per temperature and input line condition.
- Monitoring and Failure Reporting: Real time automated monitoring of output voltage regulation **shall** be required (scan outputs at least every one minute and a minimum of once per power cycle). Time to failure data as well as the condition at time of failure **shall** be maintained for each HASS failure.
- **Note 1:** In cases of all surface mounted POLs and through hole modules with maximum power ≤50 Watts for Vout ≥2V or ≤40A for Vout <2V, HASS may be replaced by unpowered thermal cycling. This consists of two unpowered thermal cycles from the minimum to maximum specified storage temperature of the module followed by functional test. Provision for sampling under these conditions will be discussed in E.2.2.5.
- **Note 2:** Vibration will not be required for dc to dc products with a maximum component height of 0.300 inch and demonstrated destruct limit of at least 20g rms during HALT vibration testing.

**E.2.2.2 HASS Cycle Reduction** As products are tested in HASS for five thermal cycles, total thermal cycles are accumulated and should demonstrate with increasing confidence that initial production has acceptable low levels of infant mortality risk. Increments of unit-cycles of HASS will be used to periodically review HASS results and determine suitability to step to shorter HASS test duration. Total unit-cycles are calculated by multiplying the quantity of units tested by the number of thermal cycles of each unit on test. For example:

**100 units x 5 thermal cycles/unit = 500 unit-cycles**

The following provision for HASS test time reduction **shall** use increments of *2000* unit-cycles for evaluation. Cycle count reduction will be made as shown in Table E-3.

**Table E-3 HASS Thermal Cycle Count Reduction Requirements**

| Reduction Interval | HASS Cycle Count | Minimum Qty of Units |
|---|---|---|
| Initial 5 cycles | 5 | 400 |
| Reduction 1 | 2 | 1000 |
| Reduction 2 | 1 | 2000 |

The following requirements **shall** be met before qualifying for HASS cycle count reduction:

- A minimum of 2000 unit-cycles at the current interval, **and**
- A minimum of three production lots at the current interval, **and**

- Defect free at current interval **or** acceptable failure rate during current interval (see Table E-1, Row D) **and** Root Cause Failure Analysis (FA)/Corrective Action (CA) for all failures at current interval.

**E.2.2.3 HASS Audit (HASA)** Once 2000 unit-cycles are completed for single cycle HASS, manufacturing will have accumulated a minimum of 6000 unit-cycles for all HASS performed to date. At this time manufacturing may submit a request to transition to HASS Audit or HASA **only if** Table E-1, Row E is satisfied for the current single cycle interval. Requirements for HASA:

- Initial sample size = 5% of production up to a maximum of 100 units/wk.
- Duration = 1 Thermal Cycle with vibration (no vibration for low profile dc to dc).
- Failures that occur in a sample population require immediate Root Cause FA/CA and risk assessment to determine if the population that did not go through HASS audit is at risk **or** revert back to 100% HASS. Note, single failures generally will not require reverting to 100% HASS unless the manufacturer deems the risk of continuing to perform HASA to be unacceptable. Two or more failures resulting in a defect rate in excess of Table E-1 Row E require a production stop or revert to 100% HASS until corrective action is taken.

**E.2.2.4 Elimination of HASA Requirement**

- Following a period of six months or 2000 unit-cycles accumulated during HASA, manufacturing may request to eliminate HASA **only if** additional reliability audit procedures are in place (see E.2.3). Elimination also requires row F of Table E-1 be met during the HASA period of evaluation.

**E.2.2.5 Elimination of Unpowered Thermal Cycle Requirement** Unpowered thermal cycle for low power and SMT POLs may be discontinued after 4000 units pass through the process if no more than one defect is detected and corrective action has been implemented for that defect. When more than 1 defect has occurred, the 4000 unit count will be reset such that only the most recent failure is included in the count.

**Example:** In 4000 consecutive units tested,
Sample 1000 fails
Sample 2500 fails

After sample 4000, there have been two failures therefore 100% thermal cycle will continue to be required and the sample count is reset at sample 1001. After sample 5000 there have been no additional failures. During the last 4000 consecutive units tested, there has been a single defect (sample 2500). Assuming corrective action has been implemented for that failure, unpowered thermal cycle can be eliminated if ORT is in place.

**E.2.3 Ongoing Reliability Test (ORT) Requirements - (All ORT Requirements are AABUS)** ORT will be a requirement for transition to audit (BI only) or to eliminate a BI/HASS audit. One exception to this will be for low volume products (<6000 units/year) where there will be **no** ORT requirement.

All ORT failures require immediate Root Cause FA/CA and risk assessment to determine if the population that did not go through ORT is at risk.

**E.2.3.1 ORT Requirements Necessary to Implement Burn-In Audit** Prior to submitting for approval to go to BIA, manufacturing must implement an Ongoing Reliability Test audit. This may be performed using existing Burn-In facilities. ORT **shall** consist of one of the following:

- ***Option 1:*** Long Term using BI Test Equipment.
  - Sampling of a minimum of 4 units every four weeks (see **Note 1**).
  - Units **shall** remain on test for 672 hours (28 days).
  - Test conditions **shall** match those of standard BI.
- ***Option 2:*** Short Term using BI Test Equipment.
  - Sampling of a minimum of 4 units every two weeks (see **Note 1**).
  - Units **shall** remain on test for 336 hours (14 days).
  - Test conditions **shall** match those of standard BI.

Options 1 and 2 may be interchanged based on internal supplier test feedback as well as customer feedback.

**Note 1:** Four units per test period applies to ≤1kW products. For product power >1kW, use two units per test period.

**E.2.3.2 ORT Requirements for Eliminating HASA** Prior to submitting for approval to eliminate HASA, manufacturing must implement an Ongoing Reliability Test audit. This may be performed using existing HASS facilities. ORT **shall** consist of the following

- Using HASS Test Equipment.
  - Sampling of a minimum of eight units every four weeks.
  - Units **shall** see a minimum of 10 thermal cycles each over full operating temperature range, line and load variation over full operating range and vibration consistent with Appendix D (low profile dc to dc converters do not require vibration).

**E.2.3.3 ORT Requirements for Unpowered Thermal Cycle** When manufacturing chooses to perform unpowered thermal cycling on eligible POLs due to difficulty implementing Burn-In or HASA, an Ongoing Reliability Test audit must be put in place in lieu of BI/HASS. This may be performed using existing Burn-In or HASS facilities. Samples **shall** be soldered to a test board to insure low resistance contact to high current pins. ORT **shall** consist of one of the following

- **Option 1:** Long Term using BI Test Equipment.
  - Sampling of a minimum of 10 units per four week period.
  - Units **shall** remain on test for 672 hours (28 days).
  - Test conditions **shall** match those of similar products from standard BI.
- **Option 2:** Using HASS Test Equipment.
  - Sampling of a minimum of 10 units each week.
  - Units **shall** see a minimum of 10 thermal cycles each over full operating temperature range, line and load variation over full operating range.

**E.2.3.4 Disposition of ORT samples** ORT samples which have been soldered to a test board **shall** be scrapped. Other samples from ORT may be shipped only if they can be demonstrated to have not consumed more than 5% of useful life. An example of how this determination is made, follows:

- Calculate the 25 °C useful life of known elevated temperature wearout mechanisms such as Fans, Aluminum Electrolytic Capacitors, etc. Estimate the equivalent time consumed during ORT. Take the ratio of ORT life to useful life. If >0.05, products must be scrapped.

  **Example 1:** Calculated useful life of C1 (330μF aluminum electrolytic capacitor) = 10 years (87,600 hours) at 25 °C.

  Equivalent hours of life at ORT test condition of 45 °C ambient (assume 4x acceleration factor in this example) for 672 hours:

  672 hours x 4 = 2,688 equivalent hours

  2,688/87,600 = 0.03
  (OK to ship, does not exceed 0.05 maximum)

- Calculate the useful life of known cyclic fatigue wearout mechanisms such as Solder Joints, PWB vias, etc. Estimate the equivalent time consumed during ORT. Take the ratio of ORT life to useful life. If 0.05, products must be scrapped.

  **Example 2:** Useful life of a surface mount FET = 3,500 thermal cycles (0 °C to 100 °C).

  Equivalent life at ORT test condition of 2 power cycles/hour, 672 hours, equivalent ΔT of Power FET = 30 °C.

  672 hours x 2 power cycles/hour =
  1,344 thermal cycles of ΔT = 30 °C

  Apply appropriate cyclic fatigue model: (assume acceleration factor of 21x is used here for 30 °C vs 100 °C ΔT)

  Equivalent lifetime at ΔT = 30 °C:
  21 x 3,500 cycles = 73,500 cycles

  1,344/73,500 = 0.018 (OK to ship)

**E.2.4 BI/HASS Requirements for Design or Factory Changes** PCD Suppliers **shall** notify customers of Design changes per 6.5.1.3. Requirements for performing additional BI/HASS testing **shall** be AABUS.

In addition, PCD Suppliers **shall** notify customers of a change in manufacturing location. BI/HASS testing requirements **shall** be reset to those of initial manufactured products as described in E.2.

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If space not adequate, use reverse side or attach additional sheet(s).

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___ Test Method number ___, paragraph number ___

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

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