High Power Factor LED Controller with HV Start-up and MOS Integrated

Datasheet: 00

General Description

The LD7832 is a buck solution with high PFC control for LED lighting. It is equipped with power MOS and HV start up for easy design, effectively cost down and compact PCB size. This IC is operating on transition(TM) mode and integrated with completed safety requirement protections.

With HV start-up technology, high power factor and TM control, the system can easily achieve high PF and high efficiency to meet most of international standard requirements.

With completed protection functions built inside this IC. Such as LED open protection (OVP), LED short protection (ZCD UVP), over current protection (OCP), CS short protection (CSSP), open feedback protection and over temperature protection (OTP). It makes circuit easily meet most safety requirements in both normal or abnormal test.

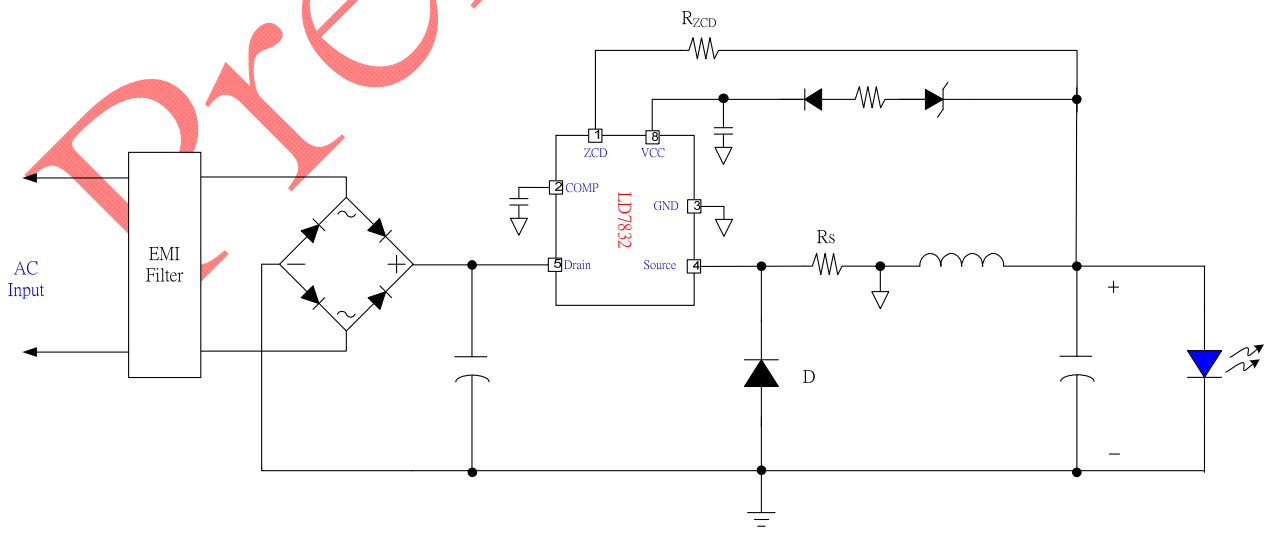
Features

- Built-in 500V power MOSFET
- Built-in HV startup
- High power factor controller integrated
- High efficiency transition mode operation
- Low cost and components count
- Accuracy current regulation
- Wide UVLO (16Von and 8 Voff)
- VCC OVP (VCC Over Voltage Protection)
- ZCD UVP (ZCD under voltage protection)
- OCP (Cycle by cycle current limiting)
- CSSP (CS short protection)
- Open feedback protection
- OTP (Overt temperature protection)
- OTP to reduce power (Option)
- 250/-500mA Driving Capability

Applications

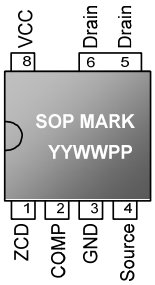
- LED Driver Application for low cost and minimum PCB size.

Typical Application for LED (Buck PFC)



LD7832 Pin Configuration

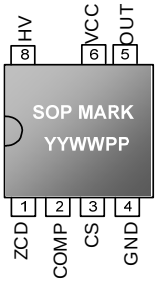
DIP-6/ SOP-6 (TOP VIEW)



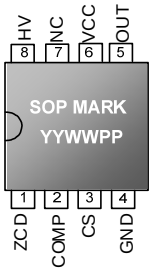
Combo IC

YY: Year code
WW: Week code
PP: Production code

SOP-7



SOP-8 (TOP VIEW)



PWM IC

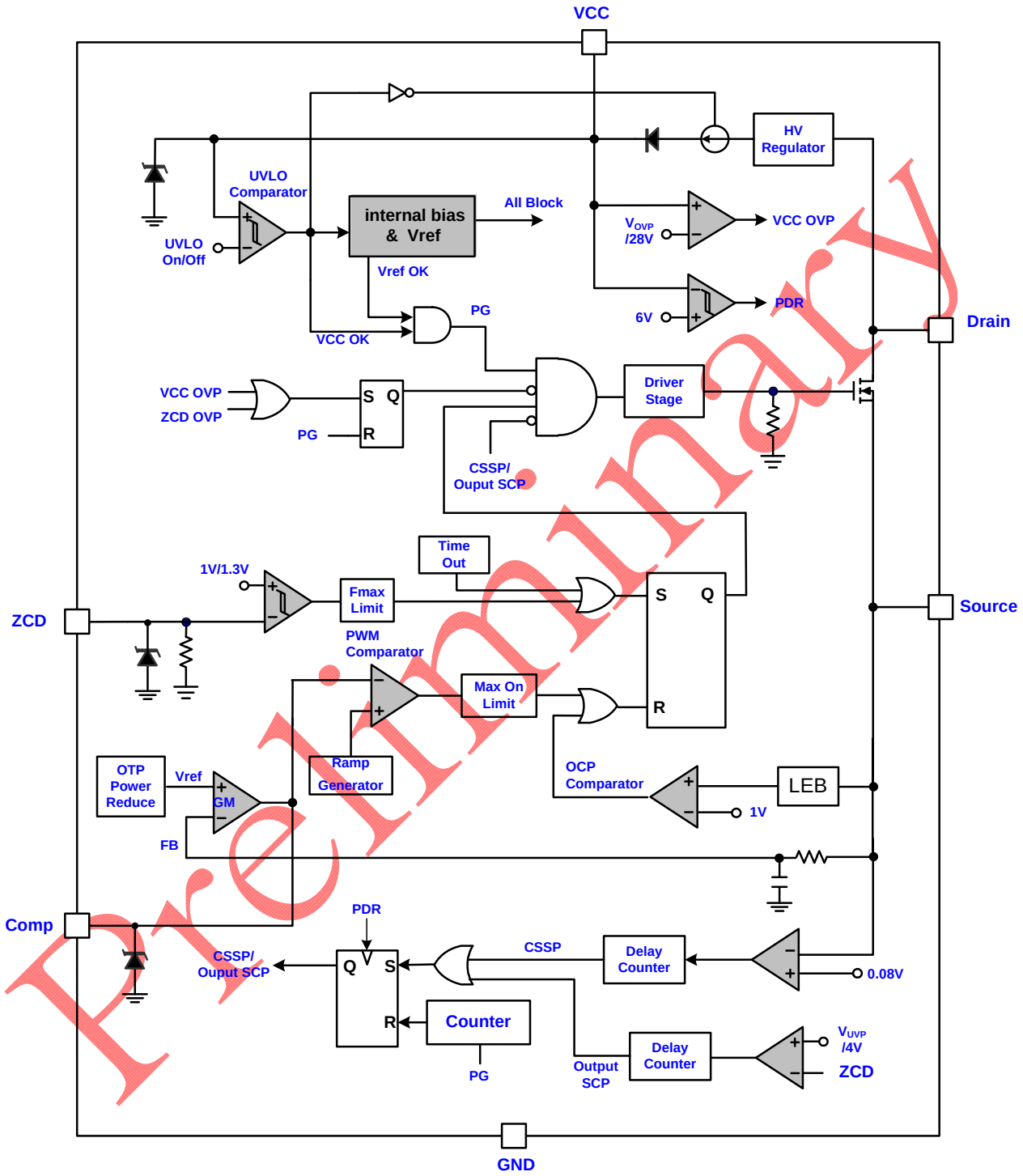
Ordering Information

Part number	Package		Top Mark	Shipping
LD7832 xx	SOP-7	Green package	LD7832 xx	
LD7832 xx	SOP-8	Green package	LD7832 xx	
LD79xx xx	DIP-6	Green package	LD79xx xx	
LD79xx xx	SOP-6	Green package	LD79xx xx	

Pin Descriptions

Pin (Combo)	Pin (PWM)	NAME	FUNCTION
1	1	ZCD	Quasi resonance detector
2	2	COMP	Compensation pin for internal error amplifier
3	4	GND	Ground
4	3	Source/CS	Source terminal of internal power MOSFET, connecting a sense resistor to ground
5, 6	8	Drain/HV	Drain terminal of the internal power MOSFET/ Connected this pin to AC terminal to provide the startup current for IC.
7		NC	
8	6	VCC	Power Supply to VCC
	5	OUT	Gate Signal Output

Block Diagram



Absolute Maximum Ratings

VCC	-0.3 ~ 30V
Source/ CS, ZCD	-6 ~ 10V
ZCD	+/-2.5mA
Drain/ HV	-0.3 ~ 500V
COMP	-0.3 ~ 6V
OUT	-0.3 ~ 30V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 125°C
Operating Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-6, θ_{JA})	160°C/W
Package Thermal Resistance (DIP-6, θ_{JA})	100°C/W
Power Dissipation (SOP-6)	400mW
Power Dissipation (DIP-6)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model(except HV pin)	3KV
ESD Voltage Protection, Machine Model	300 V
ESD Voltage Protection, Human Body Model(HV pin only)	1KV
ESD Voltage Protection, Machine Model(HV pin only)	200 V
Gate Output Current	250mA/-500mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc pin capacitor	4.7	22	μF
Comp pin capacitor	0.47	4.7	μF

Electrical Characteristics

(V_{CC}=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)					
High-voltage current Source	VCC<6V , HV=500V		1		mA
	6V<Vcc<UVLO(on)		3		mA
Off-state Leakage current	VCC>UVLO(ON), HV=500V			35	uA
Supply Voltage (VCC Pin)					
Startup Current	VCC<UVLO ON @VCC=10V		260		μA
Operating Current	V_{COMP}=3V, ZCD=2V		1		mA
(with 1nF load on OUT pin)	V_{CC} OVP tripped		0.5		mA
UVLO (off)			8		V
UVLO (on)			16		V
HV Self Bias (Linear Regulator)			13		V
VCC OVP Level			28		V
De-Latch Vcc Voltage	PDR		6		V
Compensation(Comp Pin)					
GM(1)			200u		umho
Open loop voltage	Comp pin open		5.3		V
Current Sensing (Source Pin, CS pin)					
Reference voltage(Vref)			0.2		V
OCP Threshold(Cycle by Cycle)			1		V
Trip level for CS Short protection			0.08		V
Startup Blanking Time for CSSP			32		ms
Delay Counter(CS voltage < 0.08V)			4		ms
CSSP De-Latch Counter			8		times
LEB time			250		ns
Zero Current Detector (ZCD Pin)					
Upper Clamp Voltage	ZCDin=10V		4.9		V
Lower Clamp Voltage	ZCDin=0V		0.3		V
Input Voltage Threshold			1		V
	Hysteresis		0.3		V
ZCD UVP for LED short protection			4		V
Delay Counter of ZCD UVP			4		ms
ZCD UVP De-Latch Counter			8		times
Minimum (ON+OFF)-Time, Fmax(ZCD Pin)					
Minimum ON+OFF-Time	Fs,max(125kHz) , Good TC		8		μs
Minimum OFF-Time			1		us

Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, I_{SINK}=20mA	0		0.5	V
Output High Level	V_{CC}=15V, I_{SOURCE}=20mA	10		VCC	V
Output High Clamp Level	V_{CC}=16V		13		V
Rising Time	V_{CC} =15V, CL=1nF		60		ns
Falling Time	V_{CC} =15V, CL=1nF		20		ns
Starter					
Start Timer Period	Good TC		50		μs
OTP (Over Temp. Protection)					
OTP2 Trip level(1)			145		°C
OTP1 Trip level(Power reduce) (1)	Option		135		
OTP Hysteresis(1)			30		°C
Power Reduce(CS reference voltage) (1)	Temp=135°C trigger, Latch		0.1		V

Note: (1) Guarantee by Design.

Application Information

Operation Overview

LD7832 is a controller with MOSFET Integrated for LED lighting application and operates on transition mode(TM) to meet the requirement of high power factor and high efficiency. It can be minimum external components counts and PCB size for LED lighting application.

LD7832 is a voltage-mode TM PFC controller. The turn-on time of switch is fixed and the turn-off time is varied during steady state. Therefore, the switch frequency varies in accordance with input voltage variation. The varied frequency can provide lower EMI for AC/DC on for electrical regulation. Beside all, LD7832 features LED open protection, LED short protection, over current protection, CS short protection, open feedback protection and over temperature protection. Also, the LD7832 requires no mains voltage sensing unlike what the other traditional current mode PFC controllers behave for power saving.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes too significant power to meet the current power saving requirement. In most cases, startup resistors carry large resistance. And a larger resistance will spend more time to startup.

To achieve the optimized topology, as shown in figure 1, LD7832 is implemented with a high-voltage startup circuit on Drain pin, combines with an integrated MOSFET, for such requirement. During the startup, a high-voltage current source sinks current from the output of full-bridge rectifier to provide the startup current and charge the VCC capacitor. On the condition of VCC below PDR, the charge current will remains at 1mA to protect the circuit from being damaged, even in case VCC pin is shorted to ground. In contrast, the charge current will increases to 3mA once VCC rises above PDR voltage threshold during start up. Meanwhile, the VCC supply current is as low as 260μA that most of the HV current is adopted to charge the VCC capacitor. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

As the VCC voltage rises higher than UVLO(on) to power on the LD7832 and further to deliver the gate drive signal, the high-voltage current source will be disabled and the supply current is provided from the inductor. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect the voltage on the VCC pin to ensure the supply voltage enough to power on the LD7832 controller and in addition to drive the power MOSFET. As shown in Fig. 2, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

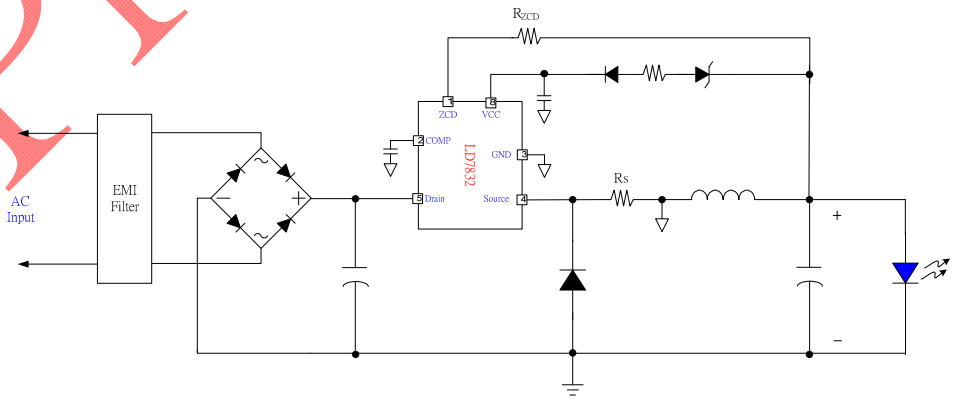


Fig. 1

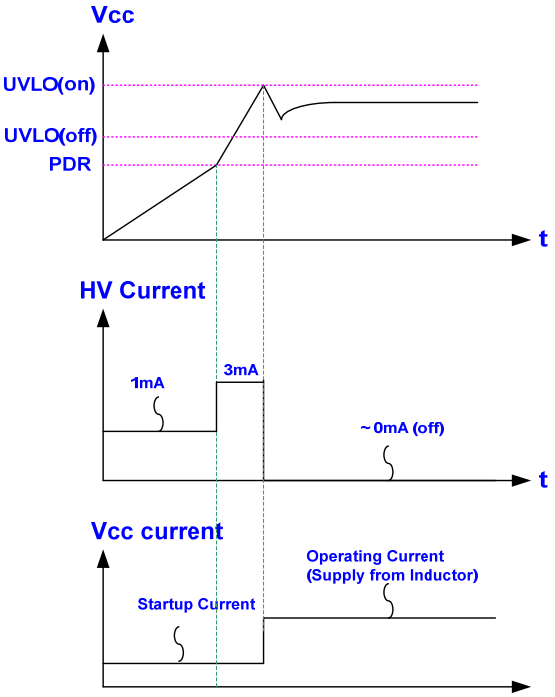


Fig. 2

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 3 shows typical ramp generator block and ZCD block. The comp pin voltage and the output of the ramp generator block are compared to determine the MOSFET On-time, as shown in Fig. 4.

The Zero Current Detection block will detect inductor signal to drive MOSFET turn on as ZCD pin voltage drops to 1V. As ZCD pin voltage drops to 1V, it means the current through the inductor is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains at above 1.3V. Once it drops below 1V, the zero current detector will act to turn on the MOSFET.

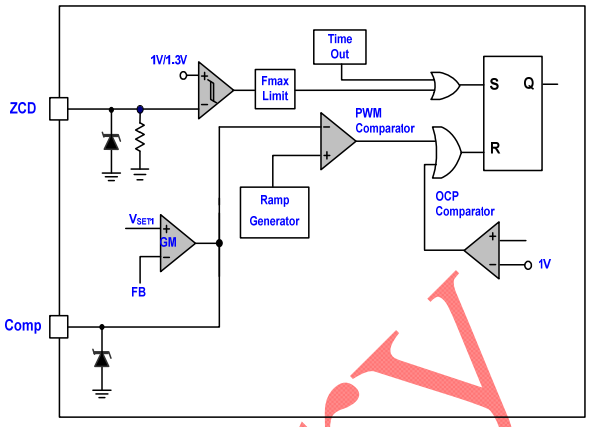


Fig. 3

The 50μs timer generates a MOSFET turn-on signal if the driver output drops to low level for more than 50μs from the falling edge of the driver output. Fig. 4 shows typical ZCD-related waveforms. Ideally, the switch must be turned on when the inductor current approaches zero; but it delays a while for ZCD delay in real situation. During delay time, the junction capacitor of the MOSFET resonates with the inductor and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

In order to simplify the design, a resistor (R_{ZCD}) connecting ZCD pin in series with the inductor as shown in Fig. 1 is used to assistant to detect the inductor signal and prevent ZCD pin damage at the same time. Fig. 4 shows the related waveform between inductor voltage and ZCD voltage. ZCD pin is clamped to 4.9V and 0.3V respectively in accordance with inductor voltage varies.

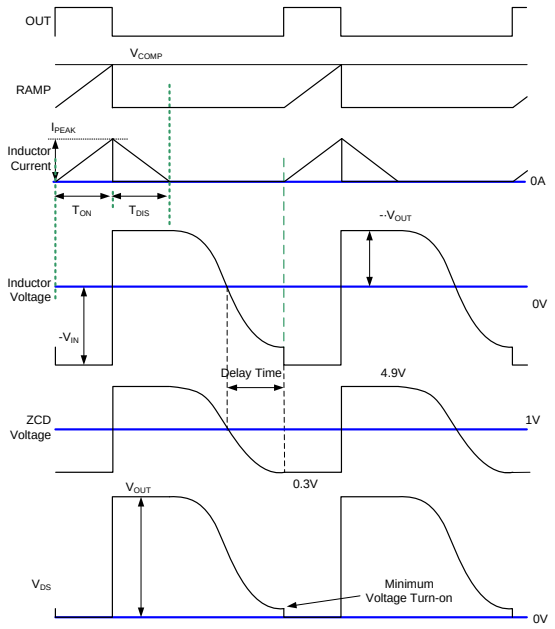


Fig. 4

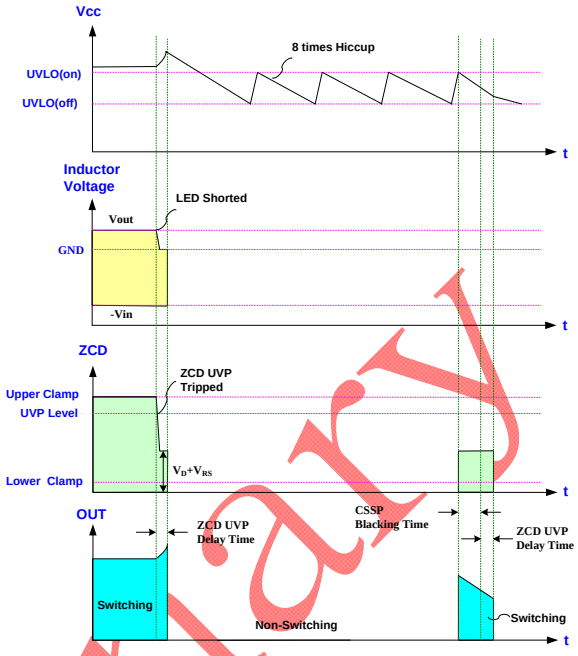


Fig. 5.

LED Short Protection (ZCD UVP) – Auto Recovery

To protect the circuit from damage due to LED short condition, a ZCD UVP function is implemented in the LD7832. The ZCD UVP function is an auto-recovery type protection. Fig. 5 shows the waveforms of the ZCD UVP operation. Under such fault condition, the reflected output voltage of inductor will pull down the ZCD voltage. If the ZCD voltage declines below to 4V and stays for over the ZCD UVP delay time, the protection will be activated to turn off the gate output until next UVLO(on). The ZCD UVP delay time is to prevent the false-trigger.

Over Current Protection (OCP)

The LD7832 detects the MOSFET current from the source pin, which is for the pulse-by-pulse current limit and output current feedback. The maximum voltage threshold of the source pin is set at 1.0V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{1.0V}{R_S}$$

Source/CS Short Protection (CSSP) – Auto Recovery

In order to prevent that the sense resistor (R_S) is shorted to damage LED driver, the protection is implemented on source pin. Fig. 6 shows the CSSP operation. Once the fault occurs, the source voltage will drop to GND level instantaneously and trigger the protection after the CSSP delay time which is to avoid the false-trigger. When VCC achieves the UVLO(on), LD7832 will start the CSSP blanking time to ignore CSSP function to pass though the start-up transient.

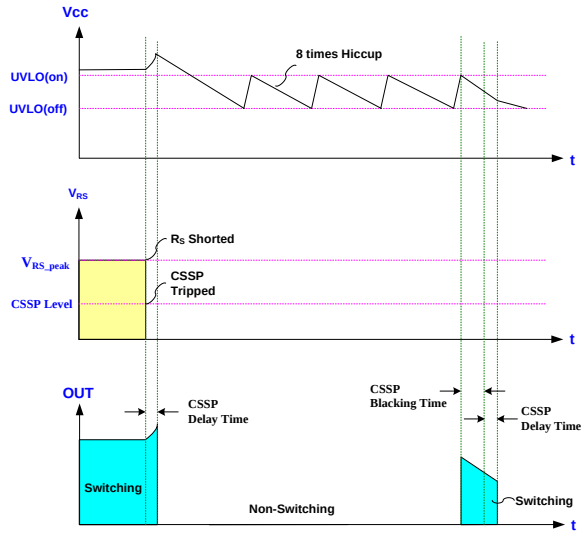


Fig. 7

Over Voltage Protection (VCC OVP)

The maximum rating of the VCC pin is limited below 30V. To prevent VCC from the fault condition, the LD7832 is implemented with OVP function on VCC pin. As soon as the VCC voltage is over OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on). The VCC OVP function of the LD7832 is an auto-recovery protection. The Fig. 7 shows its operation. Upon removal of the OVP condition will resume the VCC level and the output operation

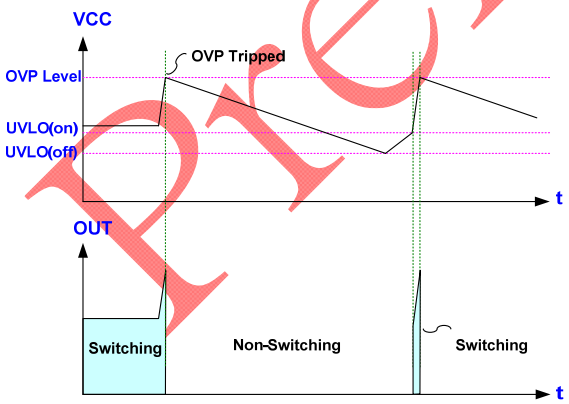


Fig. 7

Output Drive Stage

An output stage of a CMOS buffer, with typical 250mA/-500mA driving capability, is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Fault Protection

There are several critical protections were integrated in the LD7832 to prevent the power supply or adapter had being damaged. Those damages usually come from open or short condition on the pins of LD7832. Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. GND pin floating
2. CS pin floating

Reference Application Circuit