International
IOR Rectifier
DESIGN TIPS

DT 92-2A

INTERNATIONAL RECTIFIER • APPLICATIONS ENG. • 233 KANSAS ST. • EL SEGUNDO, CA. 90245 • TEL (310)322-3331 • FAX (310)322-3332

HIGH CURRENT BUFFER FOR CONTROL IC'S

By Laszlo Kiraly

INTRODUCTION

Modules and other paralleled MOS-gated power transistors can present difficulties to gate drive circuits. International Rectifier's family of Control IC drivers can provide large peak output currents acceptable for most applications. However, when driving the extremely large loads of many paralleled devices, excess power dissipation in the MOS-gate drive section of the Control IC may become an issue when switching above the few tens of kilohertz range. The subject of this Design Tip is a current-buffer to alleviate this problem.

The high input impedance power buffer shown in Figure 1 delivers 8A peak output current yet draws negligible quiescent current.

Q1 and Q2 are low current drivers for Q3 and Q4 which can be sized to suit the peak output current requirement.

OPERATION

When the input signal changes state, R1 limits the current through Q1 and Q2 for the few nanoseconds that both transistors are on.

When the input settles to its new state, the driver transistor quickly discharges the gate capacitance of the conducting output transistor forcing it into off-state. Meanwhile the gate of the other output transistor will be charged through R1; the turn-on will be delayed by the RC time constant formed by R1 and the input capacitance of the output transistor.

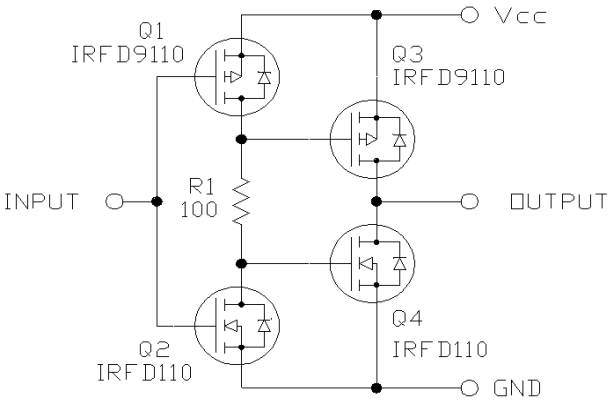

Figure 1

TEST RESULTS

The test circuit is shown in Figure 2. The buffer receives its drive signal from the IR2110, and drives an IGBT module which has a total gate charge (Q_G) of 600 nC. The IGBT module switches an inductive load current of 60A. The typical switching performance is shown in Figure 3. Turn-on and turn-off delays are 50 nS. Rise and fall times are less than 40 nS.

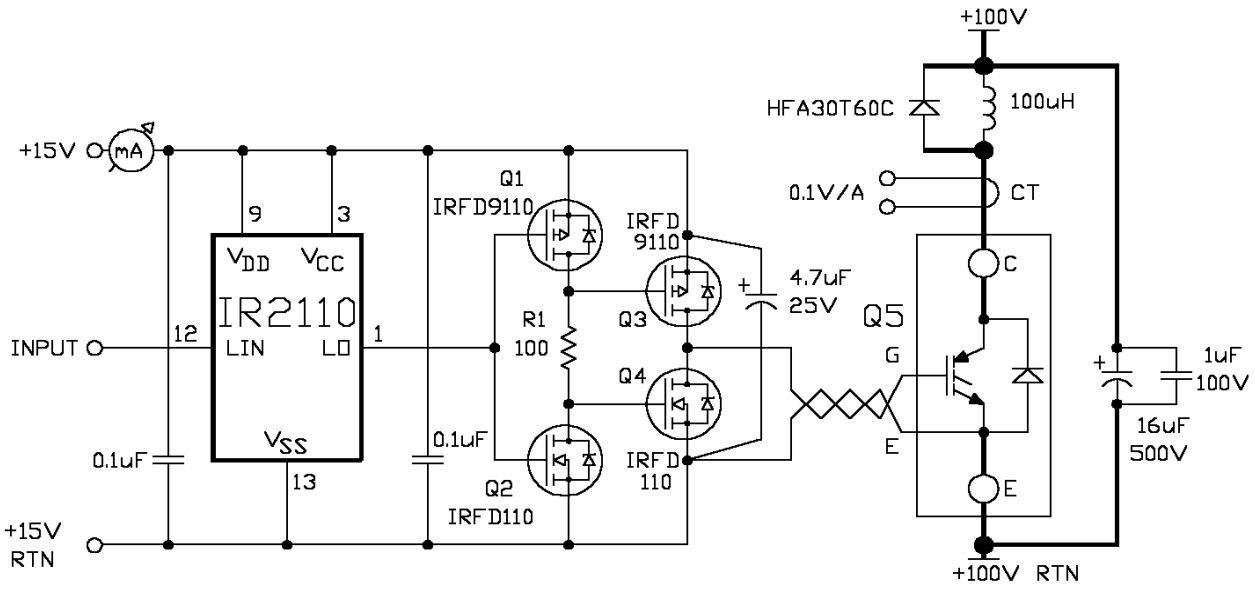

Figure 2
Test Circuit

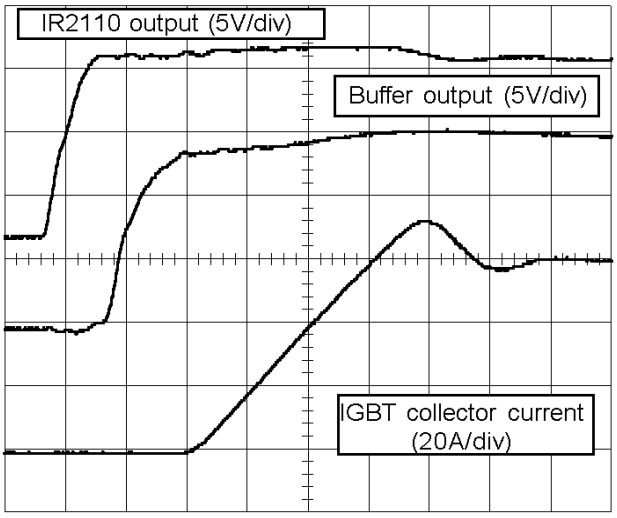

Figure 3a
Waveforms, turn-on. IGBT module switching inductive load of 60A.
(50 ns/div)

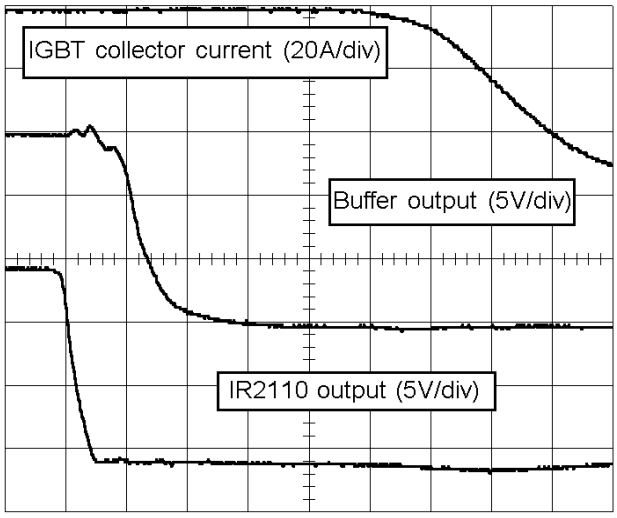

Figure 3b
Turn-off. Propagation delay is 50 ns, fall time is less than 40 nS when driving 600 nC gate charge of the module.
(50 ns/div)

The buffer was tested with a 0.1 µF capacitive load. The waveforms are shown in Figure 4. The ringing was due to the resonant circuit at the output, formed by the capacitive load and the stray inductances.

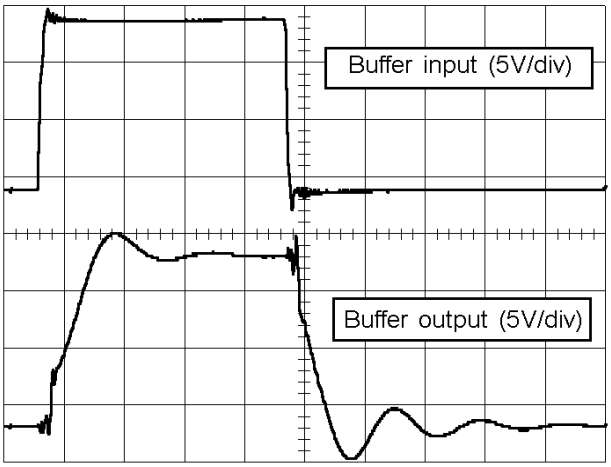

Figure 4
Waveforms driving 0.1 µF capacitor (250 ns/div)

The current consumption vs. frequency plot is shown in Figure 5.

APPLICATION SUGGESTIONS

A high current half-bridge circuit is shown in Figure 6.

It is possible to use lower voltage HEXFETs (i.e. 60V), but it was found that the large reduction in $R_{DS(on)}$ gave rise to large peak currents which caused a great deal of noise and ringing in the circuit.

LAYOUT SUGGESTIONS

- Use good quality 10 µF tantalum or 10 µF electrolytic and 0.1 µF ceramic capacitors at the output of the buffer. These decoupling capacitors should be mounted physically close to the output HEXFETs to nullify the effects of stray inductance. They reduce the ringing at the gate during turn-on.

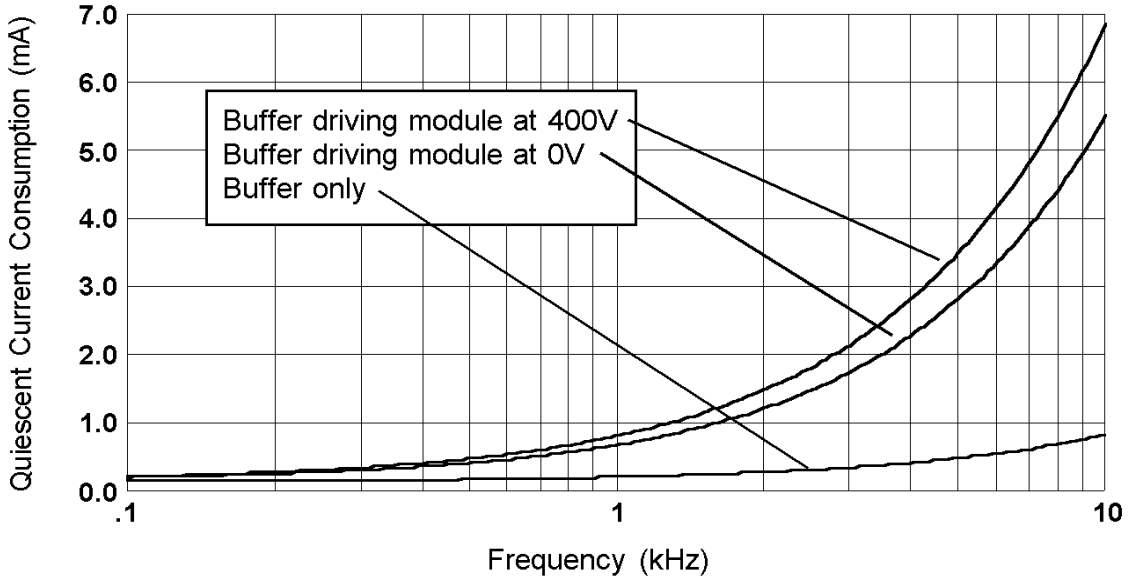

Figure 5
Current consumption vs. frequency

- Use short, tightly twisted wires between the output of the buffers and the modules.
- Use a single point ground at the emitter of the bottom IGBT module. In a bridge configuration, connect the emitters of the bottom IGBT modules to a common point with short heavy wires. Use this point as a common ground.
- Use a low ESR decoupling capacitor (Cf) at the power stage. The value of the capacitor depends on the quality of the layout and switched current. The typical value is between 10 µF and 1000 µF.

(HEXFET is the trademark for International Rectifier Power MOSFETs)

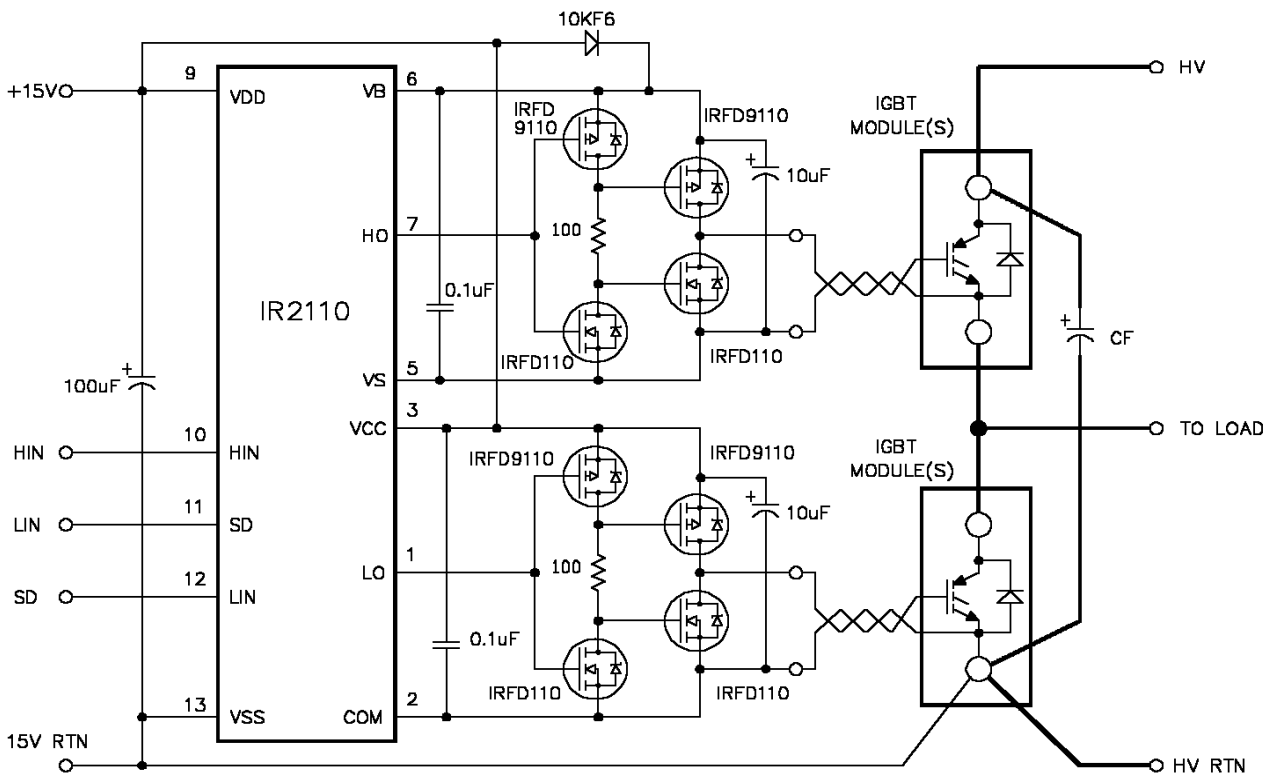

Figure 6
Application circuit schematic