HY4145 Datasheet

Single Cell Li+ Battery Gauge IC

With Protection

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1. General Description

The HY4145 operates with single Li+ battery cell as a stand–along battery gauge. Minimum firmware development support is required from system. The device uses GaugePack^{TM} algorithm, which mixes Coulomb–Counting and Open–Circuit–Voltage (OCV) measurements with battery cell characteristics to manage battery gauge, to maintain accurate battery capacity estimates with compensation for rate, temperature, age and self–discharge effects. The device provides voltage, current and thermal protection alerts, and also provides nonvolatile Flash memory for user purpose. The measured, estimated data set, protection information and specific application information on the device are accessible via a proprietary 1-Wire/2–Wire interface.

2. Features

- Used as Stand–alone Battery Gauge for Single Li+ Cell Battery Applications
  - Integrate Dual 16–Bit ADCs for Precision Voltage, Current, and Temperature Measurements
  - Use a Low Cost and Low Value Sense Resistor with Calibration for Current Measurement
  - Use Integrated and External Tempe rature Sensors for Temperature Measurement
- Integrate Accurate Battery Capacity Estimate System
  - Integrate GaugePack^{TM} Algorithm – Mixed Algorithm with Coulomb Counting, Open Circuit Cell Voltage Measurement and Cell Characteristics
  - Compensate Rate, Temperature, Age and Self–Discharge Effects Automatically
  - Require No Fully Battery Charge-to-Discharge or Discharge-to-Charge Recycling for Capacity Learning Process
  - Backup Specific Battery Capacity Information to Nonvolatile (NV) Flash Memory Automatically
- Feature Programmable Protection Alerts
  - Protections for Voltage, Current, and Temperature Faults
  - Provide Pin Alert for Voltage, Current, and Temperature Protection
- Feature Programmable Pin Indications
  - Battery Low Capacity Alert
- Backup Battery Lifetime Data to Nonvolatile (NV) Flash Memory Automatically
- Provide 96 Bytes Nonvolatile (NV) User Scratch Pad Flash Memory

- Support Low Power Modes Management
- Support Power Supply Management for Direct Battery Connection
- Support 1-Wire and 2–Wire Communication Interfaces
- Support SHA-1 Authentication for Safety
- Tiny, RoSH–free / Pb–free, 2.5mm x 4mm 12–pin DFN Package

3. Application

- Smartphone
- PDAs
- E-books
- Digital Still and Video Cameras
- Portable Instruments

4. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Material Composition	MSL[3]
HY4145-A012-01000	DFN	12	A	012	01000	Green[4]	MSL-3

1 Device No.:

For example, if the 01 version of battery gauge firmware (GaugePack™) and 000 version of data flash information are requested in DFN14 package for HY4145, the Device No. will be HY4145-C014-01000.

2 Code:

The battery gauge products can be coded with firmware portion and data flash portion. The two most significant digits present version of the firmware portion. The three less significant digits present version of the data flash portion.

3 MSL (Moisture Sensitivity Level):

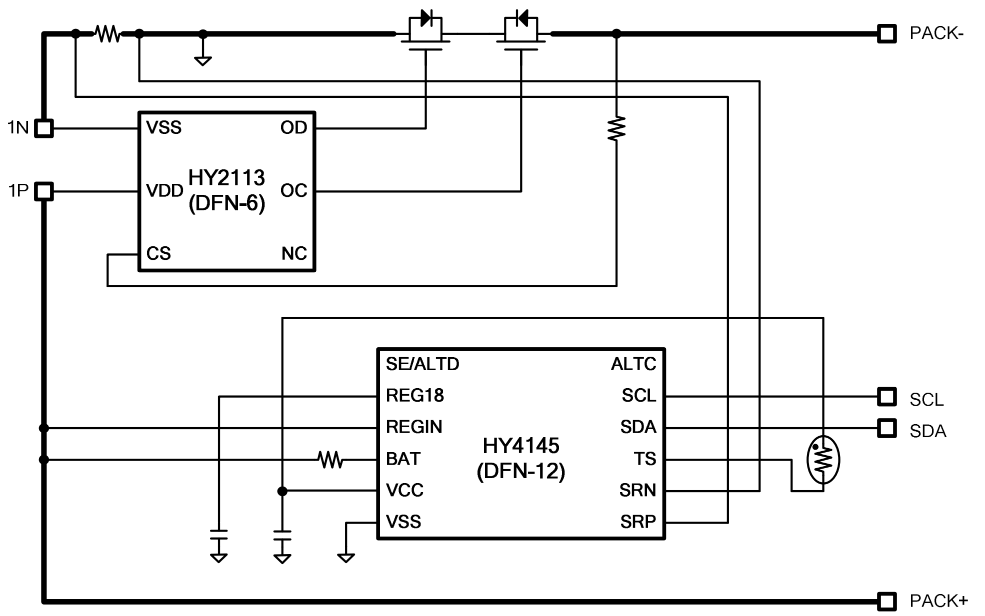
The moisture sensitivity level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

4 Green (RoHS & no Cl/Br):

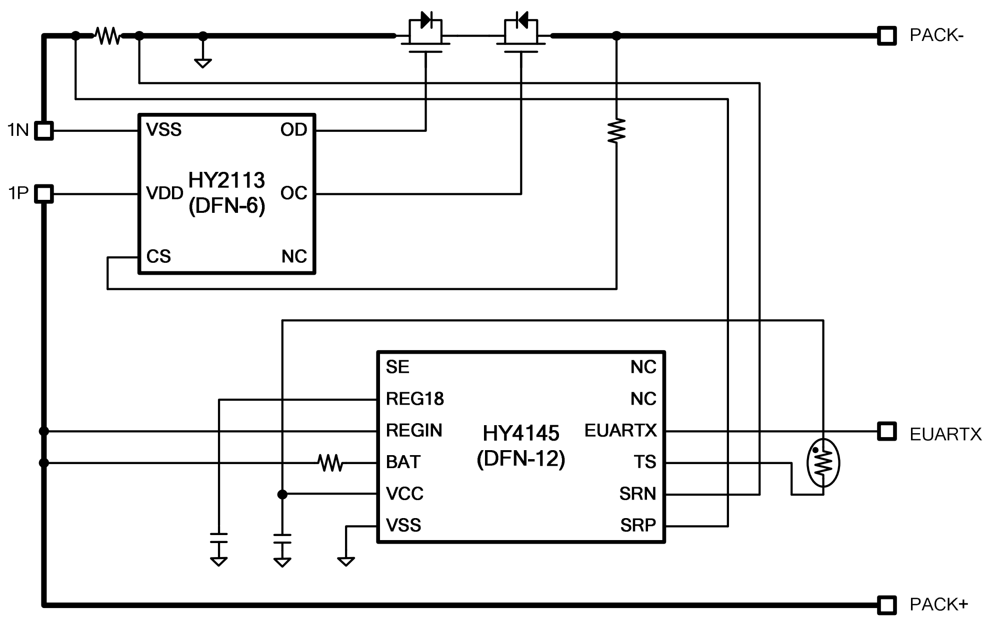
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%)

5. Application Circuit

2-Wire Interface Connection (Pack-side):

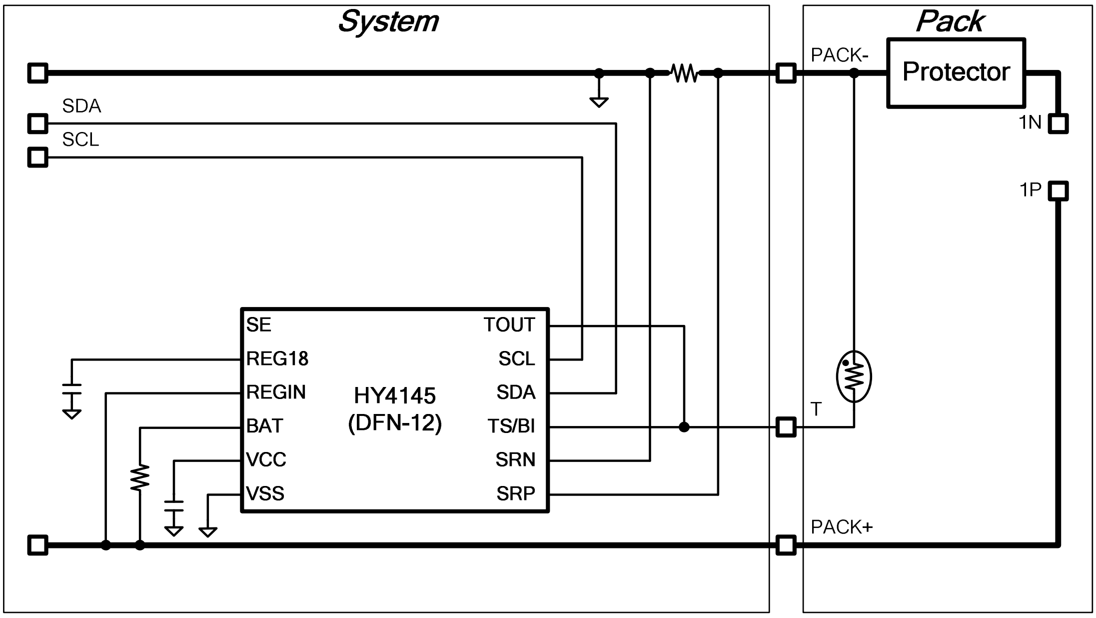


1-Wire Interface Connection (Pack-side):

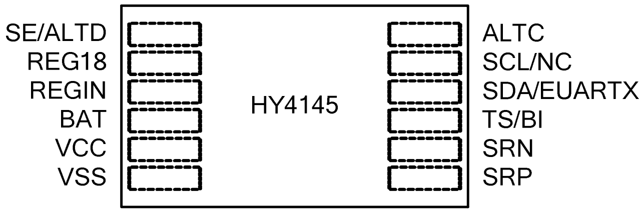


Note: I2C interface with be shipped as default. The command can make 1-Wire interface to replace I2C interface.

2-Wire Interface Connection (System-side):


System
Pack
SDA
SCL
PACK-
Protector
1N
1P
SE
REG18
REGIN
BAT
VCC
VSS
HY4145
(DFN-12)
TOUT
SCL
SDA
TS/BI
SRN
SRP
T
PACK+

6. Pin Configuration



2.5 mm x 4 mm DFN - 12

7. Pin Definition

PIN	TYPE[1]	NAME	DESCRIPTION
1	O	SEALTD	**Shutdown Enable Indication Output.** Used to indicate the device in Hibernate mode. A push-pull output. Active polarity configurable. **Discharge Protection Alert Indication Output.** Used to indicate the device in voltage, current, and temperature protection events during discharge. A push-pull output. Active polarity configurable. Note that the SE and ALTD pin can be configured to be used together or respectively. **Floated if not used.** Can be used if 2-wire communication in use.
2	OA	REG18	**1.8V Regulated Power Output.** A 1.8V regulated voltage output. Only for device use. Connect a 0.47uF ceramic capacitor to VSS.
3	P	REGIN	**Power Supply.** Connect to battery positive terminal. Connect a 0.1uF ceramic capacitor to VSS.
4	IA	BAT	**Battery Voltage Sense Input.** Used to measure battery voltage. Connect to battery positive terminal.
5	OA	VCC	**Regulated Power Supply.** A 3.0V regulated voltage output. Only for device use. Connect a 0.47uF ceramic capacitor to VSS.
6	P	VSS	**Device Ground.**
7	IA	SRP	**Current Sense Positive Input.** Connect to a 5mΩ to 20mΩ current sense resistor. Connect near to battery negative terminal.
8	IA	SRN	**Current Sense Negative Input.** Connect to a 5mΩ to 20mΩ current sense resistor. Connect near to VSS.
9	IA	TS	**Thermistor Sense Input.** Used to measure temperature in battery pack. An external high side thermistor connected to VCC used. A 20kΩ internal pull-down resister connected.
		BI	**Battery Insertion Input.**

PIN	TYPE(1)	NAME	DESCRIPTION
			Used to detect battery inserted, ex: HY4145 is used at system side.
10	I/OD	SDA	**Serial Data Input/Output.** Slave I^2C communication data line. Open–drain output. Use with an external 10kΩ pull–up resister.
		EUARTX	**Serial Data Input/Output.** Slave one-wire EUART communication data line. Open–drain output. Use with an external 10kΩ pull–up resister.
11	I	SCL	**Serial Clock Input.** Slave I^2C communication clock line. Use with an external 10kΩ pull–up resister. Can be floating if 1-Wire communication in use.
12	O	ALTC	**Charge Protection Alert Indication Output.** Used to indicate the device in voltage, current, and temperature protection events during charge. A push-pull output. Active polarity configurable. **Can not be floating if not used.** Can be used if 2-wire communication in use.
	OA	TOUT	**Power Output to Thermistor Network.** Connect a thermistor to VSS. A 200kΩ internal pull-up resister connected.

NOTE: (1) I = DIGITAL INPUT; O = DIGITAL OUTPUT; OD = OPEN-DRAIN OUTPUT; IA = ANALOG INPUT; OA = ANALOG OUTPUT; P = POWER CONNECTION.

8. Function Outline

The HY4145 functions as an accurate battery gauge for a battery pack using single Li+ cell. The device provides accurate estimates of capacity information and timely voltage, temperature and current measurements. Minimum firmware development support is required from system.

The proprietary GaugePack™ mixing Coulomb Counting and Open Circuit Cell Voltage (OCV) related algorithms estimates battery capacity to be the key to support precise battery information, such as Remaining Capacity (RC), State–Of–Charge (SOC), Time–To–Empty (TTE) and Time–To–Full (TTF), based on battery cell characteristics. With compensation for rate, temperature, age and self–discharge effects exercised, the performance of battery gauge is well improved. The configurable capacity learning process does not require any fully charge-to-discharge or discharge-to-charge battery cycling, and offers best opportunity to update status of battery capacity. The critical capacity information is periodically backed up into the integrated Flash memory in case of loss of power.

The HY4145 integrates two sets of precision 16–bit delta-sigma ADCs for voltage, temperature, and current measurements. The performance of measurements is optimized with appropriate calibrations and compensations during manufacturing and normal operation. The current is measured across a low costly, small value sense resistor (5mΩ to 20mΩ typically) located between battery and package terminals. The temperature can be measured from the integrated temperature sensor and the external thermistor network powered and controlled by the device.

The HY4145 features protection alerts for voltage, current and temperature faults during operation. The related thresholds and delays can be configured in user programmable Flash memory. A specific pin is assigned to indicate the voltage, current, and temperature protection events, and can be used to control external components. The device also features pin indications for low capacity faults during operation.

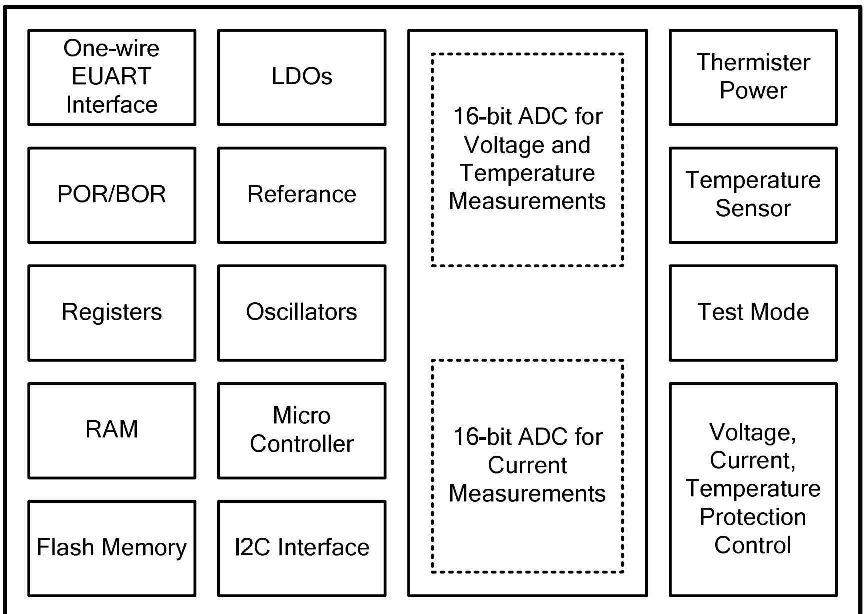
Battery cell and application information is stored in non-volatile Flash memory. Many of these Flash memory locations are accessible during application development. They can not be accessed directly during end–equipment operation. Access to these memory locations is achieved through individual commands, a sequence of data–flash–access commands, or use of the companion evaluation software.

The HY4145 provides 96 bytes of user programmable Flash memory, partitioned into three 32–byte blocks: Manufacturer Info Block A, Manufacturer Info Block B, and Manufacturer Info Block C. This data space is accessed through a Data Flash interface.

The HY4145 uses a proprietary 1-Wire/2–Wire communication interface, and executes commands. The measured, estimated data set, protection alerts, and specific application information are accessed through a series of commands, called *Standard Commands*. Further capability is provided by *Extended Commands*. These commands are used to read and write information contained within the HY4145 control and status registers, as well as the Flash memory locations. The 7–bit address **1010101** is assigned to the HY4145.

The HY4145 offers four power modes: NORMAL, SLEEP, FULLSLEEP, and HIBERNATE, to minimize power consumption and transits between modes automatically with appropriate configurable settings and communication events. Some of these modes can be initiated through commands.

9. Block Diagram



HY4145 Block Diagram

10. Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage on REGIN pin relative to VSS	–0.3V to 7.0V
Voltage on BAT1 pin relative to VSS	–0.3V to 12.0V
Voltage on BAT pin relative to VSS	–0.3V to 7.0V
Voltage on REG18, VCC pins relative to VSS	–0.3V to 3.6V
Voltage on SRP, SRN, TS/BI, SE, ALTD/TOUT, SE/ALTC	–0.3V to VCC + 0.3V
Voltage on SDA, SCL, EUARTX pins relative to VSS	–0.3V to 6.0V
Functional Temperature Range	–40℃ to +100℃
Storage Temperature Range	–65℃ to +150℃
Soldering Temperature (10 Sec)	+260℃

* *This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

ELECTRCAL CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{REGIN}	Normal operation.	3.0		5.5	V
		No Flash writes.	2.7		3.0	
Supply Current	I_{CC}	NORMAL Mode. (Note 1) $I_{LOAD} > I_{SLEEP}$		110		µA
	I_{SLP}	SLEEP Mode. $I_{LOAD} \leq I_{SLEEP}$		50		
	$I_{FULLSLP}$	FULLSLEEP Mode. $I_{LOAD} \leq I_{SLEEP}$		18		
	I_{HIB}	HIBERNATE Mode. $I_{LOAD} \leq I_{HIBERNATE}$		4		
Power–Up Communication Delay	t_{PUCD}			350		ms
SDA, SE, ALTD, ALTC, EUARTX Output Logic Low	V_{OL}	I_{OL} = 3mA			0.4	V
SE, ALTD, ALTC Output Logic High	V_{OH}	I_{OH} = –1mA	V_{CC} – 0.5			V

SDA Output Logic High	$V_{OH(OD)}$	External pull–up resisters to VCC. I_{OH} = –1mA	V_{CC} – 0.5			V
SDA, SCL, EUARTX Input Logic Low	V_{IL}		–0.3		0.6	V
SDA, SCL, EUARTX Input Logic High	V_{IH}		1.2		6.0	V
BAT Input Voltage Range			V_{SS} – 0.125		V_{SS} + 5.0	V
SRP, SRN Input Voltage Range			V_{SS} – 0.125		V_{SS} + 0.125	V
TS Input Voltage Range			V_{SS} – 0.125		V_{CC} – 0.1	V

POWER–ON RESET

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power–On–Reset Voltage	V_{POR}		1.90	2.00	2.10	V

3.0V LDO REGULATOR

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Output Voltage, VCC	V_{CC}	$V_{CC} + V_{DROP} \le V_{REGIN} \le$ 4.5V, $I_{CC} \le$ 3mA, T_A = 25°C	2.7	3.0	3.3	V
		2.7V $\le V_{REGIN} \le V_{CC} + V_{DROP}$, I_{CC} = 3mA, T_A = 25°C	V_{REGIN} - 0.18	V_{REGIN} - 0.21	V_{REGIN} - 0.25	
Dropout Voltage	V_{DROP}	I_{CC} = 1mA, T_A = 25°C	60	70	80	mV
		I_{CC} = 3mA, T_A = 25°C	180	210	240	mV
Temperature Regulation	dV_{CC_TEMP}	I_{CC} = 0, 1, 2, 3mA		500		ppm/°C
Line Regulation	dV_{CC_LINE}	I_{CC} = 1mA, 3.5V $\le V_{REGIN} \le$ 4.5V		30		mV/V
Load Regulation	dV_{CC_LOAD}	$I_{CC} \le$ 3mA, V_{REGIN} = 3.6V		12		mV

1.8V LDO REGULATOR

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Output Voltage, V_{REG18}	V_{REG18}	$I_{REG18} \le$ 3mA	1.6	1.8	2.0	V
Temperature Regulation	dV_{REG18_TEMP}	I_{REG18} = 0, 1, 2, 3mA		500		ppm/°C
Line Regulation	dV_{REG18_LINE}	I_{REG18} = 1mA		12		mV/V
Load Regulation	dV_{REG18_LOAD}	$I_{REG18} \le$ 3mA, V_{REGIN} = 2.7V		6		mV

THERMISTOR SENSE CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TS Output Resistance	R_{TS}		33	44	55	kΩ
TS Output Resistance Temperature Coefficient	TC_{TS}			25		PPM/°C

THERMISTOR DRIVE CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{TOUT}	I_{TOUT} = 0		V_{CC}		V
TOUT Pass Element Resistance	$R_{DS,ON}$	I_{TOUT} = 1mA		50	100	Ω

ULTRA HIGH FREQUENCY OSCILLATOR CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OSC}			8		MHz
Startup Delay	t_{SXO}			2.5	5	ms

HIGH FREQUENCY OSCILLATOR CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OSC}			2		MHz
Startup Delay	t_{SXO}			2.5	5	ms

LOW FREQUENCY OSCILLATOR CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OSC}			32.768		KHz
Frequency Error	f_{EIO}	0 ≤ Ta ≤ 60ºC	–1.5	0.25	1.5	%
		–20ºC ≤ Ta ≤ 70ºC	–2.5	0.25	2.5	
		–40ºC ≤ Ta ≤ 85ºC	–4.0	0.25	4.0	
Startup Delay	t_{SXO}				500	µs

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage Range (V_{SRN} and V_{SRP})	$V_{SR,IN}$	$V_{SR} = V_{SRP} – V_{SRN}$	–0.15		0.15	V
Conversion Time	t_{SXO}	Single conversion		1		s
Resolution		Single conversion	15		16	bits
Full Scale Error	$V_{SR,ERR}$			0.35		%
Full Scale Drift	$V_{SR,DRIFT}$			150		PPM/°C
Offset Error	$V_{SR,OS}$			10		µV
Offset Error Drift	$V_{SR,OS,DRIFT}$			0.4	2.7	µV/°C
Integral Nonlinearity Error	I_{NL}			±0.007	±0.034	FSR
Effective Input resistance	$Z_{SR,IN}$		2.5			MΩ
Input Leakage Current	$I_{SR,LKG}$				0.3	µA

ADC (TEMPERATURE AND BATTERY MEASUREMENT) CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 2.7V to 5.5V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage Range	$V_{ADC,IN}$		–0.2		1	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time	t_{SXO}	Single conversion		250		ms
Resolution		Single conversion	14		15	bits
Offset Error	$V_{ADC,OS}$			10		µV
Full Scale Error	$V_{ADC,ERR}$			0.1	0.7	%
Full Scale Drift	$V_{ADC,DRIFT}$			50		PPM/°C
Input Offset	$V_{ADC,OS}$			1		mV
Offset Error Drift	$V_{ADC,OS,DRIFT}$			2.5	18	µV/°C
Integral Nonlinearity Error	I_{NL}			±0.007	±0.034	FSR
Effective Input resistance	$Z_{ADC,IN}$		2.5			MΩ
Input Leakage Current	$I_{ADC,LKG}$				0.3	µA

DATA FLASH MEMORY CHARACTERISTICS

($V_{REGIN} = V_{BAT} = 3.3V$. $C_{REGIN} = 0.1uF$. $C_{VCC} = 0.47uF$. $C_{REG18} = 0.47uF$. $T_A = –40°C$ to $+85°C$. Unless otherwise noted, typical values are at $T_A = 25°C$ and $V_{REGIN} = V_{BAT} = 3.6V$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention	T_{DR}		10			Years
Flash Programming Write Cycles			20000			Cycles
Row Programming Time	$t_{ROWPROG}$				2	ms
Mass Erase Time	$t_{MassErass}$				200	ms
Page Erase Time	$t_{PageErass}$				20	ms
Flash Write Supply Current	I_{CCPROG}			5	10	mA
Flash Erase Supply Current	$I_{CCERASE}$			5	10	mA

2–WIRE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

($V_{REGIN} = V_{BAT} = 1.8V$. $C_{REGIN} = 0.1uF$. $C_{VCC} = 0.47uF$. $C_{REG18} = 0.47uF$. $T_A = –40°C$ to $+85°C$. Unless otherwise noted, typical values are at $T_A = 25°C$ and $V_{REGIN} = V_{BAT} = 3.6V$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 1)	0		400	KHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 2)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs

High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 3, 4)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 3)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + $0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + $0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 5)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 6)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 1: Timing must be fast enough to prevent the HY4145 from entering sleep mode due to bus low for period > t_{SLEEP}.

Note 2: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

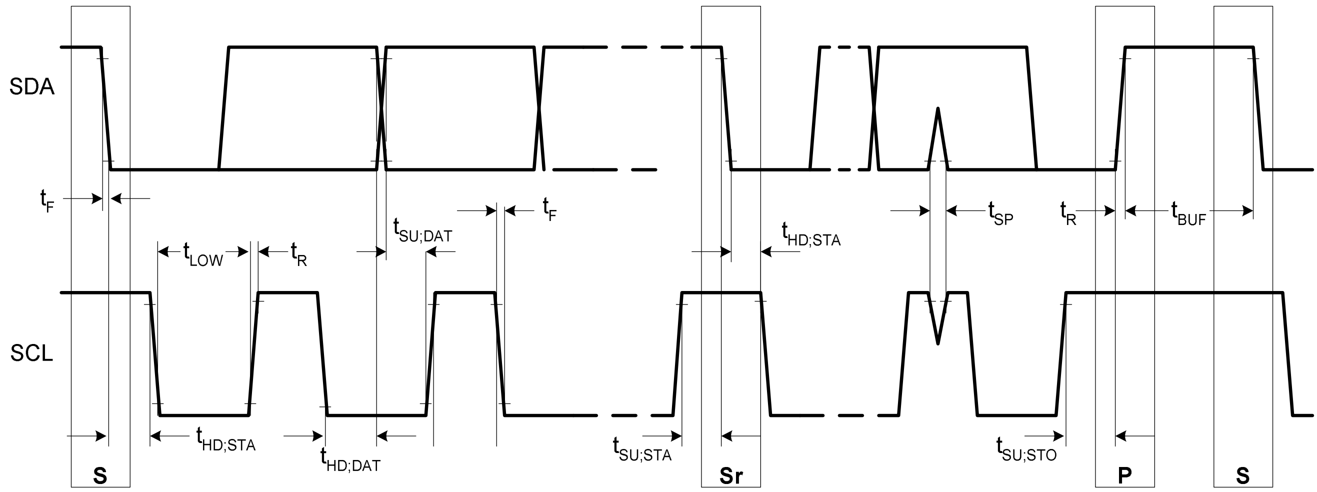
Note 3: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 4: This device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 5: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 6: C_b – total capacitance of one bus line in pF.

Figure 1. I²C Bus Timing Diagram



1–WIRE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

(V_{REGIN} = V_{BAT} = 1.8V. C_{REGIN} = 0.1uF. C_{VCC} = 0.47uF. C_{REG18} = 0.47uF. T_A = –40°C to +85°C. Unless otherwise noted, typical values are at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 1)	0		400	KHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 2)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 3, 4)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 3)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + $0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + $0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 5)	0		50	ns

Capacitive Load for Each Bus Line	C_B	(Note 6)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 1: Timing must be fast enough to prevent the HY4145 from entering sleep mode due to bus low for period > t_{SLEEP}.

Note 2: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 3: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 4: This device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 5: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 6: C_b – total capacitance of one bus line in pF.

11. Data Commands

Standard Commands

The HY4145 uses a series of 2–byte standard communication protocol to enable system reading and writing of battery information. Each standard command has associated command code(s), as indicated in Table 1. Because each command consists of two bytes of data, two consecutive transmissions must be executed both to initiate the command function, and to read or write the corresponding two bytes of data. Additional options for transferring data, such as spooling, are described in Section, *I²C Interface*. Standard commands are accessible in NORMAL mode operation. The read/write permissions depend on the NORMAL access mode, FULL ACCESS, SEALED or UNSEALED (for details about the access modes, refer to Section *Access Modes*.)

Table 1. STANDARD COMMANDS

COMMAND	ACCESS[1]	NAME	FORMAT[2]	MINIMUM	MAXIMUM	DEFAULT	UNIT
0x00 / 0x01	R/W	Control()	Hex	0x0000	0xffff	—	—
0x02 / 0x03	R/W	AtRate()	I2	–32768	0	—	mA
0x04 / 0x05	R	AtRateTimeToEmpty()	U2	0	65535	—	minute
0x06 / 0x07	R	Temperature()	U2	0	65535	—	0.1ºK
0x08 / 0x09	R	Voltage()	U2	0	65535	—	mV
0x0a / 0x0b	R	Flags()	U2	0x0000	0xffff	—	—
0x0c / 0x0d	R	NominalAvailableCapacity()	U2	0	65535	—	mAh
0x0e / 0x0f	R	FullAvailableCapacity()	U2	0	65535	—	mAh
0x10 / 0x11	R	RemainingCapacity()	U2	0	65535	—	mAh
0x12 / 0x13	R	FullChargeCapacity()	U2	0	65535	—	mAh
0x14 / 0x15	R	AverageCurrent()	I2	–32768	32767	—	mA
0x16 / 0x17	R	RunTimeToEmpty()	U2	0	65535	—	minute
0x18 / 0x19	R	AverageTimeToFull()	U2	0	65535	—	minute
0x1a / 0x1b	R	StandbyCurrent()	I2	–32768	32767	—	mA
0x1c / 0x1d	R	StandbyTimeToEmpty()	U2	0	65535	—	minute
0x1e / 0x1f	R	MaxloadCurrent()	I2	–32768	32767	—	mA
0x20 / 0x21	R	MaxloadTimeToEmpty()	U2	0	65535	—	minute
0x22 / 0x23	R	AvailableEnergy()	U2	0	65535	—	10mWh
0x24 / 0x25	R	AvailablePower()	U2	0	65535	—	10mW
0x26 / 0x27	R	TimeToEmptyatContantPower()	U2	0	65535	—	minute
0x28 / 0x29	R	InternalTemperature()	U2	0	65535	—	0.1ºK
0x2a / 0x2b	R	CycleCount()[3]	U2	0	65535	—	cycle

							count
0x2c / 0x2d	R	RelativeStateOfCharge()	U2	0	100	—	%
0x2e / 0x2f	R	StateOfHealth()	U2	0	200	—	% / num
0x30 / 0x31	R	Current()	I2	–32768	32767	—	mA
0x32 / 0x33	R	SafetyStatus()	U2	0x0000	0xffff	0x0000	—
0x34 / 0x35	R	PassedCharge()	U2	0	65535	—	0.25mAh
0x36 / 0x37	R	DepthOfDischarge0()	U2	0	0xffff	—	Hex

1. SEALED and UNSEALED modes are entered via commands to *Control()* plus access keys.
2. I2 = 2-byte Signed Integer; U2 = 2-byte Unsigned Integer.
3. Critical register value is automatically saved to Flash Data during NORMAL mode operation and recalled from Flash Data on Power–On–Reset procedure.

Control Commands

Issuing command *Control()* requires a series of 2–byte standard communication protocol. These additional bytes specify the specific control function desired during normal operation and features when the HY4145 is in different access modes, as indicated in Table 2.

Table 2. Control() SUBCOMMANDS

COMMAND	ACCESS	FUNCTION	DESCRIPTION	DEFAULT
0x0000	R	ControlStatus()	Reports the status of data flash checksum, hibernate, etc.	—
0x0001	R	DeviceType()	Reports the device type (HY4145).	0x4145
0x0002	R	FirmwareVersion()	Reports the firmware version on the device.	—
0x0003	R	HardwareVersion()	Reports the hardware version on the device.	—
0x0004	R	DFChecksum()	Calculates a Data Flash checksum and reports the checksum on a read.	—
0x000c	R	DFVersion()	Reports the Data Flash version on the device.	—
0x0010	W	SetFullSleep()	Forces ControlStatus().FULLSLEEP to 1.	—
0x0011	W	SetHibernate()	Forces ControlStatus().HIBERNATE to 1.	—
0x0012	W	ClearHibernate()	Forces ControlStatus().HIBERNATE to 0.	—
0x0013	W	SetShutdown()	Enables the SE pin to change state.	—
0x0014	W	ClearShutdown()	Disables the SE pin from changing state.	—
0x0020	No[1]	SealedDevice()	Places the device into SEALED state.	—
0x0022	R	IFChecksum()	Calculates an Instruction Flash checksum and reports the checksum on a read.	—
0x0040	No[1]	CalibrationMode()	Places the device in calibration mode.	—
0x0041	W	Reset()	Forces a full reset of the device. It is a one-shot action.	—
0x0042	W	QuickStart()	Forces a re-calculation about capacity information.	—
0x0043	No[1]	DesignCapacity()	Write Design Capacity() in data flash.	—
0x0044	No[1]	CycleCount()	Write Cycle Count() in data flash.	—
0x0045	No[1]	CellAge()	Write Cell Age() in data flash.	—
0x0046	W	ClearLearned()	Forces Flag().LRND to 0.	—
0x0055	R	ChipType()	Chip Type, and fixed with part number.	0x4145
0x0085	No[1]	Set2Wire()	Force 2-Wire interface for communication.	—
0x0086	No[1]	Set1Wire()	Force 1-Wire interface for communication.	—

1. CAN be written in SEALED mode; CANNOT be written in UNSEALED mode.

Extended Commands

Extended commands offer more functionality beyond the standard commands. Each extended command has associated command code(s), as indicated in Table 3. These command code(s) is not limited to be a 2–byte word. The read/write permissions depend on the NORMAL access mode, FULL ACCESS, SEALED or UNSEALED (for details about the access modes, refer to Section *Access Modes*.)

Table 3. EXTENDED COMMANDS

COMMAND	SEALED	UNSEALED	DESCRIPTION	FORMAT[1]	UNIT
0x38	R	R	WakeCurrentThreshold()	I1	mV
0x39	R	R	OperationConfigB()	Hex	—
0x3a / 0x3b	R	R	OperationConfigA()	Hex	—
0x3c / 0x3d	R	R	DesignCapacity()	U2	mAh
0x3e	N/A	R/W	DataFlashClass()[2]	Hex	—
0x3f	N/A	R/W	DataFlashBlock()[2]	Hex	—
0x40 to 0x53	R/W	R/W	BlockData() / Authenticate()[3]	Hex	—
0x54	R/W	R/W	BlockData() / AuthenticateCheckSum()	Hex	—
0x55 to 0x5f	R	R/W	BlockData()	Hex	—
0x60	N/A	R/W	BlockDataChecksum()	Hex	—
0x61	N/A	R/W	BlockDataControl()	Hex	—
0x62	R	R	DeviceNameLength()	Hex	—
0x63 to 0x69	R	R	DeviceName()	Hex	—

1. I1 = 1-byte Signed Integer; U2 = 2-byte Unsigned Integer.
2. In SEALED mode, Data Flash CANNOT be accessed through commands 0x3e and 0x3f.
3. The BlockData( ) command area shares functionality for accessing general data flash and for using Authentication.

Data Flash

In HY4145, Data Flash is a non–volatile memory that contains initialization default values, battery status, calibration information, configuration information, and application information. The Data Flash can be access in several different ways, depending on what mode the HY4145 is operating in and what data is being accessed. The Data Flash locations are summarized in Table 4.

Table 4. DATA FLASH SUMMARY

CLASS	SUBCLASS ID	SUBCLASS	OFFSET	FORMATE	NAME	MINIMUM	MAXIMUM	DEFAULT	UNIT
1st Level Safety	1	Voltage	0	I2	Low Temp Over Voltage (LT OV) Threshold	3700	5000	4300	mV
1st Level Safety	1	Voltage	2	I2	Low Temp Over Voltage (LT OV) Recovery	0	4400	3900	mV
1st Level Safety	1	Voltage	4	I2	Standard Temp Over Voltage (ST OV) Threshold	3700	5000	4500	mV
1st Level Safety	1	Voltage	6	I2	Standard Temp Over Voltage (ST OV) Recovery	0	4400	4100	mV
1st Level Safety	1	Voltage	8	I2	High Temp Over Voltage (HT OV) Threshold	3700	5000	4400	mV
1st Level Safety	1	Voltage	10	I2	High Temp Over Voltage (HT OV) Recovery	0	4400	4000	mV
1st Level Safety	1	Voltage	12	U1	Over Voltage (OV) Time	0	240	8	s
1st Level Safety	1	Voltage	13	I2	Under Voltage (UV) Threshold	0	3500	2200	mV
1st Level Safety	1	Voltage	15	I2	Under Voltage (UV) Recovery	0	3600	3000	mV
1st Level Safety	1	Voltage	17	U1	Under Voltage (UV) Time	0	240	8	s
1st Level Safety	1	Current	32	I2	Charge Over Current (COC) Threshold	0	20000	6000	mA
1st Level Safety	1	Current	34	I2	Charge Over Current (COC) Recovery	0	1000	300	mA
1st Level	1	Current	36	U1	Charge Over Current	0	240	8	s

Safety					(COC) Time				
1st Level Safety	1	Current	38	I2	Discharge Over Current (DOC) Threshold	0	20000	6000	mA
1st Level Safety	1	Current	40	I2	Discharge Over Current (DOC) Recovery	0	1000	300	mA
1st Level Safety	1	Current	42	U1	Discharge Over Current (DOC) Time	0	240	8	s
1st Level Safety	1	Current	43	U1	Current Recovery Time	0	240	8	s
1st Level Safety	1	Temp	64	I2	Charge Over Temp 1 (COT1) Threshold	0	2550	550	0.1ºC
1st Level Safety	1	Temp	66	I2	Charge Over Temp 1 (COT1) Recovery	0	2550	500	0.1ºC
1st Level Safety	1	Temp	68	U1	Charge Over Temp 1 (COT1) Time	0	240	2	s
1st Level Safety	1	Temp	69	I2	Discharge Over Temp 1 (DOT1) Threshold	0	2550	600	0.1ºC
1st Level Safety	1	Temp	71	I2	Discharge Over Temp 1 (DOT1) Recovery	0	2550	550	0.1ºC
1st Level Safety	1	Temp	73	U1	Discharge Over Temp 1 (DOT1) Time	0	240	2	s
1st Level Safety	1	Temp	74	I2	Discharge Start High Temp (DHT) Threshold	0	1200	600	0.1ºC
1st Level Safety	1	Temp	76	I2	Discharge Start High Temp (DHT) Recovery	0	1200	550	0.1ºC
Charge Ctrl	5	Charge Temp	0	I2	JEITA Temp 1 (JT1)	–400	1200	0	0.1ºC
Charge Ctrl	5	Charge Temp	2	I2	JEITA Temp 2 (JT2)	–400	1200	120	0.1ºC
Charge Ctrl	5	Charge Temp	4	I2	JEITA Temp 3 (JT3)	–400	1200	450	0.1ºC
Charge Ctrl	5	Charge Temp	6	I2	JEITA Temp 4 (JT4)	–400	1200	550	0.1ºC
Charge Ctrl	5	Charge Temp	8	I2	Temp Hysteresis	0	100	10	0.1ºC
General Cfg	3	General Data	0	H1	Operation Cfg B	0x00	0xff	0xF0	—

General Cfg	3	General Data	1	H1	Operation Cfg A High	0x00	0xff	0x00	—
General Cfg	3	General Data	2	H1	Operation Cfg A Low	0x00	0xff	0x31	—
Battery Cfg	3	Battery Data	3	I2	Design Capacity (DC)	0	32767	8996	0.25mAh
Battery Cfg	3	Battery Data	5	U2	Design Age	0	25600	2.93	% per 100 cycles
Battery Cfg	3	Battery Data	7	I2	Termination Voltage	0	4500	3000	mV
Charge Ctrl	3	Charge Termination	11	I2	Charging Voltage	0	1000	4200	mV
Charge Ctrl	3	Charge Termination	13	I1	Taper Voltage	0	255	100	mV
Charge Ctrl	3	Charge Termination	14	I2	Taper Current	0	1000	100	mA
Charge Ctrl	3	Charge Termination	16	I1	Current Taper Window	0	60	40	s
Charge Ctrl	3	Charge Termination	17	I1	Minimum Taper Charge	0	1000	25	0.01mAh
Gauge	3	Current Data	18	I2	Initial Maximum Current	32767	0	440	mA
Gauge	3	Current Data	20	I2	Initial Standby Current	256	0	44	mA
Gauge	3	Current Data	22	I2	State Of Health Current	32767	0	100	mA
Gauge	3	Current Threshold	24	I2	Quit Current Threshold	0	1000	15	mA
Gauge	3	Learning Threshold	28	H1	Relaxation Voltage Time Threshold	0x00	0xff	0x0E	—
Gauge	3	Learning Threshold	29	U1	SOC Delta Threshold	0	255	40	%
Gauge	3	Learning Threshold	30	U1	SOC Learning Qualification Threshold	0	255	15	%
Gauge	3	Learning Threshold	31	U1	SOC Learning High Threshold	0	255	40	%
Gauge	3	Learning Threshold	32	U1	SOC Learning Low Threshold	0	255	20	%
Gauge	3	Capacity Threshold	33	I2	SOC1 Set Threshold	0	65535	150	mAh
Gauge	3	Capacity Threshold	35	I2	SOC1 Clear Threshold	0	65535	175	mAh
Gauge	3	Capacity Threshold	37	I2	SOCF Set Threshold	0	65535	75	mAh

Gauge	3	Capacity Threshold	39	I2	SOCF Clear Threshold	0	65535	100	mAh
Gauge	3	Current Sense	41	I2	Sense Resistor	0	65535	10000	µΩ
Gauge	3	Current Sense	43	I2	Sense Resistor Temp Coefficient	–3840	3840	0	0.117 ppm/ºK
Power	3	Current Threshold	45	I1	Sleep Current	0	100	10	mA
Power	3	Current Threshold	46	I1	Hibernate Current	0	255	3	mA
Power	3	Voltage Threshold	47	I2	Hibernate Voltage	2400	3000	2700	mV
Power	3	Current Threshold	49	I2	Charge Current Threshold	0	1000	40	mA
Power	3	Current Threshold	51	I1	Discharge Current Threshold	0	255	30	mA
Power	3	Time Threshold	52	U1	Full Sleep Wait Time	0	255	180	s
Power	3	Current Threshold	53	I1	Wake Current Threshold	0	255	240	40µV
Power	3	Current Threshold	54	I2	Deadband	0	5	5	mA
Flash Cfg	3	Voltage Threshold	56	I2	Flash Update OK Voltage	2000	5000	3100	mV
Gauge	3	Capacity Data	58	I2	Reserve Capacity	0	9000	0	mAh
Manufacture Data	6	Manufacture Data	0	H2	Pack Lot Code	0x0000	0xffff	0x0000	—
Manufacture Data	6	Manufacture Data	2	H2	PCB Lot Code	0x0000	0xffff	0x0000	—
Manufacture Data	6	Manufacture Data	4	H2	Firmware Revision	0x0000	0xffff	—	—
Manufacture Data	6	Manufacture Data	6	H2	Hardware Revision	0x0000	0xffff	—	—
Manufacture Data	6	Manufacture Data	8	H2	Cell Revision	0x0000	0xffff	0x0001	—
Manufacture	6	Manufacture	10	H2	Flash Data Revision	0x0000	0xffff	0x0001	—

Data		Data							
Manufacture Data	6	Manufacture Data	12	H2	Device Type	0x0000	0xffff	0x4145	—
Manufacture Data	6	Manufacture Data	32	H2	Specification Info	0x0000	0xffff	0x0031	—
Manufacture Data	6	Manufacture Data	34	U2	Manufacturer Date	0	65535	0	—
Manufacture Data	6	Manufacture Data	36	H2	Serial Number	0x0000	0xffff	0x0001	—
Manufacture Data	6	Manufacture Data	38	S21	Manufacturer Name	—	—	Hycontek	ASCII
Manufacture Data	6	Manufacture Data	50	S21	Device Name	—	—	HY4145	ASCII
Manufacture Data	6	Manufacture Data	58	S5	Device Chemistry	—	—	LION	ASCII
Manufacturer Info	32	Manufacturer Info	32 – 63	S32	Block A [0 – 31]	—	—	—	—
Manufacturer Info	32	Manufacturer Info	64 – 95	S32	Block B [0 – 31]	—	—	—	—
Manufacturer Info	32	Manufacturer Info	96 – 127	S32	Block C [0 – 31]	—	—	—	—
Thermistor	30	Data	0 – 93	I47	Thermistor Info	—	—	—	—
Lifetime Data	9	Temp Data	0	I2	Lifetime Maximum Temp	0	1400	300	0.1ºC
Lifetime Data	9	Temp Data	2	I2	Lifetime Minimum Temp	0	1400	200	0.1ºC
Lifetime Data	9	Voltage Data	4	I2	Lifetime Maximum Cell Voltage	0	32767	3500	mV
Lifetime Data	9	Voltage Data	6	I2	Lifetime Minimum Cell Voltage	0	32767	3200	mV
Lifetime Data	9	Current Data	12	I2	Lifetime Maximum Charge Current	–32767	32767	1500	mA
Lifetime Data	9	Current Data	14	I2	Lifetime Maximum Discharge Current	–32767	32767	–3000	mA
Gauge	9	Battery Data	76	I2	Design Capacity (DC)	0	32767	8696	0.25mAh
Gauge	9	Battery Data	78	U2	Cycle Count	0	65535	0	%

Gauge	9	Battery Data	80	I2	Cell Age	0	25600	2.93	% per 100 cycles
Lifetime Data	9	Current Data	82	I2	Lifetime Maximum Average Discharge Current	–32767	32767	–1000	mA
Lifetime Data	9	Temp Data	84	I2	Lifetime Average Temp	0	1400	250	0.1ºC
Lifetime Data	9	Temp Data	86	I2	Lifetime Over Temp Count	0	65535	0	count
Lifetime Data	9	Temp Data	88	I2	Lifetime Over Temp Duration	0	65535	0	s
Lifetime Data	9	Voltage Data	90	I2	Lifetime Over Voltage Count	0	65535	0	count
Lifetime Data	9	Voltage Data	92	I2	Lifetime Over Voltage Duration	0	65535	0	s
Lifetime Data	9	Temp Data	94	I4	Lifetime Temp Sample Count	0	140000000	0	num
Lifetime Data	9	Flash Data	96	I2	Lifetime Flash Update Count	0	32767	0	num
Lifetime Data	7	Resolution	0	I1	Lifetime Temp Resolution	0	255	10	0.1ºC
Lifetime Data	7	Resolution	1	I1	Lifetime Voltage Resolution	0	255	25	mV
Lifetime Data	7	Resolution	2	I1	Lifetime Current Resolution	0	255	100	mA
Lifetime Data	7	Resolution	3	I1	Lifetime Update Time	0	65535	60	s
Calibration	2	Data	0	I3	CC Gain	—	—	—	—
Calibration	2	Data	3	I3	Voltage Gain	—	—	—	—
Calibration	2	Data	8	I2	Internal Temp Gain	—	—	—	—
Calibration	2	Data	6	I2	External Temp 1 Gain	—	—	—	—
Calibration	2	Data	10	I3	CC Offset	—	—	—	—
Calibration	2	Data	17	I4	CC Count	—	—	—	—
Calibration	2	Data	19	U1	CC Time	0	255	180	s
Security	31	Codes	0	H4	Unseal Key 0	0x00000000	0xffffffff	0x28804288	—
Security	31	Codes	8	H4	Unseal Key 1	0x00000000	0xffffffff	0x28751690	—
Security	31	Codes	4	H4	Full Access Key 0	0x00000000	0xffffffff	0xffffffff	—
Security	31	Codes	12	H4	Full Access Key 1	0x00000000	0xffffffff	0xffffffff	—

Note: (1) Encoded battery profile information created by HY4145EV software.

12. Detailed Description

Manufacturer Information Blocks

The HY4145 contains 96 bytes of user programmable Data Flash storage: Manufacturer Info Block A, Manufacturer Info Block B, Manufacturer Info Block C. The method for accessing these memory locations is slightly different, depending on whether the device is in FULL ACCESS, UNSEALED, or SEALED mode.

Access Modes

The HY4145 provides three security modes (FULL ACCESS, UNSEALED, and SEALED) that control Data Flash access permissions according to Table 5. Data Flash locations, specified in Table 4, are accessible to user. Manufacturer information refers to the three reserved 32–byte blocks.

Table 5. Data Flash Access

SECURITY MODE	DATA FLASH ACCESS	MANUFACTURER INFORMATION	KEY ACCESS
FULL ACCESS	R/W	R/W	R/W
UNSEALED ACCESS	R/W	R/W	R
SEALED ACCESS	NONE	R (A); R/W (B, C)	NONE

Only the FULL ACCESS mode allows the HY4145 to write the access–mode transition keys: Full Access Key and Unseal Key.

Battery Parameter Measurement

The HY4145 uses two sets of ADCs to make voltage, temperature and current measurements. Measurement sequence repeats continuously while the HY4145 is in NORMAL mode. All measured results can be accessed via I^2C interface.

Voltage Measurement

The battery voltage is measured across the positive and negative terminals of battery pack periodically. The values are updated within 1 second.

Temperature Measurement

The HY4145 uses the integrated temperature sensor and an external thermistor network to measure temperature. The values are updated within 1 second. Characteristics of the external thermistor can be programmed into Data Flash. Depending on the setting of *[TEMPS]* bit in *Operation Cfg A()* register, the device will use the selected temperature measurement for capacity estimate.

With the set PRES bit in *Operation Cfg A()* register, the external thermistor can be selected with high side connection to VCC. With the cleared PRES bit in *Operation Cfg A()* register, the external thermistor can be selected with low side connection to VSS, or low side connection to the negative terminal of the battery cell if the HY4145 is used at system side.

Current Measurement

The HY4145 continually measures the current flow into and out of battery by measuring the voltage drop across a low value, approximately 10mΩ, current sense resistor, R_{SNS}. The voltage sense range between the SRP and SRN pins is ±125mV with a resolution of 1mA. The HY4145 detects charge activity when $V_{SR} = V_{SRP} – V_{SRN}$ is positive, and discharge activity when $V_{SR} = V_{SRP} – V_{SRN}$ is negative. The values are updated within 1 second.

Charge and Discharge Coulomb Counting

The HY4145 continuously integrates the current measurements over time, using an internal counter.

Power Modes

The HY4145 has four power modes: NORMAL, SLEEP, FULLSLEEP, and HIBERNATE. In NORMAL mode, the HY4145 is fully powered and executes any allowable task. Otherwise, the HY4145 operates in other power saving modes, if the battery voltage is above the Power–On–Reset (POR) threshold voltage.

Shutdown Enable (SE Pin)

The SE pin indicates empty battery situation. The feature is useful to shutdown any device in a deeply discharged battery to protect the battery. **The SE pin MUST be floating if not used.** Note that the SE pin can not be used as the shutdown feature during Power–On–Reset (POR).

The following bits are use to configure and control SE pin:

- One *Operation Cfg A()* bit, also stored in Data Flash, enables or disables the shutdown functionality.

- SE_EN bit: If set, enable the shutdown functionality, and the SE pin is active. Default is 1.

- Two *Control*() subcommands enable or disable the shutdown functionality if SE_EN bit is 0 in *OperationCfgA()*.
  - *SetShutdown()* (0x0013): Enable the shutdown functionality, activate the SE pin, and set the SHUTDOWN bit *ControlStatus()*.
  - *ClearShutdown()* (0x0014): Disable the shutdown functionality, pull the SE pin down, and clear the SHUTDOWN bit in *ControlStatus()*.
- Two *ControlStatus()* bits indicate the status on SE pin.
  - SE (default = 0): If set, the SE pin is active by SE_EN bit in *OperationCfgA()*.
  - SHUTDOWN (default = 0): If set, the shutdown functionality is enabled by the *SetShutdown()* subcommand.
- One *OperationCfgA()* bit, also stored in Data Flash, control the polarity of the SE pin, ALTC pin, and ALTD pin.
  - SE_POL (default = 0): If reset, the SE pin is high to indicate empty battery (*RemainingCapacity()* = 0). If set, the SE pin are low to indicate empty battery (*RemainingCapacity()* = 0). If reset, the ALTC pin and ALTD pin are high to indicate alert events. If set, the ALTC pin and ALTD pin are to indicate alert events.

Voltage, Current, and Temperature Protection (ALTC Pin, ALTD Pin)

When 2-Wire communication is in use, the ALTC pin and ALTD pin can be used to indicate fault conditions. The ALTC pin indicates the voltage, current, and temperature protection events if the device is operating under a fault situation during charge. The ALTD pin indicates the voltage, current, and temperature protection events if the device is operating under a fault situation during discharge. The features are useful to shutdown any device operating under a fault situation. **The ALTD pin MUST be floating if not used. The ALTD pin MUST connect to VSS or VCC if not used.** Note that the ALTD pin and ALTC pin can not indicate the protection events and used as the shutdown feature during Power–On–Reset (POR).

The following bits are use to configure and control ALTC pin and ALTD pin:

- One *OperationCfgA()* bit, also stored in Data Flash, enables or disables the shutdown functionality.

- ALT_EN bit: If set, enable the alert functionality, the ALTC pin and ALTD pin is active. If cleared, enable the shutdown functionality, the ALTC pin and ALTD pin is disabled. Default is 0.

When 1-Wire communication is in use, the ALTC pin and ALTD pin can be used to indicate fault conditions. The ALTD pin indicates the voltage, current, and temperature protection events if the device is operating under a fault situation during discharge. The ALTC pin indicates the voltage, current, and temperature protection events if the device is operating under a fault situation during charge. The features are useful to shutdown any device operating under a fault situation. Note that the ALTC pin and ALTD pin can not indicate the protection events and used as the shutdown feature during Power–On–Reset (POR).

Battery Pack Removed and Battery Insertion Detection (BI Pin)

The HY4145 can be installed at system side with battery insertion feature ready for use as described as below.

Removable Battery Setting ([NR] = 0): If the [NR] bit in *Operation Cfg A()* register is cleared, the [BAT_DET] in *Flag()* register is always set.

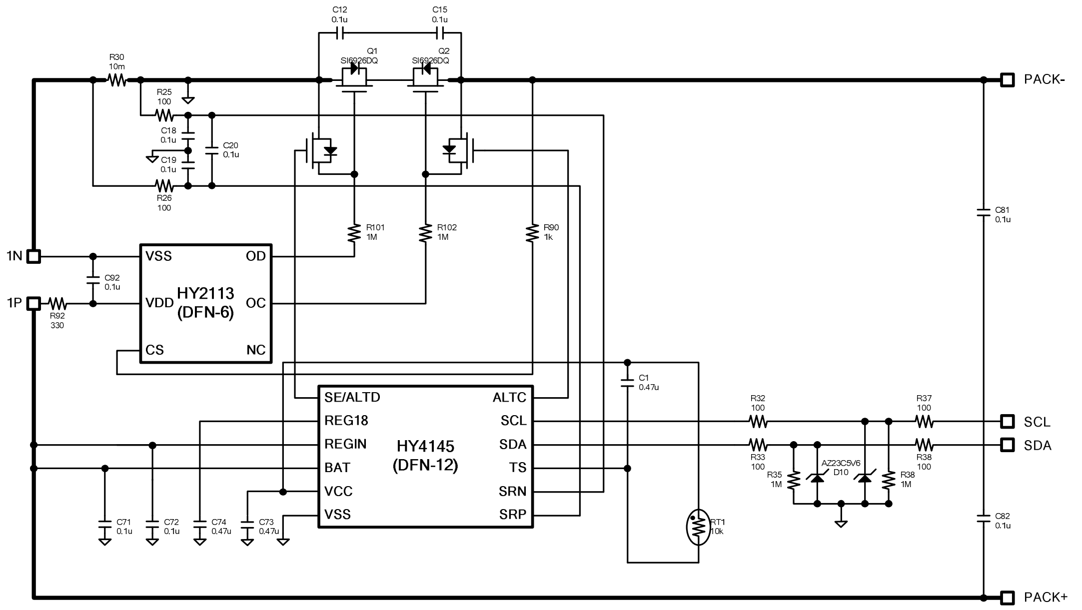
Non-removable Battery Setting ([NR] = 1): If the [NR] bit in *Operation Cfg A()* register is set and the external thermistor is connected, the [BAT_DET] in *Flag()* register is set. Otherwise, the [BAT_DET] is cleared. When the battery is inserted and detected immediately under Normal mode, the HY4145 will reset automatically. When the battery is inserted and detected periodically under Sleep mode, the HY4145 will reset automatically.

13. One-wire Enhanced Universal Asynchronous Receiver Transmitter

Enhanced Universal Asynchronous Receiver Transmitter, EUARTX, peripheral is usually called serial communications interface or SCI. It can be configured as a half-duplex synchronous system, which can communicate with peripheral devices, with an internal open-drain pull-down and an external resistive pull-up.

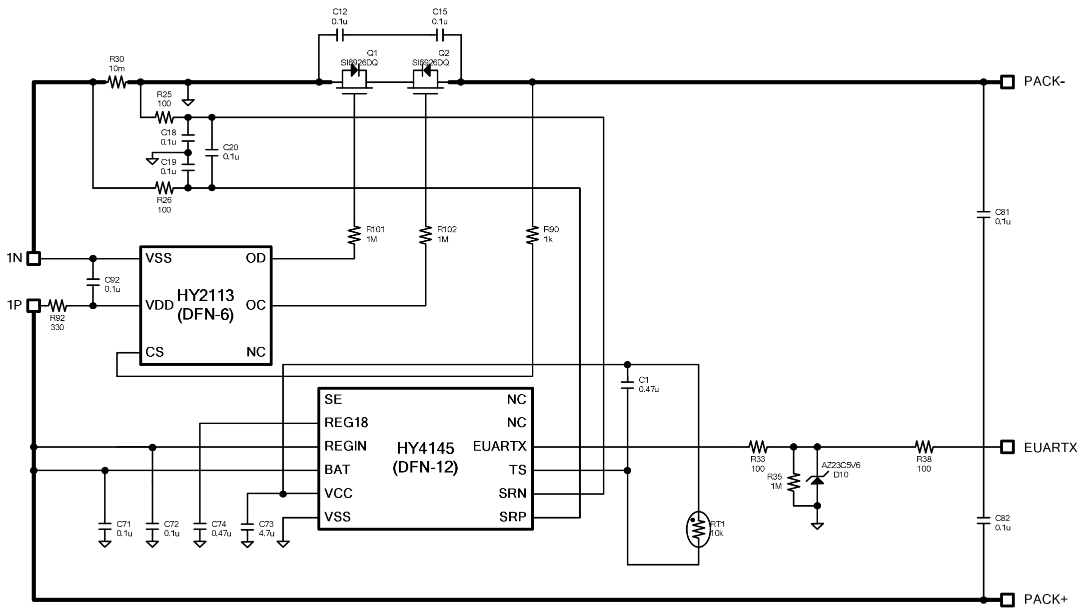
14. Operation Example

2-Wire Communication (Pack-side):



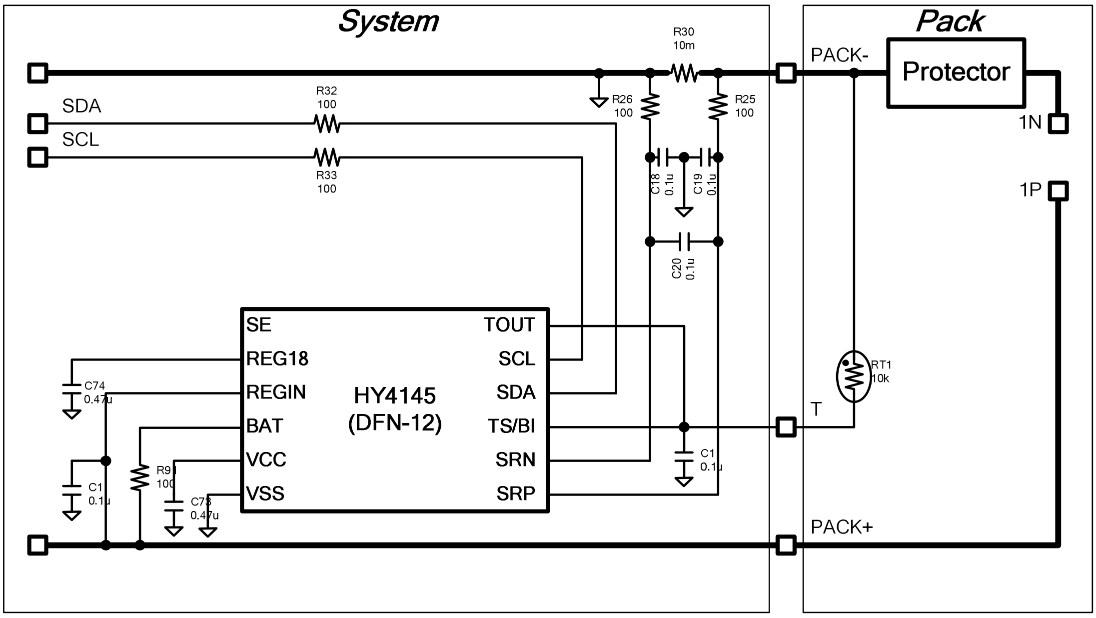
Note:
1. Pin 11 to be SCL as default, and can be programmed as NC.
2. Pin 10 to be SDA as default, and can be programmed as EUARTX.
3. Pin 12 can not stay floating, and must connected to VSS or VCC.

1-Wire Communication (Pack-side):

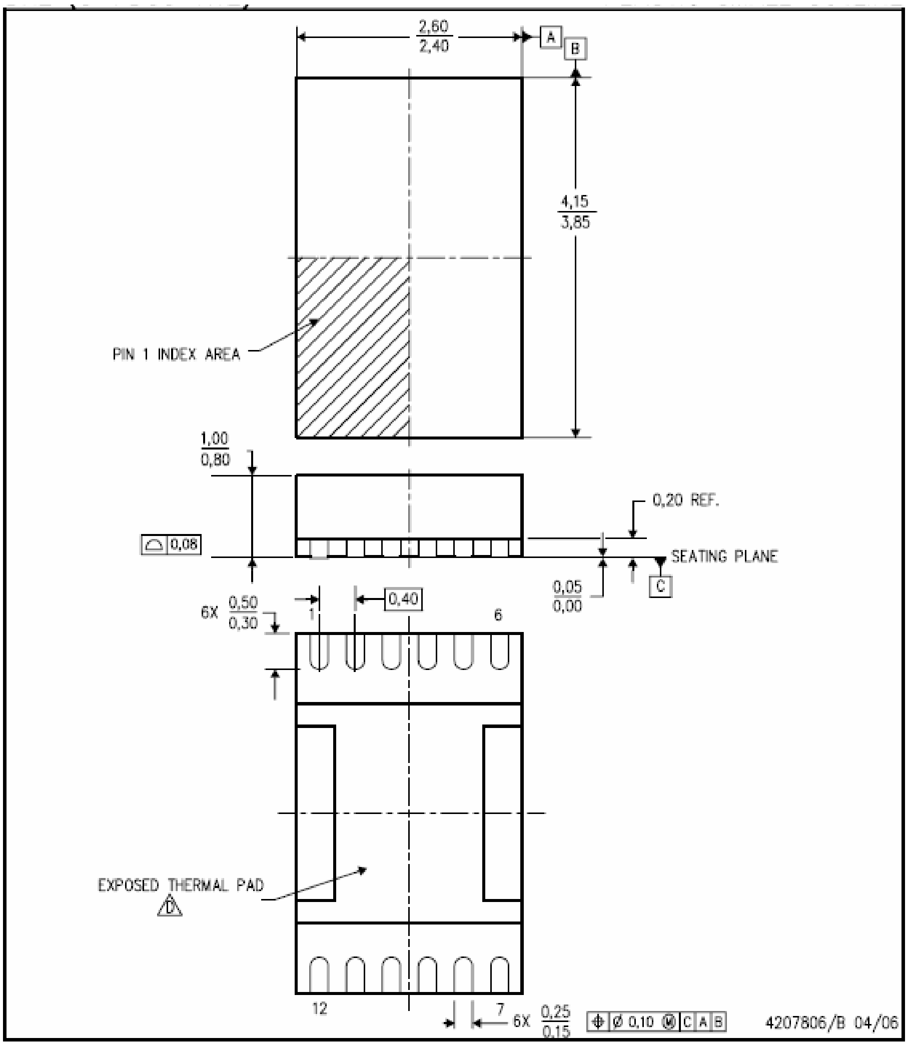


Note:
1. Pin 11 to be SCL as default, and can be programmed as NC.
2. Pin 10 to be SDA as default, and can be programmed as EUARTX.
3. Pin 12 can not stay floating, and must connected to VSS or VCC.

2-Wire Communication (System-side):


System
Pack
R30
10m
PACK-
Protector
1N
1P
SDA
SCL
R32
100
R33
100
R26
100
R25
100
C18
0.1u
C19
0.1u
C20
0.1u
SE
REG18
REGIN
BAT
VCC
VSS
HY4145
(DFN-12)
TOUT
SCL
SDA
TS/BI
SRN
SRP
C74
RT1
10k
T
PACK+

15. Package Information



16. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
1.0	32	New
2.0	35	Updated from 1.0
2.1	38	Updated from 2.0