Small-Signal Analysis of the Phase-Shifted PWM Converter

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***Abstract*—The specific circuit effects in the phase-shifted pulse-width-modulated (PS-PWM) converter and their impact on the converter dynamics are analyzed. The small-signal model is derived incorporating the effects of phase-shift control and the utilization of transformer leakage inductance and power FET junction capacitances to achieve zero-voltage resonant switching. The paper explains the differences in the dynamic characteristics of the PS-PWM converter and its PWM counterpart. Model predictions are confirmed by experimental measurements.**

I. Introduction

In recent years, the phase-shifted pulse-width-modulated (PS-PWM) converter has found many applications due to its distinct characteristics [1]–[4]. This topology permits all switching devices to operate under zero-voltage switching (ZVS) by using circuit parasitics such as leakage inductance and power FET junction capacitance to achieve resonant switching. The ZVS allows operation with much reduced switching losses and stresses, and eliminates the need for primary snubbers. It enables high switching frequency operation for improved power density with good conversion efficiency. The circuit appears similar to a conventional PWM buck topology, but its small-signal properties are significantly different from those of the PWM buck converter's. This is due to the phase-shift operation and the presence of a large leakage inductance in the primary of the transformer.

In this paper, the small-signal analysis of the PS-PWM converter is performed by modeling the effects introduced by the phase-shift operation and the use of the transformer leakage inductance to resonate with the junction capacitances of the power FET's to achieve ZVS. A new small-signal model is developed by modifying the small-signal circuit model of its PWM counterpart [6]. The transfer functions of the power stage are compared to the corresponding transfer functions of its PWM counterpart to show the significant differences between them. Experimental results are presented to verify the accuracy of the model.

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II. Operation of the PS-PWM Converter

To achieve ZVS, the two legs of the bridge are operated with a phase shift. This operation allows a resonant discharge of the output capacitances of the MOSFET's, and subsequently, forces the conduction of each MOSFET's antiparallel diode prior to the conduction of the MOSFET. Because the operation of the circuit has been described in detail [1]–[5], only the circuit operation is emphasized, which is significant for development of the small-signal model. Fig. 1 shows the converter topology and the waveforms for the current I and voltage V_{AB} in the primary and the voltage across the secondary of the power transformer V_s. In examining these waveforms, it should be noted that the leakage inductance L_{lk} does not have to be minimized for the proper operation of the converter. In fact, the load range at which the converter operates with ZVS increases with the leakage inductance. However, the large leakage inductance dictates the slope of the current when voltage is applied to the primary (t_2 or t_6). This finite slope reduces the duty cycle of the secondary voltage D_{eff} and has a significant impact on the dynamic characteristics of the converter.

The duty cycle of the secondary voltage can be expressed as

$$D_{\text{eff}} = D - \Delta D \tag{1}$$

where D is the duty cycle of the primary voltage set by the control, and ΔD is the loss of duty cycle due to the finite slope of the rising and falling edges of the primary current. Examining Fig. 1, ΔD can be expressed as [5]

$$\Delta D = \frac{I_1 + I_2}{\frac{V_{\text{in}}}{L_{lk}} \cdot \frac{T_s}{2}} \tag{2}$$

$$\Delta D = \frac{n}{\frac{V_{\text{in}}}{L_{lk}} \frac{T_s}{2}} \left(2I_L - \frac{V_{\text{out}}}{L} (1 - D) \frac{T_s}{2} \right) \tag{3}$$

where n is the transformer turns ratio, $n = N_s/N_p$, V_{in} and V_{out} are input and output voltages, respectively, T_s is the switching period, I_L is the output filter inductor current, and L is the output filter inductance.

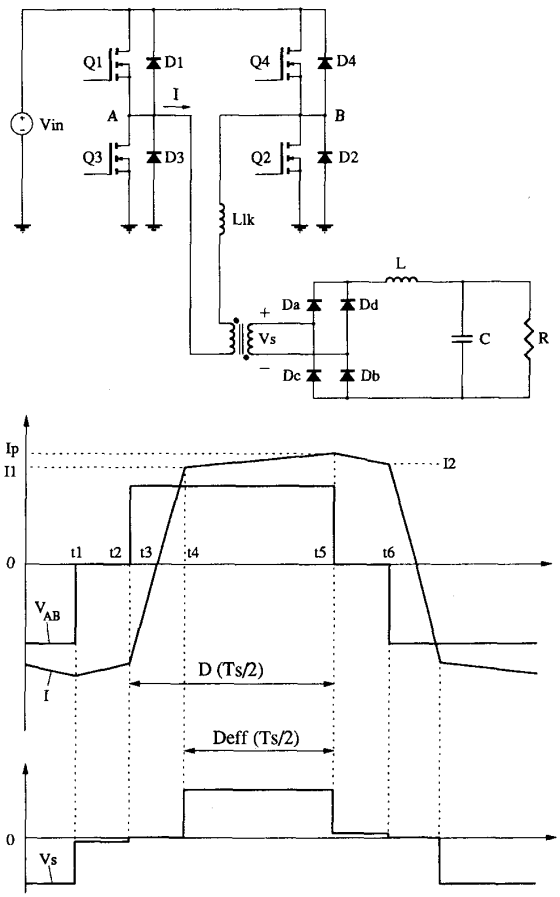

Fig. 1. PS-PWM converter: Scheme and circuit waveforms.

III. Method of Analysis

One way of performing the small-signal analysis of the PS-PWM converter would be to apply state-space averaging. Doing this would, however, be a tedious job, because it would require solving the third-order system composed of six systems of equations (corresponding to six topological stages of the converter) whose averaging factors are implicit functions of the states.

The analysis presented in this paper uses the fact that the PS-PWM converter is a buck-derived topology. It can be seen from the description of the circuit operation that the effective duty cycle, $d_{\text{eff}} = D_{\text{eff}} + \hat{d}_{\text{eff}}$, of the transformer secondary voltage depends not only on the duty cycle d of the primary voltage but also on the output filter inductor current i_L, the leakage inductance L_{lk}, the input voltage, v_{in}, and the switching frequency f_s. This can be concluded by examining (3). The small-signal transfer functions of this converter, therefore, will depend on L_{lk}, f_s, and the perturbations of the filter inductor current $\hat{i}_L$, input voltage, $\hat{v}_{\text{in}}$, and duty cycle of the primary voltage $\hat{d}$.

To accurately model the dynamic behavior of this converter, it is necessary to find out the contributions of L_{lk}, f_s, $\hat{i}_L$, $\hat{v}_{\text{in}}$, and $\hat{d}$ to $\hat{d}_{\text{eff}}$. These effects can be incorporated into the small-signal circuit model of the PWM buck converter (Fig. 4) to obtain the model for the PS-PWM converter.

IV. Specific Circuit Effects

A. Duty Cycle Modulation Due to the Change of the Filter Inductor Current

Fig. 2 illustrates the effect of duty cycle modulation due to the change of the filter inductor current. When the steady-state operation (solid lines) is perturbed by an increase of the filter inductor current by the amount $\hat{i}_L$, the primary current will follow the dashed line and reach the reflected filter inductor current at a later time than it would in the steady-state operation. This will cause a reduction of the duty cycle of v_s.

The additional delay in increase of the secondary voltage due to $\hat{i}_L$ can be calculated using Fig. 3 as follows:

$$\Delta t = 2n\hat{i}_L \frac{L_{lk}}{V_{\text{in}}}. \tag{4}$$

The change of d_{eff} due to this effect, denoted as $\hat{d}_i$, is

$$\hat{d}_i = -\frac{\Delta t}{(T_s/2)} = -\frac{4nL_{lk}f_s}{V_{\text{in}}}\hat{i}_L \tag{5}$$

or

$$\hat{d}_i = -\frac{R_d}{nV_{\text{in}}}\hat{i}_L \tag{6}$$

where $R_d = 4n^2 L_{lk} f_s$. The negative sign shows that there will be a reduction in d_{eff} if the filter inductor current is increased. This effect is equivalent to a current feedback. It will be shown shortly that it will introduce additional damping to the system and make the output impedance finite at low frequencies. Note that the duty cycle of the primary voltage has been kept constant.

B. Duty Cycle Modulation Due to the Change of the Input Voltage

Fig. 3 illustrates the effect of duty cycle modulation due to the change of the input voltage. When the steady-state operation (solid lines) is perturbed by an increase of the input voltage by the amount $\hat{v}_{\text{in}}$, the slope of the primary current will increase (dashed line) so that it will reach the reflected filter inductor current sooner than it would in the unperturbed operation. This will cause an increase of the duty cycle of v_s.

Examining Fig. 3, the change of d_{eff} as a function of $\hat{v}_{\text{in}}$ can be calculated as follows:

$$\Delta t = n\left(2I_L - \frac{V_{\text{out}}}{L}D'\frac{T_s}{2}\right)\left(\frac{L_{lk}}{V_{\text{in}}} - \frac{L_{lk}}{V_{\text{in}} + \hat{v}_{\text{in}}}\right) \tag{7}$$

where $D' = (1 - D)$.

$$\Delta t = n\left(2I_L - \frac{V_{\text{out}}}{L}D'\frac{T_s}{2}\right)\frac{L_{lk}}{V_{\text{in}}(V_{\text{in}} + \hat{v}_{\text{in}})}\hat{v}_{\text{in}}. \tag{8}$$

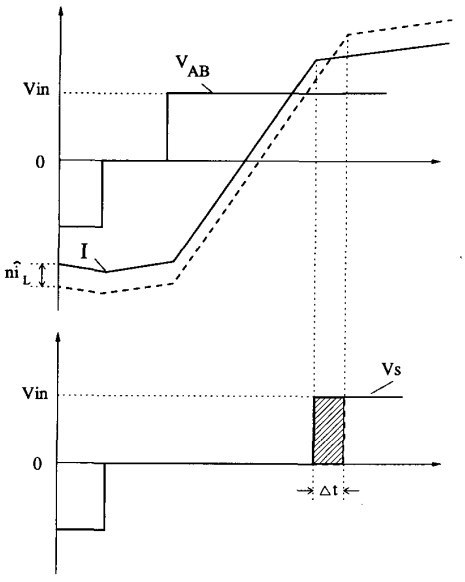

Fig. 2. Duty cycle modulation due to the change of filter inductor current.

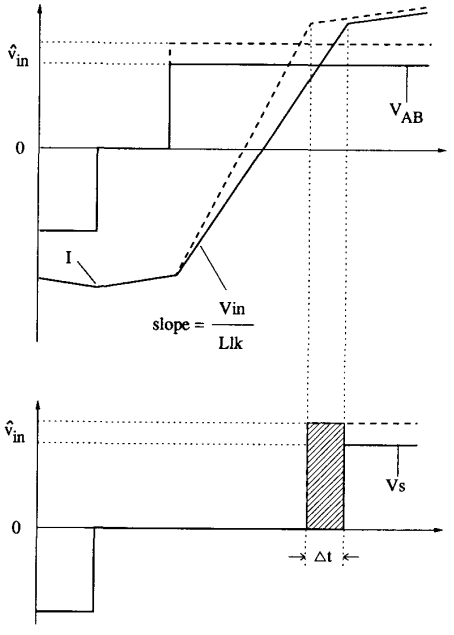

Fig. 3. Duty cycle modulation due to the change of input voltage.

Under a small-signal assumption, this becomes:

$$\Delta t = n\left(2I_L - \frac{V_{out}}{L} D' \frac{T_s}{2}\right) \frac{L_{lk}}{V_{in}^2} \hat{v}_{in}. \quad (9)$$

The change of d_{eff} caused by this effect, denoted as $\hat{d}_v$, is

$$\hat{d}_v = \frac{\Delta t}{(T_s/2)} = \left(I_L - \frac{V_{out}}{L} D' \frac{T_s}{4}\right) \frac{4nL_{lk}f_s}{V_{in}^2} \hat{v}_{in}. \quad (10)$$

In order to minimize the conduction losses due to the circulating currents in the primary of the converter, D' is always made as small as possible [5]. Because of this, the term containing D' is justifiably neglected when the converter operates in deep continuous conduction mode. This gives the following expression for $\hat{d}_v$:

$$\hat{d}_v = \frac{4nL_{lk}f_sI_L}{V_{in}^2} \hat{v}_{in} \quad (11)$$

or

$$\hat{d}_v = \frac{R_dI_L}{nV_{in}^2} \hat{v}_{in}. \quad (12)$$

When the converter operates close to discontinuous conduction mode, (10) should be used for $\hat{d}_v$.

This effect can be interpreted as an additional feedforward of input voltage, and it will increase the audio susceptability of this converter. Again, there was no change in duty cycle of v_{AB}.

V. Small-Signal Model

The results of the previous analysis can now be incorporated into the averaged small-signal circuit model of the PWM buck converter. This can be done by replacing $\hat{d}$ in the buck converter model (Fig. 4) by the total change of d_{eff}, which is

$$\hat{d}_{eff} = \hat{d} + \hat{d}_i + \hat{d}_v. \quad (13)$$

The new model is shown in Fig. 5. The contribution of $\hat{d}_i$ and $\hat{d}_v$ is represented by two controlled sources and the contribution of $\hat{d}$ by two independent sources. This is to emphasize that $\hat{d}_i$ and $\hat{d}_v$ originate from the circuit itself (i.e., perturbations of i_L and v_{in}) and are not controlled by the control circuit. Close examination of (5) and (10) shows that the circuit model of the buck converter is a special case of the PS-PWM converter model. This can be concluded by making $L_{lk} = 0$, which gives $\hat{d}_i = \hat{d}_v = 0$. Transfer functions of the PS-PWM power stage can now be derived using the new model and (6) and (10). For simplicity, the following derivations use (12) for $\hat{d}_v$.

VI. Small-Signal Characteristics of the Power Stage

In this section expressions for the transfer functions of the power stage are given that can be easily incorporated into mathematical programs such as MathCAD or CC to facilitate the control circuit design. These transfer functions are compared to the corresponding transfer functions of the PWM buck converter having the same circuit elements except L_{lk}, which is assumed to be equal to zero. For simplified notation, the following definitions, referring to Fig. 5, are used.

Transfer function of the output filter is

$$H_o \equiv \frac{1}{\Delta f} = \frac{1}{s^2LC + s\frac{L}{R} + 1}. \quad (14)$$

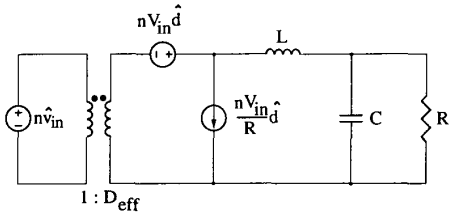

Fig. 4. Small-signal circuit model of the buck converter.

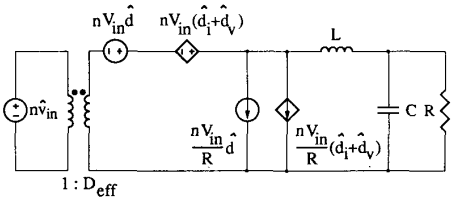

Fig. 5. Small-signal circuit model of the PS-PWM converter.

Input impedance of the output filter is

$$Z_f \equiv \frac{R\Delta_f}{1 + sRC}. \tag{15}$$

Output impedance of the output filter is

$$Z_n \equiv \frac{sL}{\Delta_f}. \tag{16}$$

The circuit parameter values used to plot the transfer functions are

Input voltage, V_{in}	=	600 V
Output voltage, V_{out}	=	360 V
Transformer turns ratio, n	=	1
Transformer leakage inductance, L_{lk}	=	52 μH
Switching frequency, f_s	=	100 kHz
Output filter inductor, L	=	315 μH
Output flter capacitor, C	=	5 μF
Load resistor, R	=	70 Ω

A. Control-to-Output Transfer Function

The control-to-output transfer function is

$$G_{vd} = H_o n V_{\text{in}} \frac{Z_f}{Z_f + R_d}. \tag{17}$$

Fig. 6 shows the control-to-output transfer functions of the PWM buck converter (dashed lines) and of the PS-PWM converter (solid lines). The differences between the transfer functions in dc gain and resonant peaking are apparent.

To gain insight on how the transformer leakage influences the power stage transfer function, the expressions for Z_f and H_o can be substituted into (17):

$$G_{vd} = \frac{nV_{\text{in}}}{s^2LC + s\left(\frac{L}{R} + R_dC\right) + \frac{R_d}{R} + 1}. \tag{18}$$

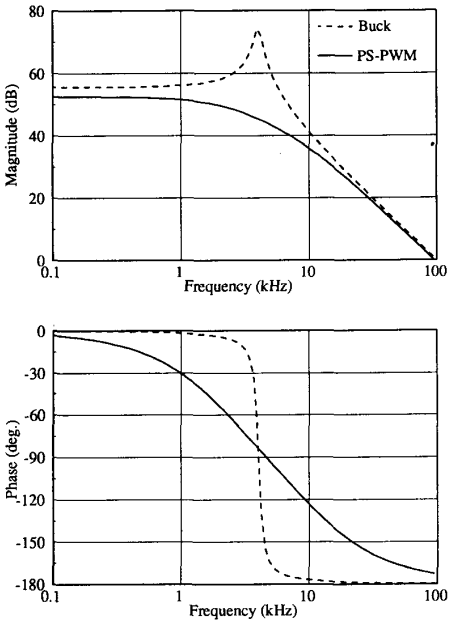

Fig. 6. Control-to-output voltage transfer functions of the buck (dashed lines) and of the PS-PWM converters (solid lines).

It can be observed from this equation that the "built-in" current feedback decreases the low frequency value of G_{vd}. This is caused by the presence of the term R_d/R. In practice, the value of this term ranges from 0 to around 0.5, with a typical value of 0.25. The upper boundary of this interval is determined by the loss of steady-state duty cycle (3), which, in practice, must be kept below a reasonable value [6]. For the purpose of further qualitative analysis, it can be assumed that $(R_d/R) + 1 \simeq 1$. After the numerator and denominator are multiplied by $1/LC = \omega_o^2$ we obtain:

$$G_{vd} \simeq \frac{nV_{\text{in}}\omega_o^2}{s^2 + s\left(\frac{1}{RC} + \frac{R_d}{L}\right) + \omega_o^2} \tag{19}$$

$$= \frac{nV_{\text{in}}\omega_o^2}{s^2 + s2\omega_o\xi + \omega_o^2} \tag{20}$$

where ξ is the damping of the second-order denominator:

$$\xi = \frac{1}{2R}\sqrt{\frac{L}{C}} + \frac{R_d}{2}\sqrt{\frac{C}{L}}. \tag{21}$$

The first term of ξ is the damping in the regular buck converter. The use of leakage inductance introduces additional damping, and the second term of ξ can become dominant. Fig. 7 shows the family of control-to-output transfer functions of the PS-PWM power stage as the ratio R_d/R varies from 0 to 0.5. The damping of the system is noticeably affected even for very small values of R_d/R.

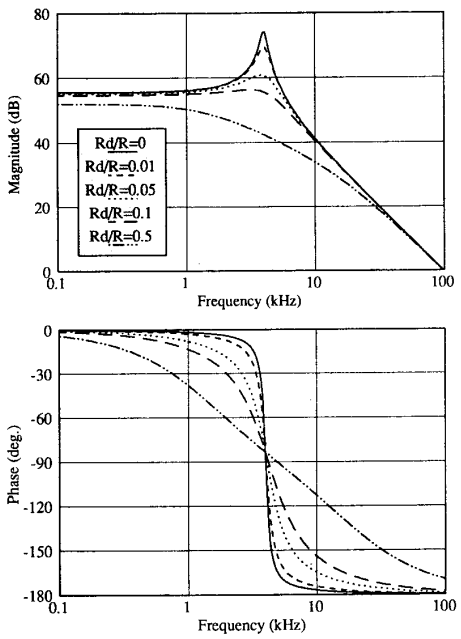

Fig. 7. Control-to-output transfer functions for different values of Rd/R.

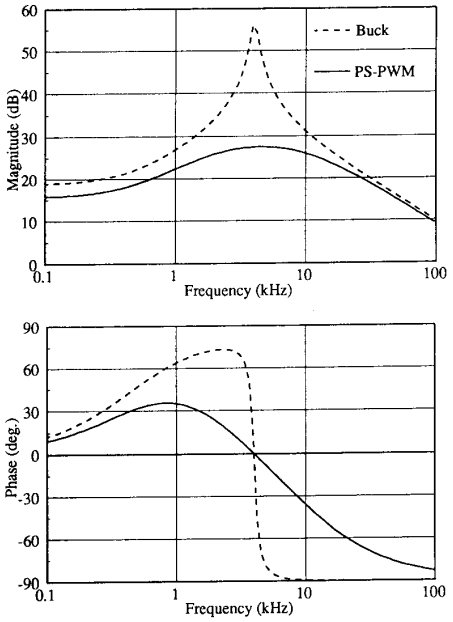

Fig. 8. Control-to-filter inductor current transfer functions of the buck (dashed lines) and PS-PWM converters (solid lines).

B. Control-to-Filter Inductor Current Transfer Function

The control-to-filter inductor current transfer function is

$$G_{id} = \frac{nV_{\text{in}}}{Z_f + R_d}. \tag{22}$$

Fig. 8 shows the control-to-filter inductor current transfer functions of the PWM buck converter (dashed lines) and of the PS-PWM converter (solid lines). The control-to-filter inductor current transfer function is altered in the same way as the control-to-output transfer function.

C. Output Impedance

The output impedance of the PS-PWM power stage is

$$Z_o = Z_n + \frac{H_o^2}{\dfrac{1}{Z_f} + \dfrac{1}{R_d}}. \tag{23}$$

Fig. 9 shows the output impedances of the PWM buck converter (dashed lines) and of the PS-PWM converter (solid lines). It can be observed that the output impedance of the PS-PWM converter is not attenuated at low frequencies. Such behavior is expected knowing that the loss of duty cycle (3) is a function of output current, i.e., the dc output voltage is a function of the dc load current.

D. Audio Susceptibility

The audio susceptibility of the PS-PWM power stage is

$$G_{vg} = H_o n D_{\text{eff}} \left(1 + \frac{R_d}{R}\frac{Z_f - R}{Z_f + R_d}\right). \tag{24}$$

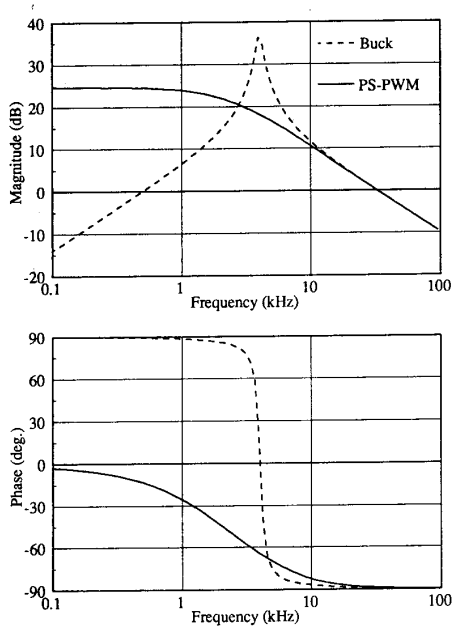

Fig. 9. Output impedances of the buck (dashed lines) and PS-PWM converters (solid lines).

Fig. 10 shows the audio susceptibilities of the PWM buck converter (dashed lines) and the PS-PWM converter (solid lines). By examining (12) one could expect the audio susceptibility of the PS-PWM converter power stage to be higher than the audio susceptibility of the buck converter. Fig. 10, however, shows that this is the case only at higher frequencies. The explanation can be found by

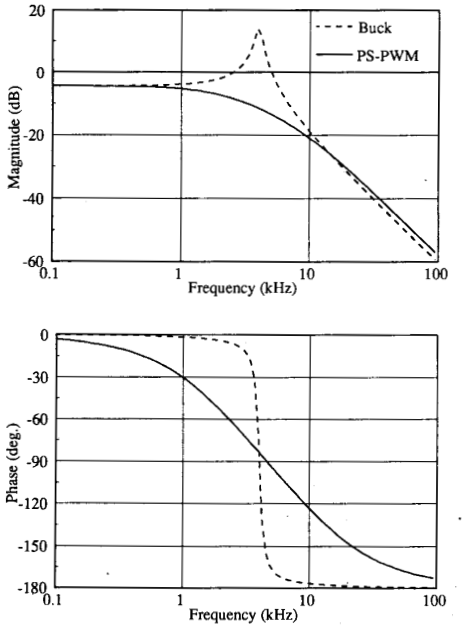

Fig. 10. Audio susceptibilities of the buck (dashed lines), and PS-PWM converters (solid lines).

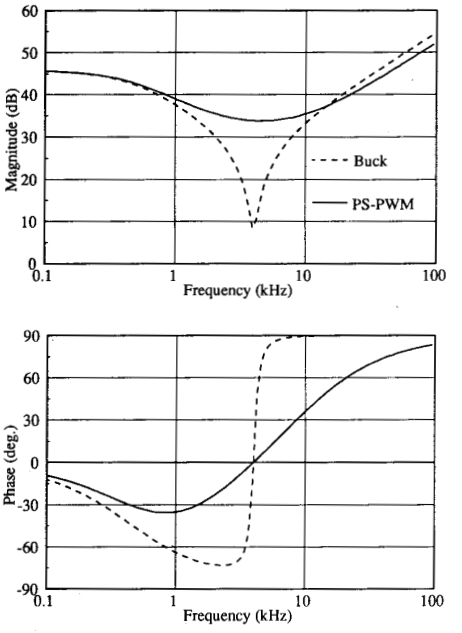

Fig. 11. Input impedance of the buck (dashed lines) and PS-PWM converters (solid lines).

examining (24). The second term inside the brackets does not exist in the PWM buck converter, and it is introduced by the use of L_{lk}. At low frequencies, $Z_f = R$, and the second term is equal to zero. This leads to the conclusion that the effect of $\hat{d}_v$ is neutralized by the influence of $\hat{d}_i$ at low frequencies.

E. Input Impedance

The input impedance of the PS-PWM power stage is

$$Z_{\text{in}} = \frac{Z_f + R_d}{n^2 D_{\text{eff}}^2 \left(1 + \dfrac{R_d}{R}\right)}. \tag{25}$$

Fig. 11 shows the input impedances of the PWM buck converter (dashed lines) and the PS-PWM converter (solid lines). As discussed in Section VI-D, the modulation of duty cycle due to the variation of input voltage affects the input impedance only at high frequencies.

VII. Experimental Verification

To verify the results of the analysis, a converter was built with the same component values as shown in Section VI. The only difference is that in order to achieve better measurement accuracy, the input voltage, the output voltage, and the load resistance have been reduced to 50 V, 20 V, and, 50 Ω, respectively.

The control-to-output transfer function is shown in Fig. 12. Both the gain and phase measurements agree very well with predictions. Fig. 13 shows the control-to-filter inductor current transfer function. The agreement between prediction and measurement is again very good. Fig. 14 shows the output impedance of the converter. The measurement clearly shows the first order response and loss of resonant peaking, predicted by analysis.

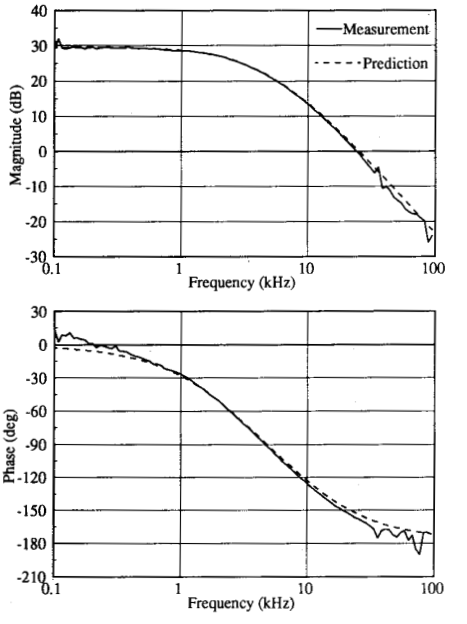

Fig. 12. Control-to-output voltage transfer function of the PS-PWM converter. Model prediction (dashed lines) and experimental measurement (solid lines).

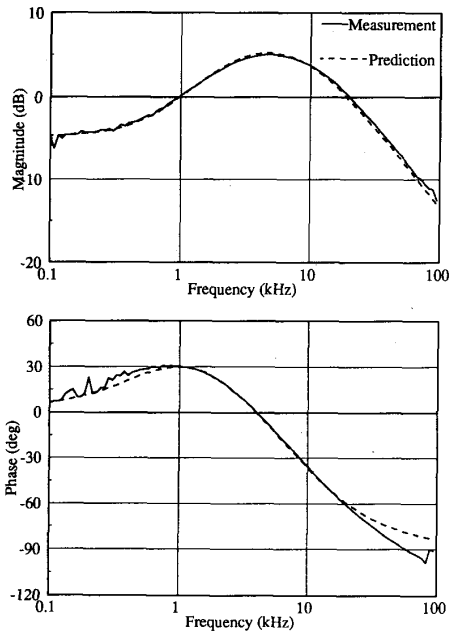

Fig. 13. Control-to-filter inductor current transfer function of the PS-PWM converter. Prediction (dashed lines) and measurement (solid lines).

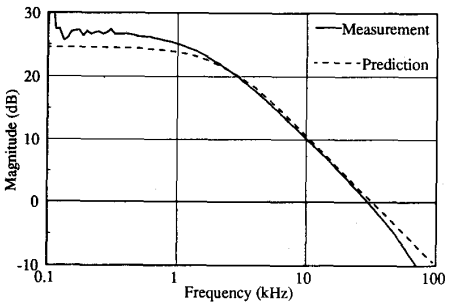

Fig. 14. Output impedance of the PS-PWM converter. Model prediction (dashed lines) and experimental measurement (solid lines).

VIII. Conclusions

The phase-shift operation and the use of the large leakage inductance to achieve ZVS have a significant impact on the dynamics of the PS-PWM converter. The conversion ratio of this converter depends both on duty cycle of the primary voltage determined by the control and on values of load current and input voltage. Due to these effects, the small-signal model of the PWM buck converter is not accurate for the PS-PWM converter.

A new small-signal model of the PS-PWM converter has been described. The effects caused by phase-shift operation and use of large leakage inductance to achieve ZVS have been modeled by introducing additional feedforward and feedback terms for duty cycle modulation. A small-signal circuit model has been developed by adding two controlled sources into the small-signal model of the PWM buck converter. The model accurately predicts the loss of resonant peaking at the resonant frequency of the output filter, the reduction of the low-frequency magnitudes of the control-to-output and control-to-filter inductor current transfer functions, and the transformation of the output impedance nature from inductive to resistive at low frequencies.

The analytical closed-form expressions for the transfer functions of the PS-PWM power stage have been derived. The new model can easily be incorporated into any circuit simulation programs such as SPICE, or into mathematical application program such as CC. The predictions of the new model have been verified by measurements.

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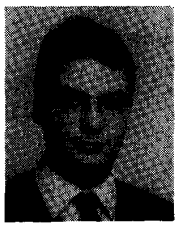

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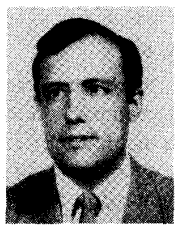

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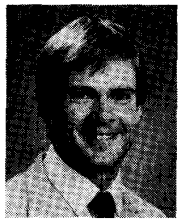
He was a researcher and instructor in the Electronics Department of the Polytechnic University of Catalunya between 1984 and 1986. In 1986 he joined the Virginia Power Electronics Center at Virginia Polytechnic Institute and State University. Currently a research assistant, he is working towards a Ph.D. degree at the Bradley Department of Electrical Engineering. His research interests include resonant power conversion, high-frequency power converters, new converter topologies, and power converters modeling and analysis.



Raymond B. Ridley received the B.S. degree from Boston University, Boston, MA, and the M.S. and Ph.D. degree in electrical engineering from Virginia Polytechnic Institute and State University, in 1981, 1986, and 1990, respectively.

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Fred C. Lee (F'90) received the B.S. degree in electrical engineering from Chen-Kung University in Taiwan and the M.S. and Ph.D. degrees in 1968, 1971, and 1974, respectively.

Dr. Lee is the director of the Virginia Power Electronics Center (VPEC), at Virginia Polytechnic Institute and State University. Under his leadership, VPEC has become one of the largest university power electronics centers in the country. Over 30 graduate students are currently enrolled in the program. The Industrial Partnership Program includes 39 major companies from all over the world.

Dr. Lee and his graduate students invented a new generation of high-frequency power converter devices known as quasi-resonant converters (QRC's) and multiresonant converters (MRC's). By eliminating switching losses and stresses, these converters are capable of operating in the megahertz range with significant improvement in performance and power density. Dr. Lee holds seven patents on QRC/MRC technology with two additional patents pending. During his career he has published over 70 referred journal papers, more than 130 technical papers in national and international conferences, and over 80 industry and government reports. He is a member of the AdCom of IEEE Power Electronics Society, and Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. He was chairman of the 1987 IEEE Power Electronics Specialists Conference.

Dr. Lee received the Society of Automotive Engineering 1985 Ralph R. Teeter Educational Award, the IEEE Power Electronics Society's 1989 William E. Newell Power Electronics Award, the PCIM Award in Leadership in Power Electronics Education, and the 1990 Alumni Award for Research Excellence from VPI&SU.

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Dr. Cho received the 1989 Presidential Young Investigator Award (PYI) from the National Science Foundation. He is a member of IEEE Power Electronics Society, and Tau Beta Pi.