Phase Accuracy of Charge Pump PLL's

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Abstract—**Phase-lock loops using charge pumps are found to have remarkably good potential for accurate phase tracking. The several favorable factors are described and numerical calculations provide examples of typical errors. Inaccuracy as small as fractional microcycles appears to be an attainable goal.**

I. INTRODUCTION

SEQUENTIAL, phase/frequency detectors have become very popular in phase-lock loops (PLL's) in recent years because of their attractive electrical properties and low-cost availability in integrated circuit chips [1]. These devices are implemented with digital logic circuits and typically have three possible logic states at their output terminals. The states are commonly designated U, D, and N (for up, down, and null).

Conversion is needed from logic states into an analog quantity suitable for processing by the loop filter and voltage-controlled oscillator (VCO) of the PLL. A charge pump is a frequently used conversion device. On each cycle of operation, the charge pump delivers to the loop filter a controlled increment of charge that depends upon the phase error. Details of charge pump operation may be found in [2].

Following the publication of [2], the realization has slowly grown that a charge pump PLL is capable of extremely accurate phase tracking of the input signal; accuracies on the order of fractional microcycles appear to be feasible. Such accuracy is not attainable using conventional multiplier-type phase detectors.

This paper examines the factors within the charge pump PLL that contribute to phase error and calculates typical numerical values. Comparisons are made to conventional phase detectors and the superiority of charge pumps is made evident.

Only steady-state phase error is considered; all noise fluctuations are neglected.

II. CHARGE PUMP PRINCIPLES

A charge pump delivers a *pump current* of $\pm I_p$ to the loop filter whenever the phase detector logic state is U or D, and presents an open circuit to the loop filter for logic state N. Polarity of pump current depends upon which of U or D is true, and this state is established by the sign of phase error.

Duration of an *active state* (U or D) is determined by the magnitude of the phase error. Indeed, the state duration t_p is simply the difference in time between switching edges of the reference signal and the VCO. Charge delivered to the loop filter on each cycle is $\pm I_p t_p$. No charge will transfer during the N state.

Manuscript received May 7, 1981; revised April 29, 1982.
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The loop filter takes the form of an impedance function, rather than a transfer function as in a conventional PLL. The simplest filter impedance that provides a second-order PLL consists of a capacitor in series with a resistor. If this impedance is connected from the charge pump output to the ground, we have a passive filter. If the impedance is connected as the feedback network of an operational amplifier, we have an active filter. Circuits are shown in [2].

The simple series RC filter impedance will be assumed tacitly in this paper but other prevalent filter circuits have identically the same phase-accuracy properties. See [2] for further details.

III. PHASE ERRORS

First to be considered is the *static phase error* (or "loop stress") which arises because the signal frequency differs from the free-running frequency of the VCO by an amount $\Delta\omega$ rad/s. It was pointed out in [2] that a charge pump PLL would have identically zero static phase error if there were no resistive loading across the filter capacitor. This zero error is obtained even with a passive filter—an impossible achievement in a conventional PLL.

Any real circuit will impose some resistive loading, designated as R_s. The resulting static phase error θ_v has been shown [2] to be

$$\theta_v = \frac{2\pi\Delta\omega}{I_p K_0 R_s} \quad \text{rad} \tag{1}$$

where K_0 is the gain of the VCO in rad/s·V.

Some numbers can be tried to give additional meaning to (1). Frequency error and VCO gain can vary over enormous limits in different applications so assignment of numbers of these parameters individually is not very useful. However, the ratio $\Delta\omega/K_0$ is the control voltage excursion needed to tune the VCO to the signal frequency. We can assign a reasonable, maximum control voltage excursion of 10 V for our calculation and be confident that few practical oscillators will have a grossly different maximum swing.

Let us further take $I_p = 10$ mA. This value is readily provided from small-scale semiconductors; it is neither so large as to lead to power consumption difficulties nor so small as to introduce small-current problems. It is perhaps a little on the high side, but not impracticably so.

That leaves R_s to be specified. Many operational amplifiers using JFET or MOSFET inputs are specified as having greater than 10^{12} Ω input resistance. These devices presumably could be used as the op amp for an active filter or as a buffer for a passive filter. Such a high resistance probably ought to be regarded as a euphemism for: "the resistance is so high that we

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can't measure it." For the present calculations, 10^{12} Ω will be used as an upper limit.

In physical hardware, it will be necessary to take account of surface leakage on the circuit board (which is a completely unknown quantity) and the insulation resistance of the filter capacitor. The latter varies widely, depending upon quality of the dielectric and operating temperature. Examination of data sheets suggests that 10^3 Ω·F is a low value for good, film-dielectric capacitors.

If the filter capacitor has a capacitance of 1 μF, then the insulation resistance will be taken as 10^9 Ω. Using that value for R_s, we find static phase error from (1) to be only 1 microcycle. A better insulation resistance (quite feasible at moderate temperatures) would yield correspondingly improved phase errors. For $R_s = 10^{12}$ Ω (possibly an optimistic upper limit), the static phase error is calculated as 1 nanocycle.

The comparison with a conventional PLL is instructive. Static phase error is commonly given [1, ch. 4] as

$$\theta_v = \frac{\Delta\omega}{K_d K_0 F(0)} \quad \text{rad} \tag{2}$$

where K_d is the phase detector gain in V/rad and $F(0)$ is the dc gain of the loop filter.

For typical numbers, take K_d = 1 V/rad. This is a good midrange choice, with some phase detectors having substantially smaller gain and others having larger. Once again, take $\Delta\omega/K_0$ = 10 V. Then, to obtain 1 microcycle to 1 nanocycle static phase error requires dc gains $F(0)$ of 1.6×10^6 to 1.6×10^9, respectively. These values are much larger than normally encountered, although not intrinsically impossible to provide. Note, however, that the same performance can be obtained from a charge pump PLL with no dc-gain device whatever.

Another phase error in a charge pump PLL arises from *leakage currents* reaching the loop filter. These leakages can arise in the VCO control port (e.g., leakage of back-biased varactor diodes), from input bias current of an operational amplifier used as a buffer or to form an active filter, or from off-state current leakage in the switches of the charge pump itself. If the total leakage is denoted I_b, then the corresponding phase error is [2]

$$\theta_b = \frac{2\pi I_b}{I_p} \quad \text{rad.} \tag{3}$$

Numerous devices for switches and op amps are available with leakage current on the order of 1 nA, or less. If we take I_b = 1 nA and I_p = 10 mA, (3) predicts 0.1 microcycle for θ_b.

In a conventional PLL, the phase detector acts as a voltage source to the loop filter and we are more concerned with *offset voltages* rather than leakage currents. (In the event that bias current is significant, we multiply it by the resistance through which it flows to convert it to an equivalent voltage.) Designating the offset voltage referred to the phase detector output as v_d, the corresponding phase error is

$$\theta_d = v_d/K_d \quad \text{rad.} \tag{4}$$

Assume, quite optimistically, that v_d = 1 mV along with K_d = 1 V/rad. Then (4) yields $\theta_d = 10^{-3}$ rad = 160 microcycles. Such a small value is extremely difficult to achieve with practical conventional circuits but is many times greater than the error predicted from leakage currents in a charge pump PLL.

Further analysis shows that voltage offsets in a charge pump PLL make no contribution to phase error. For example, consider the offset voltage of an operational amplifier used to form an active filter. The charge pump will deliver charge to the filter capacitor in exactly the amount needed to cancel out the amplifier offset. Once that charge has been dispensed, no further charge is needed to counteract the offset and the charge pump can remain in the null state. Experiments have confirmed that large offsets–sizable fractions of the supply voltages–do not introduce phase error. Therefore, the designer can select an op amp for its bias-current and input-resistance properties and can ignore voltage offsets.

The same arguments apply to other voltage offsets such as semiconductor-junction voltages in the charge pump switches or dielectric absorption in the filter capacitor.

Typical charge pumps might consist of two current sources, appropriately switched to the loop filter upon command of the digital logic in the phase/frequency detector. It is not necessary that these currents be accurately matched to one another. Unequal currents will introduce a peculiar nonlinearity–the loop responds more rapidly in one direction than the other–but no steady phase error is introduced. If conventional phase detectors utilize balanced circuits, the two halves typically must be very closely matched to minimize dc offsets and the resulting steady phase errors.

III. CONCLUSIONS

The analog circuit portions of charge pump PLL's can be designed to introduce only very small, steady phase errors, on the order of fractional microcycles. With such analog accuracy, the dominant phase uncertainties are likely to arise in the digital logic circuits due to logic switching times, input waveform transition times, etc.

Known techniques for designing conventional PLL's yield steady phase errors that are much worse–hundreds of microcycles, or larger.

REFERENCES

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[2] ——, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849–1858, Nov. 1980.

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