Designing High-Power Factor Off-Line Power Supplies

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ABSTRACT

The purpose of this paper is to provide a tutorial on power factor correction topologies and control techniques. The first part of the paper concentrates on identifying the trade-offs between various operating modes. A framework is developed to compare losses and device stresses in the CCM and CRM boost topologies. The second part provides an overview of the main design choices as well as design equations. The power stage and control circuitry design equations are explained and presented.

INTRODUCTION

The use of power factor correction (PFC) circuits has been widely discussed and is generally considered a market requirement for most off-line power supplies.[1, 2, 3] There are many reasons for this. There is a well know European requirement which is documented in IEC-6000-3-2. This specification sets limits on harmonic current for any power supply sold in the European Union (EU). While this specification is only in force in the EU, for power supply manufacturers wanting to sell into the global market, it makes sense for all their supplies to be compliant. Tables 1, 2 and 3 show the IEC harmonic limits for various classifications of equipment.

Class C is lighting equipment, Class D is personal computers and television receivers and Class A is basically everything else.

There are other reasons for wanting to limit harmonic currents, these include being able to use the full rated current from the available power source. For example, if you have a typical 15-A service (single phase 120 V) and your rectifier is 98% efficient with 55% power factor (PF) the maximum load you could power is 970 W. This assumes using 100% of the rated breaker current, which is unlikely. If the PF is improved to 99% the load increases to 1746 W, an increase of almost 80%. This increase in power can be reason enough to employ PFC circuits.

TABLE 1. LIMITS FOR CLASS A EQUIPMENT

Harmonic Order, n	Maximum permissible harmonic current, A
Odd harmonics	
3	2.3
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$	0.15, 15/n
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \le n \le 40$	0.23, 8/n

TABLE 2. LIMITS FOR CLASS C EQUIPMENT

Harmonic Order, n	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency, %
2	2
3	30 X power factor
4	10
7	7
9	5
$11 \le n \le 39$ (odd harmonics only)	3
	0.15, 15/n

TABLE 3. LIMITS FOR CLASS D EQUIPMENT

Harmonic order n	Maximum permissible harmonic current per watt, mA/W	Maximum permissible harmonic current, A
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13≤ n ≤ 39 (odd harmonics only)	3.85/n	see table 1

A typical switching power supply presents a nonlinear load to the power source. The rectifier, capacitor circuit and the resulting current drawn from the line, are shown in Fig. 1. The high peak current drawn form the line is due to the small conduction angle.

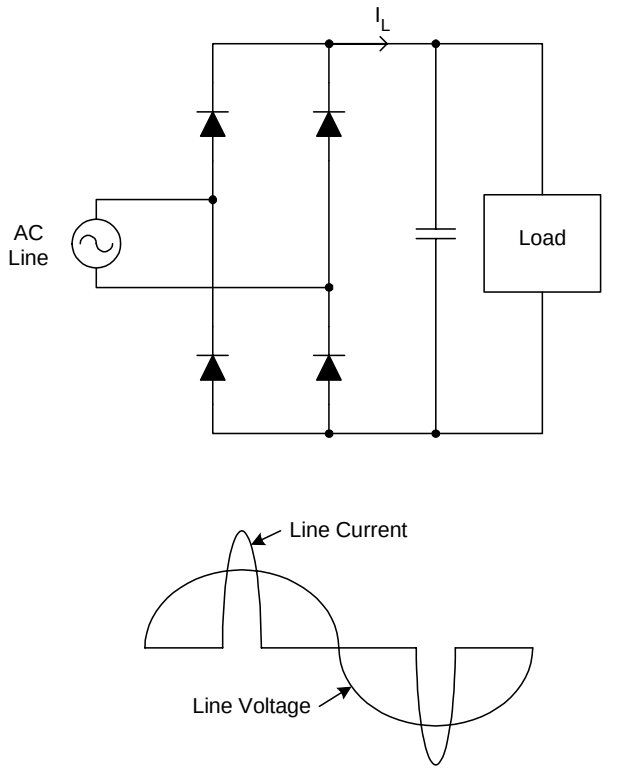


Fig. 1. Simplified rectifier circuit with line voltage and resulting current.

Historically, the definition of power factor (PF) is the cosine of the angle between the voltage and current.

$$PF = \cos(\theta - \phi) \quad (1)$$

Where $(\theta-\phi)$ is the difference in the respective phase angles. This however, is only valid for sinusoidal voltage and current waveforms, i.e. a linear source and load. A more relevant figure of merit for nonlinear systems is to look at the harmonic content of the waveforms.

From Table 1 we can see that the EU specification is indeed given in terms of harmonic current. Power factor is not specified. All of our circuits though are referred to as power factor correction circuits. This is a legacy from the power system and generation part of the industry. Power factor and Total Harmonic Distortion are related mathematically though.

Additionally, it's useful to keep the phase angle definition in mind. Recall that power is only delivered from components of the current and voltage waveforms that are in phase with each other. If the voltage waveform is a pure sinusoid, then it only has a component at its fundamental frequency. The current waveform, if distorted, will have components at multiple frequencies. These components do not contribute to the power delivered; they do however contribute to the RMS value of the current waveform. This increase in RMS current is primarily what we are concerned about.

Total Harmonic Distortion (THD) is the ratio of harmonic current to the fundamental component. Assuming there is no dc offset, the THD is defined as:

$$THD = \sqrt{\frac{\sum_{n\neq 1} I_n^2}{I_1^2}} \quad (2)$$

Power factor and THD are related by the following equation:

$$PF = \sqrt{\frac{1}{1+THD^2}} \quad (3)$$

The goal then of a PFC circuit is to reduce the harmonic content of the current waveform and keep the phase angle between the current and voltage as small as possible. In effect the circuit wants to emulate a resistive load.

This paper is organized into two parts. The first part discusses the different topologies used for PFC circuits. The main focus of Part 1 is the losses in the power stage and specifically the semiconductor components. This should help the designer understand the trade0offs with the different topologies. Part 2 provides design equations and discuss the main design considerations with the boost PFC circuit.

PART I. TOPOLOGY COMPARISON

A. PFC Techniques

There are two classifications of PFC circuits, active and passive. Passive techniques rely on a combination of inductors and capacitors to smooth out the current waveform. The passive approach is usually less expensive than an active approach, but it is hard to optimize for universal line operation and suffers from a large, heavy inductor required to meet the THD requirements. The passive approach is usually a low power, fixed line voltage option.

Active PFC circuits can be derived from all of the basic topologies.[1] There are also topologies that have been developed specifically as PFC circuits.[4, 5, 6] By far though the most popular topology used in PFC applications is the boost converter. This is for obvious reasons. The line voltage varies from zero to some peak value typically in the range of 180 V to 380 V. A buck topology would have a hard time with this input range. The Buck-boost converter has high switch voltage stress and discontinuous conduction mode (DCM) operation (which can provide good PFC in normal operation) has large current stress for the same power level.

The boost converter also has a smooth input current waveform as opposed to the pulsating profile of a buck derived topology, so filtering is much easier. This is not a trivial point since any filtering that is needed on the input side of the converter adds cost and can potentially degrade the PF you are trying to correct.[7]

The boost converter can operate in two modes, continuous conduction mode (CCM) and DCM. Fig. 2 shows example inductor current profiles for the different operating modes. DCM operation has the disadvantage of much higher peak currents than CCM for the same power level. A third option called transition mode or critical conduction mode (CRM) is really just a variation of CCM. The power stage equations and transfer functions are the same as CCM. The difference is a control function, which when implemented forces the inductor current to operate just at the border of CCM and DCM. Since the line voltage is constantly changing in a PFC circuit, the operating frequency will change as well. This is due to the fact that as the line voltage varies, the time needed for the inductor current to decay back to zero will vary accordingly.

The control techniques required to implement the designs will be discussed in a later section. The question arises though, which operating mode is better. The answer in most cases is, it depends.

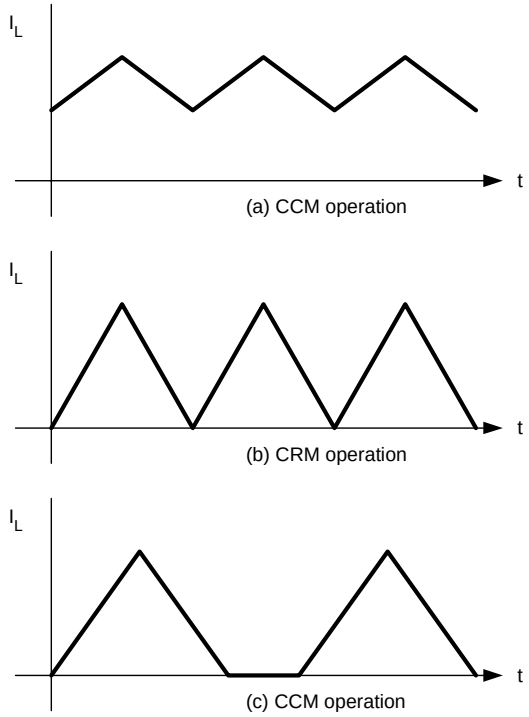


Fig. 2. Three inductor current operating modes.

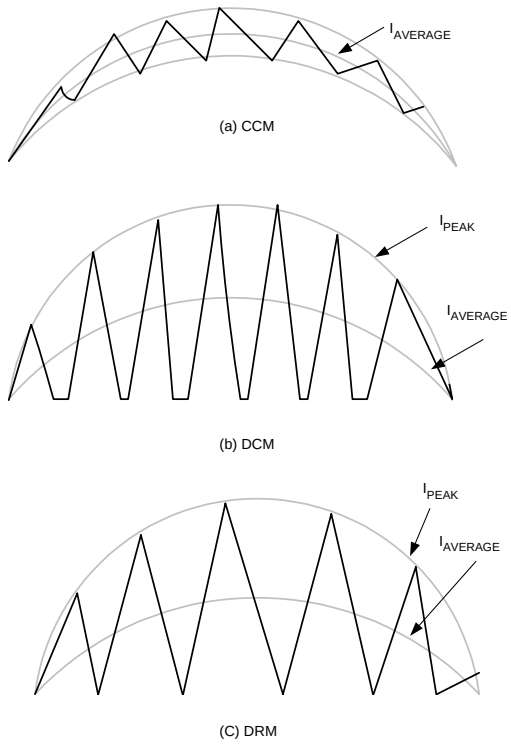


Fig. 3. PFC inductor current profiles.

B. Boost topology comparison

The main differences between the CCM and CRM topologies relate to the amplitude of the current and the ripple profile. The current profile effects two items, power losses in the power stage components and filtering requirements.

The peak current in the CRM boost is twice the amplitude in CCM operation. This leads to higher conduction losses. The peak-to-peak ripple is also twice the average current. This effects switching losses in the MOSFET as well as ac losses in the magnetics. On the other hand, the boost diode losses are much higher in CCM operation. This is due to the big reverse recovery problem.

Qualitatively you can say that for low to medium power applications the CRM boost has an advantage in losses, while the filtering requirement is not so severe as to be a big disadvantage. The CCM boost is a better choice for medium to high power applications. The peak currents are significantly lower which reduces conduction losses while the lower ripple current reduces filter requirements.

To better quantify this we need to take a look at the losses in the main components, which are different in the two modes of operation. For example, the gate charge, and diode turn-on losses are essentially the same in both modes of operation, so these won't be considered.

CCM Losses

First we will consider the losses in the CCM boost converter. In order to do this we should first define the currents in the converter (see Fig. 2 and 3). The input current waveform follows the line voltage. If we allow the ripple in the inductor to be 20% of the peak line current, which is a typical value, then the peak inductor current (IL_pk_ccm) is given by equation (4).

$$IL\_pk\_ccm = \frac{\sqrt{2} \bullet Pin}{VAC} + 0.1 \bullet \frac{\sqrt{2} \bullet Pin}{VAC} \qquad (4)$$

The valley of inductor current (at the crest of the line) is shown in equation (5).

$$IL\_valley\_ccm = \frac{\sqrt{2} \bullet Pin}{VAC} - 0.1 \bullet \frac{\sqrt{2} \bullet Pin}{VAC} \qquad (5)$$

The peak and valley of inductor current vary with the line voltage.

Fig. 4 shows a simplified schematic of the boost converter and an expanded view of the relevant current waveforms.

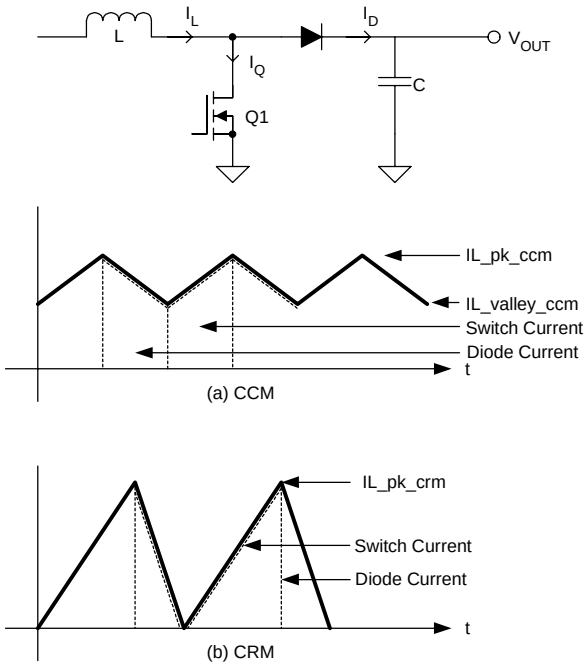


Fig. 4. Simplified boost schematic with switch and diode current waveforms.

The RMS switch current in the CCM boost is given by equation (6).[8]

$$Iq\_rms\_ccm = \frac{Pin}{VAC} \bullet \sqrt{1 - \frac{8}{3 \bullet \pi} \frac{\sqrt{2} \bullet VAC}{Vout}} \quad (6)$$

The diode turns on at the peak of inductor current as the switch turns off. The inductor current is at the valley though when the switch turns on. The conduction loss is given by equation (7).

$$Pq\_rms\_ccm = Iq\_rms\_ccm^2 \bullet Rdson \quad (7)$$

Switching loss can be broken down into the loss associated with turning the MOSFET OFF and ON, i.e. the overlap in drain voltage and current as well as the Coss loss and the reverse recovery loss of the boost diode.

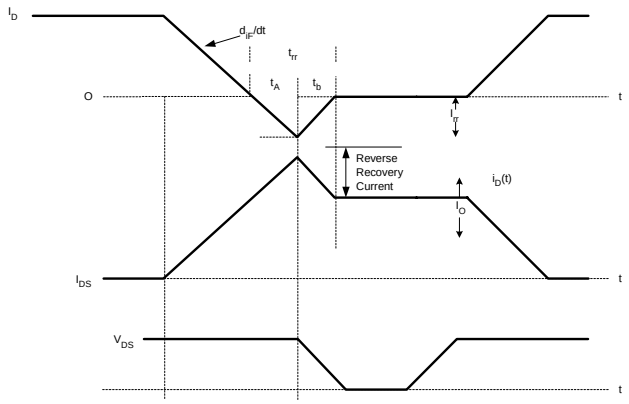


Fig. 5. Illustrates the MOSFET and diode current and voltage.

The energy losses associated with the MOSFET turn-on and turn-off are given in equation (8) and (9).

These equations describe the energy lost in a switching cycle. They need to be averaged over the line cycle and then multiplied by the switching frequency to find the total loss, (10).

Similarly the turn-on losses are summed over the line period. To get the power loss you multiply by the switching frequency, (10) and (11).

The MOSFET also experiences loss due to the reverse recovery current of the diode. This loss is very dependant on 3 terms, the di/dt of the current through the diode at turn-off, the forward current of the diode (I_F), and the reverse voltage. The effect these parameters have on the diode varies with the diode type and manufacturer.

The reverse voltage is fixed and equal to Vout. The currents through the diode vary as a function of line and load. To make things even more difficult, most manufacturers give limited data to calculate the recovery characteristic. So, the calculation of this loss term is an approximation. The MOSFET energy loss due to reverse recovery is given in (13).[9]

$$Eq\_ccm\_turnon = Vout \bullet \left[\frac{\left(IL\_valley\_ccm \bullet \left|\sin(wt)\right|\right) \bullet transistor\_rise}{2} \right] \quad (8)$$

$$Eq\_ccm\_turnoff = Vout \bullet \left[\frac{\left(IL\_pk\_ccm \bullet \left|\sin(wt)\right|\right) \bullet transistor\_fall}{2} \right] \quad (9)$$

$$Eq\_ccm\_turnoff\_tot = \frac{\sum_{i=1}^{n} Eq\_ccm\_turnon_i}{n} \quad (10)$$

$$Pq\_ccm\_turnoff\_tot = Eq\_ccm\_turnoff\_tot \bullet Fs \quad (11)$$

$$Pq\_ccm\_turnon\_tot = Eq\_ccm\_turnon\_tot \bullet Fs \quad (12)$$

$$Err = Vout \bullet \left[\frac{Irrm\_pfc \bullet \sin(wt)}{2} \bullet \frac{Irrm\_pfc \bullet \sin(wt)}{didf} + \frac{Irrm\_pfc \bullet \sin(wt)}{4} \bullet \left(trr - \frac{Irrm\_pfc \bullet \sin(wt)}{didf} \right) \right] \quad (13)$$

$$Err\_diode = Vout \bullet \left[\frac{Irrm\_pfc \bullet \sin(wt)}{4} \bullet \left(trr - \frac{Irrm\_pfc \bullet \sin(wt)}{didf} \right) \right] \quad (14)$$

$$Pdiode\_ccm = \sum_{i=1}^{200} \frac{\left(IL\_pk\_ccm \bullet \left| \sin(i \frac{\pi}{200}) \right| \right) \bullet VFF \bullet (1 - D_i)}{201} \quad (15)$$

$$Pdiodebridge\_ccm = \sum_{i=1}^{200} \frac{\left(IL\_pk\_ccm \bullet \left| \sin(i \frac{\pi}{200}) \right| \right) \bullet VFF \bullet 2}{201} \quad (16)$$

Where Irrm_pfc is the peak reverse recovery current taken from the manufacturers data sheet, and didf is the di/dt through the diode at turn-off. The sin (ωt) term is needed because the diode current, and therefore the reverse recovery current will vary with the line voltage.

Equation (13) also must be averaged over the line cycle and then multiplied by the switching frequency to find the total power.

The diode also experiences power loss during the turn-off period. This occurs during the t_b period (see Fig. 5). The loss during this time is shown in equation (14).

Diode conduction loss is simply the current in the diode multiplied by its average voltage, see equation (15).

Lastly, the input bridge rectifiers experience loss as shown in equation (16).

CRM Losses

Now lets look at the losses associated with the CRM boost. Here the switching losses in the boost diode are essentially eliminated. This of course, is the principal advantage of this approach. On the other hand the conduction losses will increase. The peak inductor current in the CRM boost is:

$$IL\_pk\_crm = \frac{2 \bullet \sqrt{2} \bullet Pin}{VAC} \quad (17)$$

Again, we can see that it is approximately twice the peak of CCM operation. The rms current through the MOSFET is shown in equation (18).[10]

$$Iq\_rms\_crm = 2 \bullet \sqrt{2} \frac{Pin}{VAC} \bullet \sqrt{\frac{1}{6} - \frac{4 \bullet \sqrt{2} \bullet VAC}{9 \bullet \pi \bullet Vout}} \quad (18)$$

The turn-off loss due to current and voltage overlap follow the same equation as the CCM case, except that the current is higher (i.e. IL_pk_crm). The turn-on loss due to commutating the inductor current into the MOSFET is zero since the current is at zero when the MOSFET turns ON. The conduction loss also is simply I_{rms}^2 x $R_{DS,on}$ with the RMS current given above.

The boost diode experiences conduction loss with the higher peak current (IL_pk_crm) as do the bridge diodes.

These equations, for both the CCM and CRM cases are included in the Appendix, where a MathCad version is given. In the Appendix, the equations are modified to calculate the losses for a range of input power.

Again, there are more losses in the power stage, which were not discussed here. These include the Coss loss in the MOSFET as well as gate charge loss. These losses will be the same for CCM operation as well as CRM operation so we are not considering them in the trade-off between the two modes of operation. For an excellent discussion of MOSFET switching behavior see reference.[11]

We've quantified the losses in the semiconductors that are different in the different operating modes. One area that has not been calculated is the magnetic losses. A detailed analysis of the magnetics is beyond the scope of this paper, and would be very dependant on filter requirements/specifications, magnetic materials used, etc. Some general comments can be made though to help compare specific cases.

First, the inductor design will be driven by the amount of loss tolerable and size constraints. In magnetic components you can trade-off core size for loss. At some point though the core size becomes too large for the application. In comparing CRM to CCM operation, the small inductance will be traded-off to higher ripple current. On the other hand, core loss is a strong function of ac flux. Clearly, the CRM case will have much higher ac flux due to the large amount of ripple current.

Loss Summary

Above a couple of hundred watts, the input filter requirements for the CRM case will dominate the size of the magnetics. At much higher power levels, there is interesting work being done to interleave CRM converters.[12] This effectively reduces the ripple current and makes the filter more manageable at the expense of a more complicated control scheme.

The above discussion and equations are intended to provide a framework for comparing the two methods in a particular application. Each individual application will have its own unique design objectives. The equations given in the text, and expanded in the Appendix, can be easily modified for a particular application or device choice. This hopefully will aid in making the trade-off for an individual application. Typically cost and size are key aspects of the requirements. Efficiency is usually important in that it effects the required heat sink/thermal design.

The equations described above were used to plot the losses of a CCM and CRM converter. The input power was swept to see where the crossover point was. The analysis was performed using identical semiconductors. For this analysis the MOSFET used was an IRF840 while the diode was an 8ETH06 diode from International Rectifier. The device parameters were taken directly from the data sheet and can be found in the Appendix. In this case, the semiconductor losses cross each other around 300 W. If magnetic losses are accounted for this point will occur slightly below 300 W.

In a boost converter one of the most difficult components to deal with is the diode. In low to medium power applications, the CRM mode can eliminate the diode issues with relatively little negative impact to the rest of the system. As the power increases, the higher currents start to tip the trade-off towards CCM operation. In CCM operation, passive snubbers and active techniques are often employed to reduce the effects of the reverse recovery current.

One interesting development to watch is the introduction of silicon carbide (SiC) devices.[16] These devices can significantly reduce the reverse recovery losses. They have a characteristic which looks capacitive. The trade-off is they have a slightly higher forward voltage drop (VFF) than a traditional Si diode. Depending on the diode and operating point, about 0.5 V higher.

PART II. BOOST CONVERTER DESIGN

POWER STAGE CONSIDERATIONS

We have looked at the topology trade-offs. Let's now take a look at the design issues and criteria associated with each operating mode.

In terms of power stage design, the main elements are the boost inductor, the power switch, the boost diode and the output capacitor. The inductor design equations are based on the ripple current specification. The selection of switches depends on the peak and RMS current through them. Because of the relatively low switching frequency of the PFC front-ends (typically in the 100 kHz or lower range), it is possible to use IGBTs with some benefits in conduction losses at high power levels. Both the power switch and the boost diode have to be rated at or above 500 V (about 20% above the boost output voltage). The boost diode should have ultrafast reverse recovery characteristics (for CCM operation). The output capacitor is generally the most expensive component in the PFC front-end. In many cases, hold-up time requirements dictate the value of this capacitor. However, the ripple current in this capacitor can be minimized by using leading edge modulation for the PFC stage while the second stage is using trailing edge modulation.[2,13]

A. Inductor Design

CCM

Typically the CCM inductor is designed with the ripple current (Δi) equaling 20% of the peak current. The main point is that the ripple current is small compared to the 60-Hz component.

To calculate the inductance:

$$L_{CCM} = \frac{\sqrt{2} \bullet VAC,min \bullet D \bullet Ts}{\Delta i} \quad (19)$$

Where VAC, min, is the minimum line voltage, Ts is the switching period, and D is the duty cycle at the peak of low line (remember D is constantly changing throughout the line cycle).

$$\Delta i = 0.2 \bullet \frac{\sqrt{2} \bullet Pin}{VAC} \quad (20)$$

$$D = \frac{Vout - VAC}{Vout} \quad (21)$$

CRM

The inductor calculation for CRM mode is different because you are designing the inductor to start the next switching cycle at zero current. The time it takes to reach zero is dependant on the line voltage and inductance. So, the inductance will determine the frequency range the converter operates over. This is typically a key parameter. To find the inductor value we first need to find equations for the on and off times. We do this by recognizing that the peak inductor current (IL_pk_crm) is also Δi.

$$IL\_pk\_crm = \frac{2 \bullet \sqrt{2} \bullet Pin}{VAC} \quad (22)$$

Also, using V=L di/dt and solving for di at the peak of the line we get:

$$\Delta i = \frac{t_{on} \bullet \sqrt{2} \bullet VAC}{L} \quad (23)$$

Setting these two equations equal to each other and solving for t_{on} yields:

$$t_{on} = \frac{2 \bullet Pin \bullet L}{VAC^2} \quad (24)$$

Similarly for t_{off}, we use the same general equations, but for t_{off} recognize that the voltage across the inductor is Vout - Vin.

$$\Delta i = \frac{t_{off} \bullet \left(Vout - \sqrt{2} \bullet VAC\right)}{L} \quad (25)$$

Again equating the IL_pk_crm equation with the Δi equation and solving for t_{off} yields:

$$t_{off} = \frac{2 \bullet \sqrt{2} \bullet Pin \bullet L}{VAC \bullet \left(Vout - \sqrt{2} \bullet VAC \bullet \sin(\omega t)\right)} \quad (26)$$

Summing t_{on} and t_{off} we can find the period and therefore the frequency. After some algebra Fs is given by equation (27).

$$Fs = \frac{Pin \bullet \left(Vout - \sqrt{2} \bullet VAC \bullet \sin(\omega t)\right)}{2 \bullet L \bullet Vout} \quad (27)$$

Here we can see that even for a given rms line voltage and load, the switching frequency will vary as the instantaneus line voltage varies. It also gives a useful design equation. Since we usually will want to fix a minimum line frequency we can solve the above equation, for the inductance that satisfies that goal. The minimum frequency will occur at the peak of the line, at this point sin(ωt) will equal 1.

$$L = \frac{VAC^2 \bullet \left(Vout - \sqrt{2} \bullet VAC\right)}{2 \bullet Fs_{min} \bullet Vout * Pin} \quad (28)$$

That completes the inductance calculation for both operating modes. The design of the inductor itself is driven in both cases by the current waveforms. Reference [14] is an excellent reference for the inductor design.

C. Switch Selection

The main switch selection in CCM and CRM operation is driven by the amount of power dissipation allowable. The equations for calculating the RMS currents, conduction and switching loss were given above. The maximum voltage rating is the same in both cases.

Choosing a device which minimizes gate charge and device capacitance is often desirable. The key is to choose a device which minimizes the sum of switching and conduction losses at a given frequency.

The diode selection is based on reverse voltage, forward current, and switching speed. Again, CRM operation significantly simplifies the diode operation. A slower and therefore less costly diode can be chosen for CRM. In CCM the diode selection is critical. As discussed above, a diode with a fast recovery characteristic is important. The equations given in Part I can be used to evaluate the energy loss associated with a given diode. SiC diodes show promise but time will tell if they become commercially viable.

D. Output Capacitor

In addition to the capacitance value and voltage rating, the output capacitor rating is influenced by the systems hold up requirements, the maximum RMS current rating, and to a lesser extent the ESR of the capacitor. Previous papers have outlined the hold-up requirements for the output capacitor.[1,2] In most cases the hold-up time is the main driver in determining the output capacitance. In CRM, at higher power levels the ESR and ripple current rating of the output capacitor operation may also have an impact.

Capacitance required for a given hold-up time is given by:

$$Co = \frac{2 \bullet Pout \bullet t_{hold-up}}{Vout^2 - Vout_{min}^2} \quad (29)$$

For the CCM case, the RMS current in the output capacitor is typically given by equation (30).

$$Ic\_RMS = \frac{V_{out}}{R_{load}} \bullet \sqrt{\frac{16 \bullet V_{out}}{3 \bullet \pi \bullet Vin_{pk}} - 1} \qquad (30)$$

However, it has been shown that the proper synchronization with the 2nd stage dc-to-dc converter can result in a significant reduction in RSM current.[13]

Fig. 6 helps illustrate the timing of the switching action between the PFC circuit and the down stream dc-to-dc converter. A simplified power stage is shown to highlight the switches. The capacitor current during a switching cycle depends on the status of the switches Q1 and Q2. The relevant waveforms are shown in Fig. 6. Clearly, when the switches are synchronized to both (Q1 and Q2), turn on at the same time, i.e. synchronized trailing edge modulation, the capacitor current experiences its highest ripple current. This is because while Q1 is ON, all the current available from the line being shunted to ground while the dc-to-dc converter is pulling its current out of the output capacitor. To maximize ripple current cancellation, the off time of Q1 should be synchronized with the on time of Q2. A straightforward way of achieving this is to implement leading edge modulation of the PFC and training edge modulation of the dc-to-dc stage.

Table 4 compares the measured RMS capacitor current for leading edge/trailing edge modulation (LEM/TEM) verses traditional trailing edge/trailing edge modulation (TEM/TEM). [15] The data shown was taken on a 200 W application. The two rows correspond to different operating points for the second stage converter, i.e. with two different duty cycles.

Table 4 illustrates that the boost capacitor ripple current can be reduced by about 50% at nominal line and about 30% at high line. Circuits to synchronize two discrete controllers can be found in reference.[15] Alternately, control ICs which combine the two controllers in one IC and provide the necessary synchronization internally are also available. The UCC38500 and UCC3851x family are good examples.

In the CRM case, the capacitor current is a little more complex. Since the frequency is varying throughout the line cycle, the overlap of diode current and downstream converter current is very difficult to predict. The rms calculation for the CCM case is also a good approximation since the rms value is relatively insensitive to the higher turn-off slope.[17] If a more exact answer is desired, simulation or measurement is the best approach.

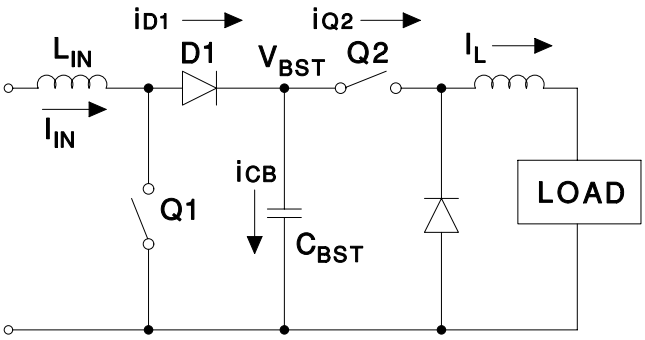


Fig. 6a. Simplified representation of two-stage power supply. Q1 is the boost switch while Q2 is the buck derived converters switch.

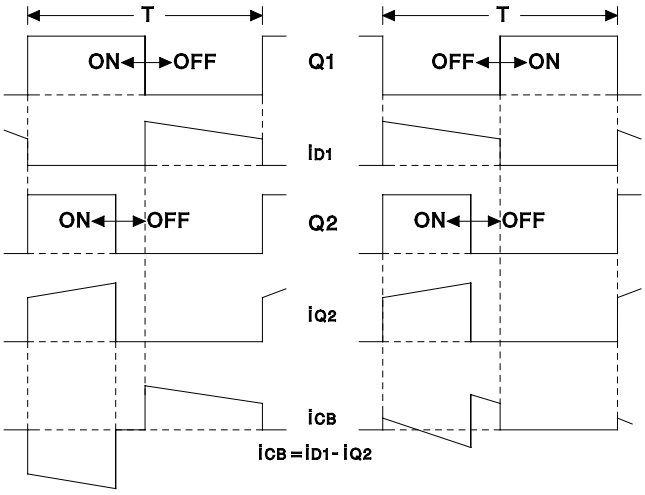


Fig. 6b. Current and voltage waveforms for trailing edge/trailing edge modulation/synchronization (left) vs. leading edge/trailing edge modulation/synchronization (right).

TABLE 4 EFFECTS OF SYNCHRONIZATION ON BOOST CONVERTER CURRENT

	V_{IN} = 85 V		V_{IN} = 240 V	
Second stage duty cycle	**Traditional TEM/TEM**	**LEM/TEM**	**Traditional TEM/TEM**	**LEM/TEM**
0.35	1.491 A	0.835 A	1.024 A	0.731 A
0.45	1.432 A	0.93 A	0.897 A	0.614 A

CONTROL CIRCUIT CONSIDERATIONS

We have taken a look at the power stage in considerable detail. This is appropriate since the power stage design is what determines the efficiency and reliability of the converter. The power stage design also influences the overall performance of the system. However, the design is not complete, nor can the converter operate properly without proper design of the control loops.

The control of the PFC circuit is usually broken down into two areas, the reference circuit for the current loop, and the control loops themselves. The reference circuit for the current loop is the multiplier.

The two techniques we are considering have slightly different algorithms to control the inductor current. In both cases the boost inductor is in the input side of the converter. Since inductor current is one of the state variables of the converter, this allows us to have a control loop directly control the input current. The CCM case typically uses average current mode control (ACMC). While it is possible to control a CCM converter using peak current mode or charge control, ACMC has the advantage of directly controlling the average input current, which is the quantity we want to control in a PFC circuit. ACMC typically gives the best line current performance of the different techniques. A basic block diagram is found in Fig. 7a.

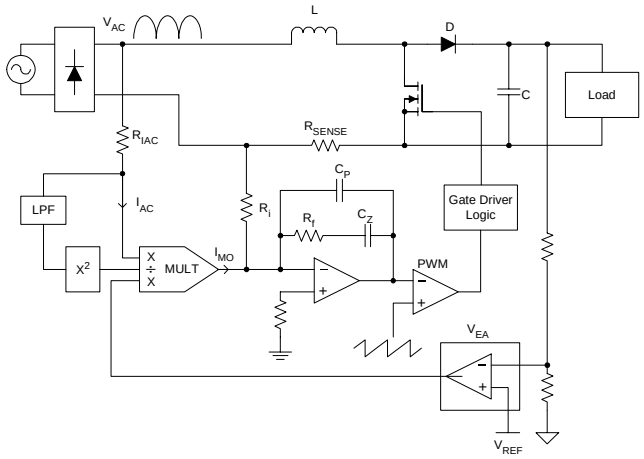


Fig. 7a. Basic block diagram of ACMC boost PFC.

The CRM converter typically uses a variation of hysteretic control with the lower boundary equal to zero current. The switch current is compared to the reference signal (multiplier output) directly. This control method has the advantage of being simple to implement. While not as high performance as the ACMC method, it provides very good PFC and is quite appropriate for power levels less than a few hundred watts. A basic block diagram is found in Fig. 7b.

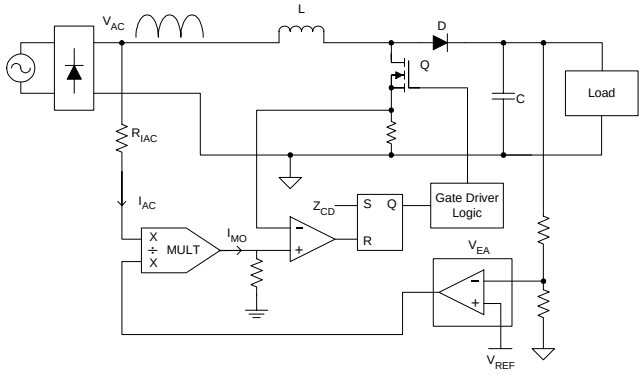


Fig. 7b. Basic block diagram of CRM boost PFC.

A. Multiplier Design Considerations

The multiplier is the heart of a PFC controller. If everything else is designed and operating properly and the multiplier is set up incorrectly, the system will not achieve good PFC. This is easily seen if one considers that the output of the multiplier is the reference for the current loop. The current loop tries to force the inductor current to follow the multiplier output. If the multiplier signal is corrupted with noise or other sources of error, the current loop will force the line current to follow the corrupted signal.

Fig. 7a and 7b shows a simplified representation of the key power stage and control elements of a boost converter. As shown, the input voltage waveform (converted to a current, I_{AC}) can be used as a reference to shape the input current waveform. The converter also needs to regulate the output voltage. The voltage error signal is combined with the I_{AC} signal to generate a signal which has the same shape as the input current and is proportional to output power. A multiplier is used in the control circuit to generate a single control parameter (I_{MO}) from multiple inputs.

In its most basic form, the multiplier combines the output voltage error signal (V_{AOUT}) generated by the voltage loop and the input voltage information represented by I_{AC}. The output of the multiplier is a current reference signal (I_{MO}) that is compared (after appropriate scaling) against the actual inductor current I_{IN} measured by the R_{SENSE} resistor. The inner current loop ensures that the inductor current follows the commanded value accurately. The outer voltage loop regulates the output voltage, but it does so with a bandwidth less than one half the line frequency. If the voltage loop had higher bandwidth, it would interfere with the current loop and cause distortion in the line current.

A closer look at the two-input multiplier reveals an inherent limitation when the input voltage (V_{IN}) changes. Fig. 8(a) and 8(b) show the input voltage and current waveforms for V_{IN} of 120 Vac and 240 Vac, respectively. As shown, when V_{IN} doubles, the input current (I_{IN}) has to halve in order to maintain constant power to the load. Fig. 9(a) and 9(b) show the two multiplier inputs for these conditions. The I_{AC} input follows V_{IN} and doubles. Since the multiplier output (I_{MO}) commands the input current, it has to halve, which can only be accomplished by reducing V_{AOUT} by a factor of four. This effectively causes the voltage loop gain to vary proportional to the input voltage range squared

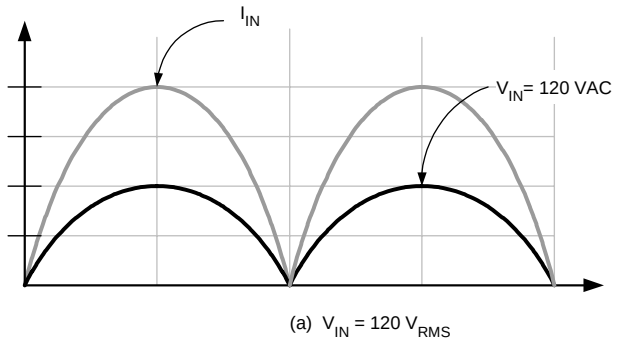


Fig. 8a. Rectified line voltage and current.

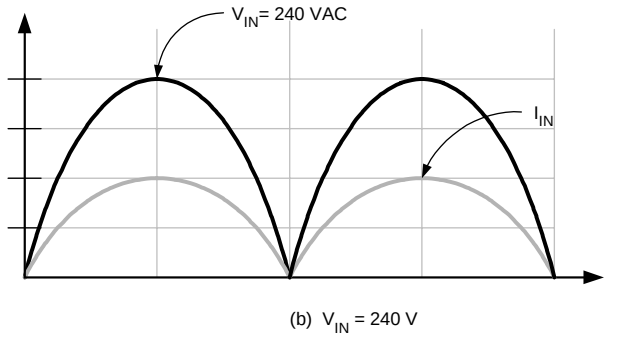


Fig. 8b. Rectified line voltage and current.

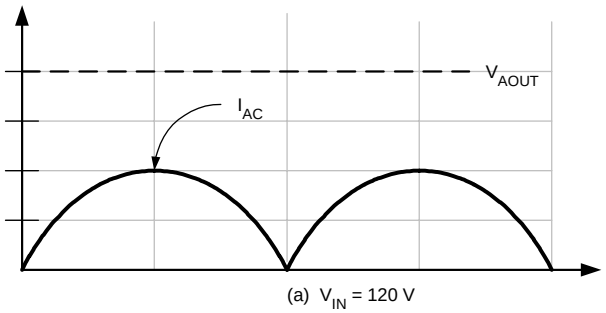


Fig. 9a. Multiplier inputs (IAC and VAOUT) at low line and high line.

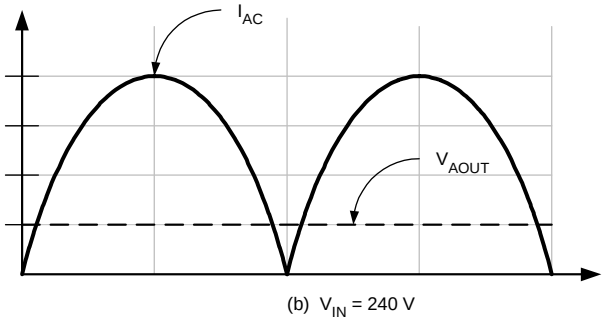


Fig. 9b. Multiplier inputs (IAC and VAOUT) at low line and high line .

Many designs have a universal input voltage range of over 3:1 (85-270 VAC) causing the basic multiplier to tax the voltage error amplifier range considerably. With a 3:1 variation in line voltage the voltage loop gain must vary 9:1. This makes for a challenging design when stability, ripple voltage reduction and transient response specifications need to be met. In addition, it is often desirable to limit the power drawn from the line when the line voltage falls below the minimum specification. In order to provide protection to the supply and the source during a brown-out condition. Without input voltage information this function is difficult to implement.

These challenges are often a good trade-off to the simplicity and low cost that is desired in lower power systems. Additionally we will see that there are techniques to improve the transient response of the lower bandwidth systems.

In systems where higher performance is desired, the multiplier is modified to include an input voltage feedforward function (V_{FF}).[1] An appropriately scaled signal proportional to input voltage is added as an input to the multiplier. The inverse of the signal is squared ($1/V_{FF}^2$) and combined with the other input terms according to equation (31). With the addition of this term, the input voltage changes do not warrant a change in V_{AOUT} for a given load. In fact, the voltage amplifier output becomes proportional to the output power for the normal operating range. To illustrate this, revisit the examples given in Fig. 8 and 9. Now, when V_{IN} doubles, the new input ($1/V_{FF}^2$) will reduce by a factor of four, and coupled with a doubled I_{AC}, will result in the desired value of half the original I_{MO} without any change in V_{AOUT}. A key advantage of this technique is constant loop gain and constant peak power over the entire input range.

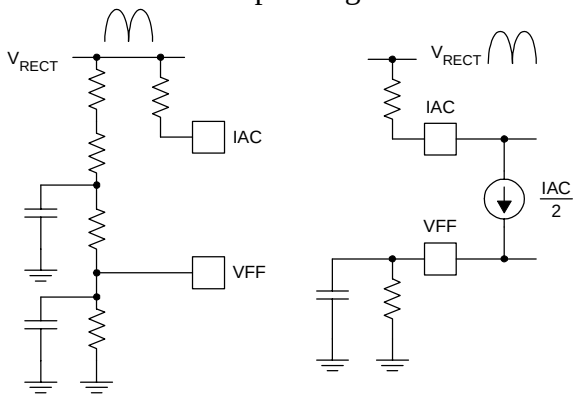


Fig. 10. Input voltage feed-forward sensing schemes.

Now lets take a closer look at the multiplier design for the 3 input multiplier. Equation (31) is the fundamental equation that governs the multiplier operation, relating the current output of the multiplier (I_{MO}) to the three inputs.

$$I_{MO} = K \bullet \frac{I_{AC} \bullet (V_{AOUT} - 1)}{V^2_{FF}} \qquad (31)$$

Where:

I_{AC} = Multiplier input current, proportional to instantaneous V_{IN}

V_{AOUT} = Output voltage error signal

V_{FF} = Average value of rectified line voltage

K = Multiplier gain

The shape of the I_{MO} current is similar to I_{AC} and the rectified input voltage. For a given V_{IN}, the peak of I_{MO} is proportional to V_{AOUT}. As already mentioned, it is important that the voltage loop has a crossover frequency significantly below the line frequency to prevent V_{AOUT} from varying during a line cycle. In other words, during a line cycle, all inputs to the multiplier other than the I_{AC} should ideally be constant.

There are three parameters we will need to calculate or specify. First the input voltage feedforward term needs to be developed.

In many ICs this voltage is derived through a resistor divider connected to the dc side of the bridge. Since this is the rectified line voltage, it needs to be filtered to remove the 120-Hz component. This can be accomplished with the use of a low pass filter. A two-stage filter was traditionally used to improve the transient response of the filter. However, in the new generation of controllers (e.g. UCC3817) this function has been simplified by mirroring the I_{AC} current into a single-pole filter. This approach does have a slower transient response than the two-stage approach. However, the feedforward term is primarily intended to correct for the large variations in line voltage seen with universal applications. For a given power supply, the input voltage does not change instantaneously from 120 V to 240 V, so a fast transient response is really not required. This approach is shown in Fig. 10. The single pole filter approach lowers system cost with reasonable performance.

Before designing the low pass filter for VFF the amount of attenuation needs to be determined. The amount of attenuation is driven by the allowable distortion budget. For a system looking to achieve 3% THD, it is typical to allow the feedforward circuit to contribute 1.5% 3rd harmonic distortion to the input waveform.[2] This leaves 0.75% for the voltage loop and 0.75% for all others sources. The rectified line voltage is a 120-Hz signal. The percent of second harmonic in the waveform is 66.2% of the average value. Therefore the attenuation needed is 1.5/66.2 or 0.022. From here it is easy to calculate the required pole frequency.

A handy relationship to remember is that for a single pole roll-off (or 20 dB/decade) a linear relationship exists between the gain and frequency (see Fig. 11). The desired gain at 120 Hz is 0.022, the gain at the pole frequency is approximately 1. Since we know 3 out of 4 variables, the pole frequency can be found:

$$f_P = 120 \bullet \frac{0.022}{1} = 2.6\text{Hz} \qquad (32)$$

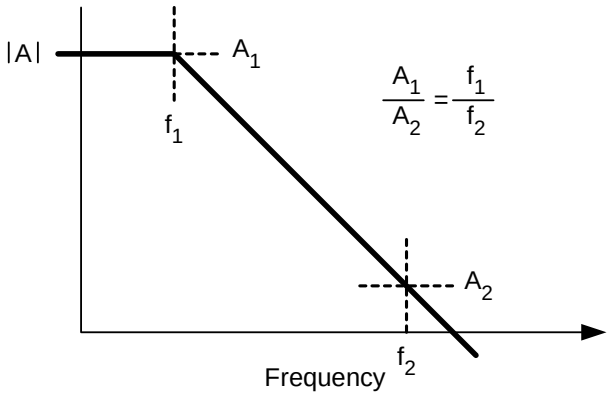


Fig. 11. V_{FF} single pole filter characteristics.

The filter is implemented with a parallel R/C circuit. The resistor is calculated to ensure the voltage on V_{FF} stays within its dynamic range over the full line. At low line (85 V_{RMS}) we want the multiplier to start entering the power-limiting region (see Fig. 13).[1] In the UCC3817 and UCC38500 control ICs the multiplier starts limiting current when V_{FF} = 1.4 V. Therefore the resistor is chosen so that at low line the voltage at the multiplier input is equal to 1.4V. If at high line the peak I_{AC} is 500 uA then the dc current through the RMS resistor will be I_{AC} divided by 2 (due to the internal current mirror) times 0.9. The 0.9 term is the conversion factor for RMS to dc for a full wave rectified signal. This gives a resistor value of 25 kΩ. The capacitor required to give a pole frequency of 2.6 Hz is approximately 2.2 μF.

Completing the multiplier set up is determining the IMO resistor. The typical approach[15], for ICs which incorporate a power-limiting characteristic, is to design for maximum power at minimum line.

Fig. 13 shows the product of V_{FF} and I_{MO-PK} (a quantity representative of input power since V_{FF} and I_{MO-PK} are proportional to V_{IN-RMS} and $I_{IN(PK/RMS)}$, respectively) as a function of V_{FF} (again, proportional to V_{IN-RMS}) for a fixed value of V_{AOUT}. For this discussion, the curve can be viewed as representing the maximum V_{AOUT} (full load) condition. There are two distinct regions of operation. The first region, labeled constant power region, is the area where the multiplier operates over nominal line range. Referring to Equation (1) and rearranging terms, it can be seen that the $I_{MO-PK} \times V_{FF}$ term will be constant over the V_{IN} range for a given V_{AOUT}. This is because I_{AC-PK} and V_{FF} vary proportionally.

The second region, labeled "power limiting region", is important for protecting the converter under line dropout or brownout situations. The multiplier output is limited in this region so that the input current is contained and the power stage components are protected from overheating at low line operation. In this region, the output power requirements are not met and the output voltage starts dropping.[2]

The key is to pick a multiplier-terminating resistor so that the multiplier can command sufficient current from the line to satisfy the load. The worst case, or maximum current required is at low line voltage, with maximum load. Again, the typical approach is to use the fundamental multiplier equation and plug in the appropriate conditions. Solving (31) (with I_{AC} 500 uA, V_{FF} = 1.4 V and V_{AOUT} = 5 V) gives an I_{MO} 360 µA.

The voltage required at the I_{MO} pin is the voltage which when developed across the R_{sense} resistor will translate into the required line current to support the load. For a 250 W converter, (low line I_{INpk} is 4.4 A) and a 0.25 Ω sense resistor, this translates to:

$$R_{IMO} = \frac{I_{INpk} \bullet R_{Sense}}{I_{MO}} \approx 3k\Omega \qquad (33)$$

There is, of course, a wrinkle in this design procedure. This assumes that the IC multiplier will supply exactly the desired current for the given inputs. In other words, the multiplier behaves exactly according to equation (31).

In reality the multiplier has a tolerance associated with it. In order to ensure that the converter will be able to supply the required power, the calculations should be checked at high line and low line using the minimum multiplier current. In most cases a larger R_{IMO} will be required.

Again refering to Fig. 13, the effects of these variations in multiplier current can be seen.

The upper deviation is normally not a cause for concern because supporting higher power at higher line voltages will not cause additional thermal stress on the system (since the input current is still less than it is at low line, full load).

Once the minimum multiplier resistor is found, the input power should be calculated over the "corners" of multiplier operation. The main issue to be analyzed is the maximum power the converter is now able to draw from the line. Keep in mind that in parts that allow the upper range of multiplier current the voltage amplifier will still regulate the output so that only the required current will be supplied to the load. This simply means that in a fault condition, the load can increase up to the new level.

The power supply has a handle to limit this potential problem though. Peak current limit will limit the input current on a cycle-by-cycle basis. This will prevent the power stage from experiencing excessive thermal problems. The choice of power devices and thermal design should take this into account.

Fig. 12 shows the peak multiplier output current (I_{MO-PK}) verses V_{AOUT} for a given line voltage (V_{IN} and V_{FF}). The instantaneous I_{MO} will vary between 0 and I_{MO-PK} during a line cycle. Any multiplier non-idealities in the middle portion of the curve can be compensated by adjusting V_{AOUT} through the outer loop. For example, if I_{MO} is not adequate at a given condition, V_O will drop, V_{AOUT} will increase and I_{MO} will be adjusted.

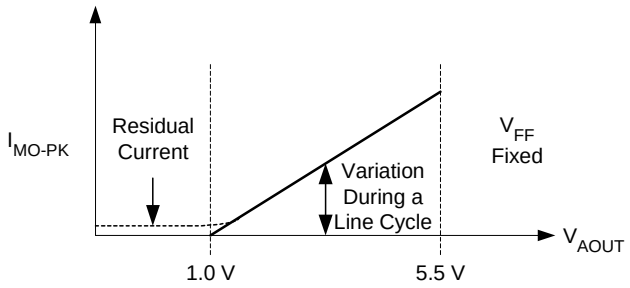


Fig. 12. Peak multiplier output current.

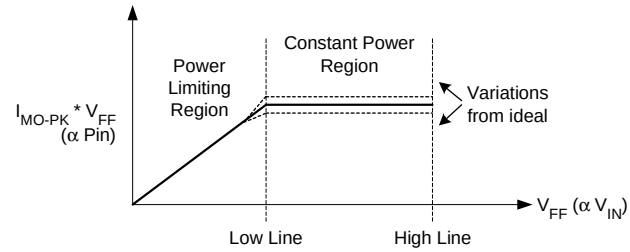


Fig. 13. Multiplier power profile, as a function of line for a fixed V_{AOUT}.

At low power operation, V_{AOUT} approaches the lower end of its operating range (1 V) and commands zero I_{MO} at no load. If there is residual (non-zero) I_{MO} at this point, some power will be delivered to the load. In the extreme case, this can lead to overvoltage on the output and trigger the OVP (overvoltage protection) circuit in the system. The consequences of reaching an overvoltage condition include higher stress on the devices (output cap, diode and FET) as well as controller biasing (Vcc) problems. During the OVP condition, switching is stopped and the self-bias circuit used in many systems (a winding off the boost inductor) loses its energy source. The controller Vcc can fall below the UVLO (undervoltage lockout) turn-off threshold during this condition and lead to a hiccup operation mode.

To prevent this effect, the residual I_{MO} should be minimized. In addition, an alternate path to limit switching can be provided. Once V_{AOUT} falls below a set threshold (e.g. 0.33 V), it can be interpreted as a zero power command and a direct signal to the output to stop switching can be generated. This zero power detect (ZPD) technique, incorporated in the new generation PFC controllers, helps prevent an overvoltage condition.

Another benefit of the ZPD technique is that it also compensates for input offset voltage in the current error amplifier. It can be shown that positive current amplifier input offset voltage can also result in power delivery under no load conditions (same effect as described above). Some controllers intentionally skew the offset in the opposite direction to negate this effect. However, that results in distortion near every zero crossing (due to the artificial offset). With the ZPD technique, the current amplifier can be designed for near-zero offset with assurance that the low power mode will be adequately handled.

The two input multiplier is fairly easy and straightforward to set up. The multiplier output is terminated within the IC, so there is now need to calculate a R_{IMO}. Additionally there is no V_{FF} to set up. The line input circuit needs to be configured to provide the correct voltage over the line range. This is accomplished by a simple voltage divider off the rectified line with the main criteria being that the voltage stays within the input voltage specification of the IC over the full line range.

The only other input is the voltage amplifier, which we will discuss in the next section.

B. Control Loop Design Considerations

The design of the voltage and current loops has a large impact on system performance. Both loops can directly contribute to line current distortion. Several good references exist which go into detail on the theory as well as the details of control loop design.[1,2,8,18]

Designing the current loop is usually the first step after the power stage has been designed. The main job of the current loop is to force the inductor current to follow the multiplier reference current. Keep in mind that the reference current is not simply a 120-Hz waveform. A full-wave rectified waveform is rich in harmonics. This waveform has a high dv/dt around the zero crossings of the line. A current loop bandwidth of around 10 kHz, for a line frequency of 50 Hz to 60 Hz, is usually adequate.

The CRM topology really doesn't require a current loop design. The control law is simple hysteretic control (with the lower boundary set to zero), so there is no compensation to be designed.

The only thing that needs calculating is the current sense resistor. This is fairly straightforward. You simply ensure that the peak current produces a voltage which, when compared against the peak multiplier signal, is sufficient to produce maximum power.

Average Current Mode Control

The ACMC converter does have an inner current loop, which needs compensation. In order to properly compensate the loop a model of the converter is needed. A small signal model of the converter based on the PWM switch model is shown in Fig. 14.[18]

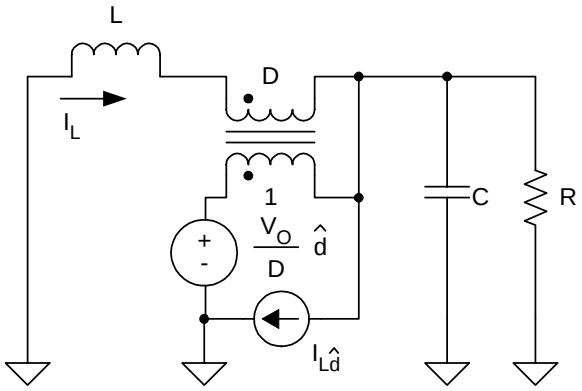


Fig. 14a. "Exact" model of boost PFC using PWM switch model.

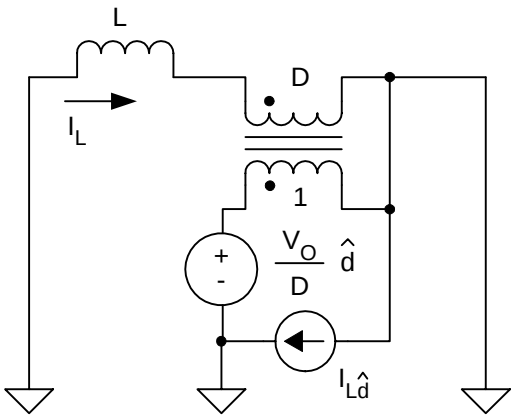


Fig. 14b. Simplified model.

Fig. 14a shows the "exact" model, while Fig. 14b shows the "simplified" model if we assume the output capacitor is large and the switching frequency ripple is small. This is a reasonable approximation for realistic circuit designs.

The transfer function for the circuit in Fig. 14a is shown below.

$$G_{id}(s) = \frac{2 \bullet V_{out} \bullet R_{SENSE}}{R \bullet (1-D)^2} \bullet \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_o \bullet Q} + \left(\frac{s}{\omega_o}\right)^2}$$

$$\omega_z = \frac{2}{R\,C} \quad , \quad \omega_o = \frac{1-D}{\sqrt{LC}}$$

$$Q = R(1-D)\sqrt{C/L} \qquad (34)$$

The R_{sense} term isn't seen directly from the figure but is included here since it relates the actual inductor current to the signal seen at the IC.

This equation is plotted in Fig. 15 for high line and low line. At higher frequencies the plot converges to the simplified model shown in Fig. 14b. The simplified model is easier to use and is adequate to design the current loop. The exact model is shown to explain what is seen if one measures the loop.

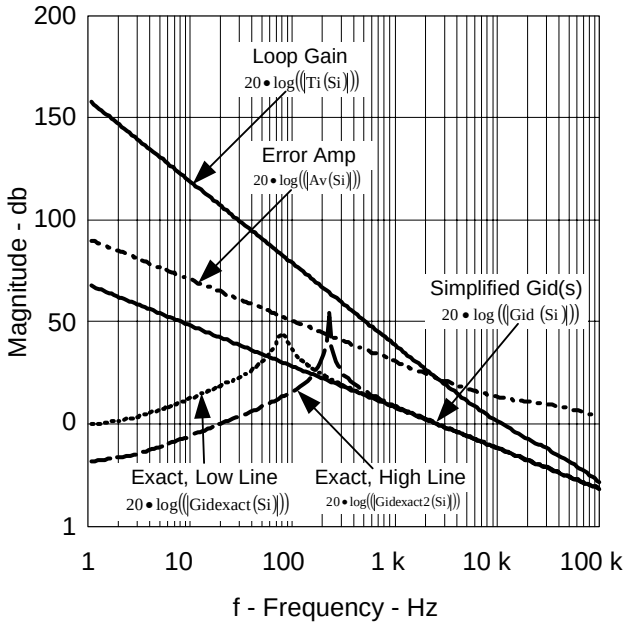


Fig. 15a. Magnitude of the current loop, eqn 34,35 and E/A transfer function.

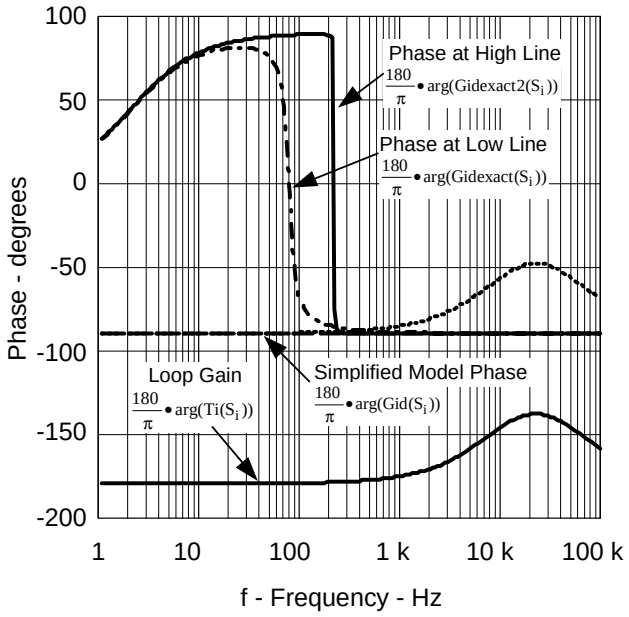


Fig. 15b. Phase plots.

The simplified current loop transfer function is given in equation (35). This has a single pole response at the usual frequencies of interest. It is typically compensated with a two pole, single zero error amplifier as shown in Fig. 16. The zero is placed to achieve the desired phase margin and the high frequency pole is placed to filter switching noise.[18]

$$G_{id}(s) = \frac{V_{out} \bullet R_{SENSE}}{s \bullet L \bullet V_{SE}} \tag{35}$$

where V_{SE} is the oscillator voltage peak to peak.

A step by step design procedure is given below.

First calculate the gain of the power stage at the desired crossover frequency (f_c):

$$\left|G_{id}(s)\right| = \frac{V_{out} \bullet R_{SENSE}}{2 \bullet \pi \bullet f_c \bullet L \bullet V_{SE}} = x \tag{36}$$

Set the midband gain (A_v) of the current loop error amplifier to be 1/x. The resistors Rf and Ri set the midband gain.

$$G_{EA} = \frac{1}{\left|G_{id}(s)\right|} = \frac{1}{x} \Rightarrow Av = \frac{R_f}{R_i} \tag{37}$$

The zero of the compensation network (f_z) is placed at the crossover frequency.

$$f_z = f_c \Rightarrow C_z = \frac{1}{2 \bullet \pi \bullet R_f \bullet f_c} \tag{38}$$

The compensator pole is placed between ½ f_s (switching frequency) and f_s to attenuate noise, see equation (39).

$$f_p = \frac{1}{2 \bullet \pi \bullet R_f \bullet \left(\frac{C_z \bullet C_p}{C_z + C_p}\right)} \approx \frac{1}{2 \bullet \pi \bullet R_f \bullet C_p} \Rightarrow C_p = \frac{1}{2 \bullet \pi \bullet R_f \bullet f_p} \tag{39}$$

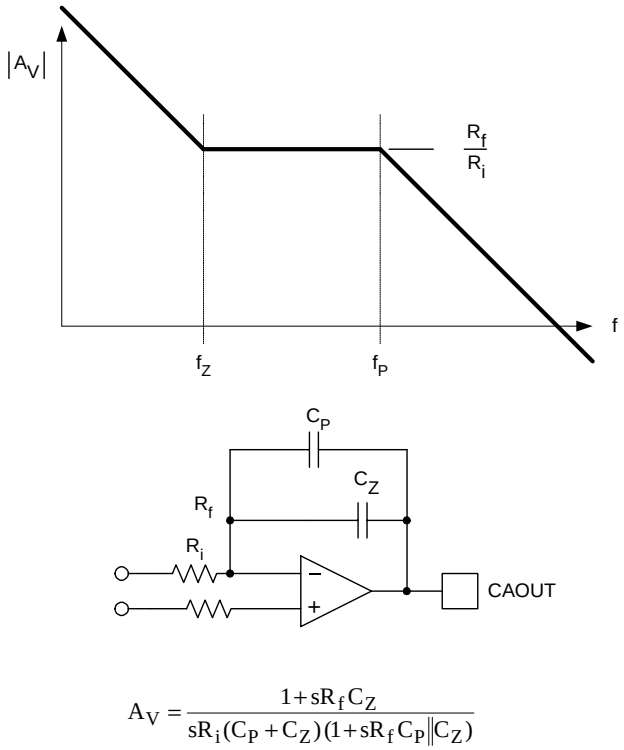


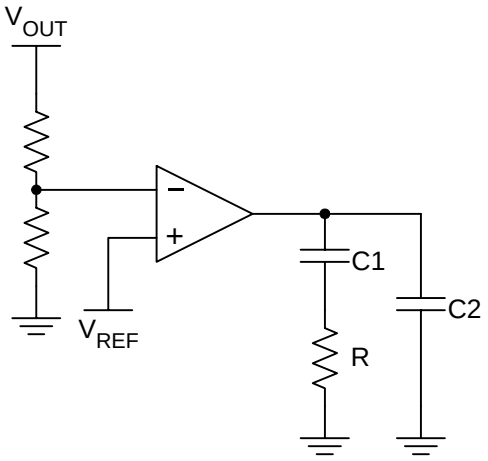
Fig. 16. Current loop error amplifier.

C. Voltage Loop Design

There are some trade-offs inherent in the voltage loop design that are particular to PFC applications. The fundamental requirement of power balance, on the line frequency time scale, requires that the voltage loop's bandwidth must be less than the line frequency (actually less than 1/2 the line frequency). If not, the voltage loop will distort the line current in order to regulate the output voltage. This creates a trade-off between power factor and transient response.

Since the loop bandwidth is low to begin with, it is normally advised to avoid integral compensation due to the further reduction in transient response that the relatively large feedback capacitor will cause. The large feedback capacitor required for integral compensation will limit the slew rate of the error amplifier. This is especially troublesome at start up when the poor transient response can cause a large overvoltage condition. Another issue is that the dc regulation of the output voltage is proportional to the loop gain. With the voltage loop gain set relatively low (with proportional gain), the output voltage will vary widely with line and load. Since the load of a PFC circuit is typically another converter, dc regulation may not an issue, and start up transient response can be more of a concern (due to the voltage stress on the output capacitors).

However, in some applications where the downstream converter is optimized for a narrow input voltage range or when maximum hold up time is required, dc regulation is more of an issue. Additionally, some PFC controllers employ a transconductance type amplifier. This is often done so that multiple functions, such as over voltage detection, can be incorporated on one IC pin. The traditional voltage type error amplifier precludes this since in a closed loop system the Vsense pin is not proportional to Vout. A transconductance amplifier's sense pin gives a true measure of output voltage whether the loop is in regulation or not. However, transconductance amplifiers are compensated by connecting an impedance between the amplifier's output and ground. Usually the amplifier's output current capability is insufficient to drive a resistive load unless the desired dc gain is very high. This implies capacitive loading and hence integral gain. In both cases then (transconductance amplifier or needing tighter dc regulation) integral compensation can be used. The gm amplifier configuration is shown in Fig. 17.



$$A_V = gm\frac{1+SRC1}{S(C1+C2)(1+SRC1\|C2)}$$

Fig. 17. gm amplifier configuration.

Integral compensation will provide zero dc error. However, since the power stage has a single pole roll-off and the integrator adds another 90 degrees of phase shift at low frequency, a zero is needed before the loop cross-over frequency. Since a zero in the compensation network becomes a pole in the closed loop gain, this zero will become the dominant pole in the system and placing this zero as high as possible in frequency will improve the transient response. Since the loop has such poor bandwidth, any improvement is welcome.

The model of the power stage with the current loop closed is shown in Fig. 18. For the case where the load is a dc-to-dc converter, the load is considered a constant power load. Therefore it has a negative small signal resistance associated with it. The negative resistance is equal an opposite in sign to the dc resistance and the two cancel each other. The gain of the power stage is given by equation (40).[2]

$$G_{PS}(s) = \frac{Pin}{(s \bullet Cout) \bullet Vout \bullet \Delta Vaout} \qquad (40)$$

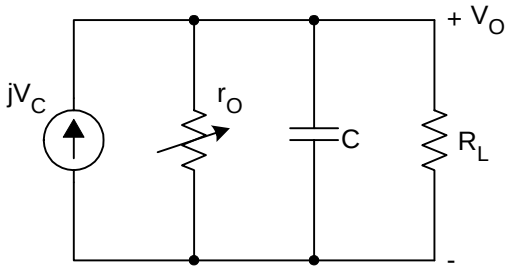


Fig. 18. Small signal model of outer voltage loop. For constant power loads, $r_o = -R_L$.

The gain for the CRM converter would be essentially the same. However, in some cases the control circuit uses a multiplier without the feedforward term. The loop gain is then a function of input voltage and is shown in equation (41).[2]

$$G_{PS}(s) = \frac{k_1 \bullet VAC^2}{(s \bullet Cout) \bullet Vout \bullet R_{sense} \bullet k_{crm}} \quad (41)$$

where k_1 is the multiplier gain, including the input voltage divider and k_{crm} is a factor of 2 for the case where the power stage is operating in CRM mode. This factor accounts for the fact that the peak of the input current is actually twice the average value.

The main design criteria for the voltage loop is usually reduction of the 120-Hz ripple component being fed back to the multiplier.[2] This is due to the fact that the ripple at the output of the voltage error amplifier is a major contributor to 3rd order harmonics in the line current. However, in some cases some increased 3rd order harmonic distortion can be tolerated and traded-off for improvements in transient response.

There are several options for designing the voltage loop compensation[13]. When using integral compensation, trade-offs can be made between 120 Hz attenuation and transient response improvements. You can trade off response using similar techniques as typically used when designing traditional voltage loops, with the added specification being 3rd order harmonic reduction.

Besides compensation methods to speed up transient response, the amplifier itself can be modified to improve the response. In systems which use a transconductance amplifier is is especially useful. There is a trade-off in designing the transconductance (gm) amplifier. For a simple gm amplifier the output current is related to the gm of the amplifier. More drive current helps slew the feedback capacitor. However, as the current is increased, the gm increases. For a given pole frequency, the higher gm tends to cause a larger capacitor to be required. This defeats the advantage of higher current capability. The trick is to design the amplifier with the appropriate amount of small signal gain (gm) while increasing the transient current capability of the amplifier.

Once the Vsense pin exceeds a threshold, it is a good indication that there is a transient condition and the loop needs to respond to force the output back into regulation. At this point the amplifier increases the drive current which causes the voltage on the feedback capacitors to slew. This amplifier output current characteristic is shown in Fig. 19a and Fig. 19b. Fig. 19a shows the small signal gain of the amplifier. Fig. 19b, shows the increased current capability as the error signal is increased. The advantage is that the amplifier is able to slew the compensation components quickly, and therefore can respond during start-up or a transient, before the output voltage overshoots excessively. This technique is implemented in some newer PFC controllers such as the UCC3851x, and UCC38050 family of controllers.

Returning to the compensation procedure, if we use the traditional approach to compensate the loop we first need to calculate the output voltage ripple.[2] Equation (42) gives the peak ripple on the boost capacitor.

$$v_{Opk} = \frac{Pin}{(2\pi \bullet f_{Ripple} \bullet Cout) \bullet Vout} \quad (42)$$

Recall from the multiplier section that we allow a 0.75% 3rd harmonic distortion contribution from the voltage amplifier. This distortion will be generated by 1.5% of the 120 Hz ripple feed back into the multiplier[2]. From this you can calculate the attenuation required and therefore the error amplifier gain at 120 Hz. If we assume the ripple voltage is 4 V, 1.5% is 60 mV. Therefore the amplifier gain (G_{VEA}) at 120 Hz is 60 mV/4 V or 0.015 or –36 dB.

The gain of the power stage is shown in equation (43).

$$G_{PS}(s) = \frac{Pin}{(s \bullet Cout) \bullet Vout \bullet \Delta Vaout} \qquad (43)$$

One approach to closing the loop is to use an error amplifier with the same configuration as we used in the current loop. In this case we calculate where to place the second pole of the error amplifier by placing it at the loop gain cross-over frequency. In other words we know the loop gain response after the zero crossing is a double pole, and we know the desired gain at 120 Hz, we can therefore calculate the frequency where we will cross 0 dB.

$$f_{pole} = 120Hz \bullet \sqrt{G_{PS}(120) \bullet G_{VEA}(120)} \qquad (44)$$

In order to maintain adequate phase margin, the zero is placed well below the pole frequency. If it is placed a full decade below, the voltage loop will have about 45 degrees of phase margin.

For example, if we assume a transconductance amplifier with a gm = 100µS, and we know the desired gain of the error amplifier at 120 Hz, we can calculate the required compensation network.

$$Gvea = gm \bullet Zout \qquad (45)$$

where Gvea is the voltage amplifiers gain. We know the attenuation we need at 120 Hz (in this case 0.015). In a transconductance configuration, the output voltage divider contributes to the attenuation also, so the error amplifier gain is:

$$Gvea_{120\ Hz} = \frac{G_{120\ Hz}}{V_{divider}} \qquad (46)$$

Zout is the impedance of the compensation network at 120 Hz. A good approximation is:

$$C2 = \frac{1}{2\pi \bullet 120 \bullet Zout} \qquad (47)$$

A Bode plot of an example is shown in Fig. 20.

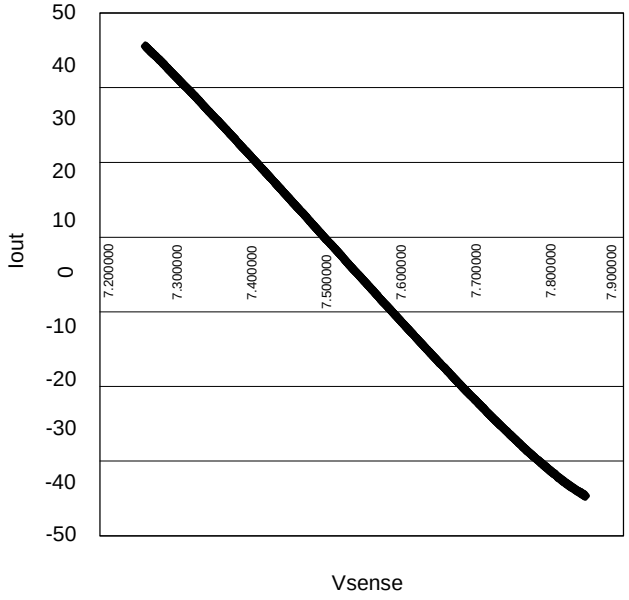


Fig. 19a. Small signal gain (transconductance) of the amplifier.

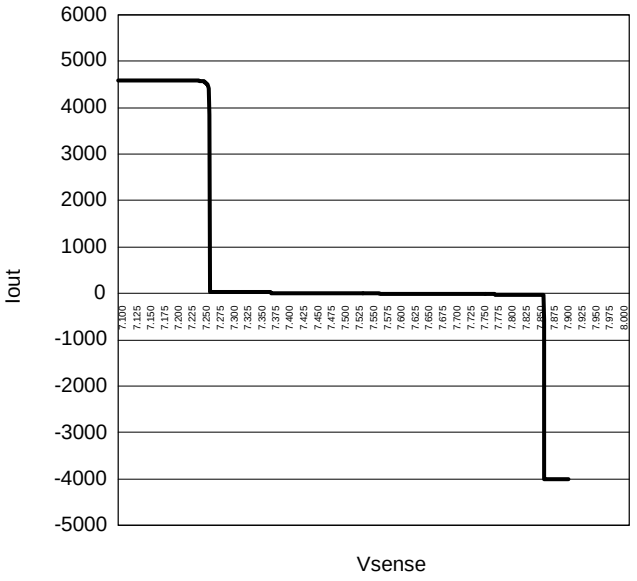


Fig. 19b. Large signal gain, showing increased current capability.

CONCLUSION/SUMMARY

Several of the more important design considerations for PFC converters have been presented. One of the first choices a power supply designer most make is which topology to use for a given application. A framework for comparing the CCM boost with the CRM boost converter has been presented. The main trade-off in the comparison is lower losses due to no reverse recovery in the boost diode vs. higher ripple and peak currents in the devices. This trade-off usually favors the CRM technique at power levels below a few hundred watts. Above that range the higher currents and the increased filter requirements for the CRM topology make the CCM technique more attractive.

We have also reviewed the main design considerations for the power stage and control circuit design. General guidelines have been presented.

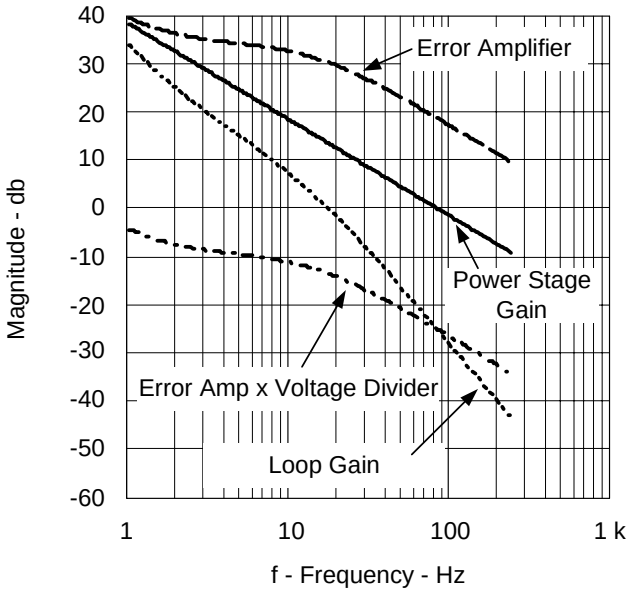


Fig. 20. Bode plots for outer voltage loop design.

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APPENDIX

This worksheet calculates the relevant currents and voltages as well as losses in PFC boost topologies. Constant output voltage and continuos conduction mode (CCM) and critical conduction mode (CRM) operation is assumed.

Constants:

$p := 10^{-12}$ $\quad nano := 10^{-9}$ $\quad u := 10^{-6}$ $\quad m := 10^{-3}$ $\quad k := 10^{3}$ $\quad MEG := 10^{6}$ $\quad j := \sqrt{-1}$

$i := 0..200$ $\quad y := 1..5$ $\quad x := 0..4$ $\quad Fs := 100 \cdot k$

$Vout := 385$ $\quad VAC\_min := 85$ $\quad VAC := 120$

$Pout := 200$ $\quad \eta := 0.95$ $\quad Pin := \frac{Pout}{\eta}$ $\quad Iload := \frac{Pout}{Vout}$

Pin_var allows input power to be varied over a range to compare losses.

$$Pin\_var_x := Pin \cdot (x + 1)$$

$$j := 0..5$$

$$VAC2 := \begin{pmatrix} 85 \\ 120 \\ 132 \\ 215 \\ 240 \\ 265 \end{pmatrix}$$

$$Vin_i := \sqrt{2} \cdot VAC \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right|$$

Boost converter duty cycle

$$D_i := \frac{Vout - Vin_i}{Vout}$$

Average boost inductor current in CCM.

$$IAC_i := \frac{Vin_i \cdot Pin}{VAC^2}$$

A. Calculate currents in the CCM boost

RMS switch current

$$Iq\_rms\_ccm := \frac{Pin}{VAC} \cdot \sqrt{1 - \frac{8}{3 \cdot \pi} \cdot \frac{\sqrt{2} \cdot VAC}{Vout}}$$

$$Iq\_rms\_ccm = 1.388$$

RMS switch current varying as a function of input power.

$$Iq\_rms\_ccm\_var_x := \frac{Pin\_var_x}{VAC} \cdot \sqrt{1 - \frac{8}{3 \cdot \pi} \cdot \frac{\sqrt{2} \cdot VAC}{Vout}}$$

Peak inductor current

$$IL\_pk\_ccm := \frac{\sqrt{2} \cdot Pin}{VAC} + 0.1 \cdot \frac{\sqrt{2} \cdot Pin}{VAC}$$

Let delta i in CCM inductor be 20% of peak current at low line.

$$IL\_ripple := 0.2 \cdot \frac{\sqrt{2} \cdot Pin}{VAC}$$

Pk current is Iin avg + 1/2 delta i

Peak inductor current as a function of input power

$$IL\_pk\_ccm\_var_x := \frac{\sqrt{2} \cdot Pin\_var_x}{VAC} + 0.1 \cdot \frac{\sqrt{2} \cdot Pin\_var_x}{VAC}$$

Inductor current valley

$$IL\_valley\_ccm := \frac{\sqrt{2} \cdot Pin}{VAC} - \left(0.1 \cdot \frac{\sqrt{2} \cdot Pin}{VAC} \right)$$

$$IL\_valley\_ccm = 2.233$$

$$IL\_valley\_ccm\_var_x := \frac{\sqrt{2} \cdot Pin\_var_x}{VAC} - \left(0.1 \cdot \frac{\sqrt{2} \cdot Pin\_var_x}{VAC} \right)$$

Peak diode current is equal to the peak inductor current.

$$Idiode\_pk\_ccm := IL\_pk\_ccm$$

B. Calculate currents in the CRM boost converter:

$$IL\_pk\_crm := 2\sqrt{2}\cdot\frac{Pin}{VAC}$$

$$IL\_pk\_crm = 4.962$$

Peak current in CRM is twice the CCM current, neglecting the ripple current for CCM.

$$IL\_pk\_crm\_var_x := 2\sqrt{2}\cdot\frac{Pin\_var_x}{VAC}$$

$$IL\_pk\_crm\_var_x := 2\sqrt{2}\cdot\frac{Pin\_var_x}{VAC}$$

$$Iq\_rms\_crm := \sqrt{\frac{1}{6} - 4\cdot\sqrt{2}\frac{VAC}{9\cdot\pi\cdot Vout}}\cdot IL\_pk\_crm$$

$$Iq\_rms\_crm = 1.603$$

$$Iq\_rms\_crm\_var_x := \sqrt{\frac{1}{6} - 4\cdot\sqrt{2}\frac{VAC}{9\cdot\pi\cdot Vout}}\cdot IL\_pk\_crm\_var_x$$

$$Idiode\_pk\_crm := IL\_pk\_crm$$

C. Calculate loss components.

Calculate diode related losses:

Assume di/dt at turn off is 100A/us.

For the purpose of calculation use the 8ETH06 IR diode as reference. Also assume IRF840 for MOSFET

$$VFF := 0.6$$

$$trr := 50\cdot nano \qquad Qrr := 120\cdot nano \qquad Irrm := 4.8 \qquad didf := 100\cdot\frac{1}{u} \qquad Rdson := 0.85$$

$$transistor\_rise := 75\cdot nano$$

$$transistor\_fall := 75\cdot nano$$

$$Irrm\_pfc_i := Irrm\cdot\left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|$$

Loss in MOSFET due to reverse recovery current from boost diode. Only valid for CCM operation.

$$\text{Prr\_ccm\_var} := \begin{bmatrix} \dfrac{\sum_{i=0}^{200} \text{Vout}\cdot\left[\left(\dfrac{\text{Irrm\_pfc}_i}{2}\cdot\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)+\dfrac{\text{Irrm\_pfc}_i}{4}\cdot\left(\text{trr}-\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)\right]}{201}\cdot\text{Fs} \\ \dfrac{\sum_{i=0}^{200} \text{Vout}\cdot\left[\left(\dfrac{1.5\text{Irrm\_pfc}_i}{2}\cdot\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)+\dfrac{(1.5\text{Irrm\_pfc})_i}{4}\cdot\left(\text{trr}-\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)\right]}{201}\cdot\text{Fs} \\ \dfrac{\sum_{i=0}^{200} \text{Vout}\cdot\left[\left[\dfrac{(2\text{Irrm\_pfc})_i}{2}\cdot\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right]+\dfrac{(2\text{Irrm\_pfc})_i}{4}\cdot\left(\text{trr}-\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)\right]}{201}\cdot\text{Fs} \\ \dfrac{\sum_{i=0}^{200} \text{Vout}\cdot\left[\left[\dfrac{(2.5\text{Irrm\_pfc})_i}{2}\cdot\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right]+\dfrac{2.5\text{Irrm\_pfc}_i}{4}\cdot\left(\text{trr}-\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)\right]}{201}\cdot\text{Fs} \\ \dfrac{\sum_{i=0}^{200} \text{Vout}\cdot\left[\left[\dfrac{(3\text{Irrm\_pfc})_i}{2}\cdot\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right]+\dfrac{(3\text{Irrm\_pfc})_i}{4}\cdot\left(\text{trr}-\dfrac{\text{Irrm\_pfc}_i}{\text{didf}}\right)\right]}{201}\cdot\text{Fs} \end{bmatrix}$$

$$\text{Prr\_ccm\_var} = \begin{pmatrix} 2.567 \\ 3.85 \\ 5.133 \\ 6.416 \\ 7.7 \end{pmatrix}$$

Losses in MOSFET due to turn-off overlap of voltage and current:

$$Pq\_ccm\_turnoff\_var := \begin{bmatrix} \frac{\sum_{i=0}^{200} Vout \cdot \left[\frac{\left(IL\_pk\_ccm\_var_0 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs \\ \frac{\sum_{i=0}^{200} Vout \cdot \left[\frac{\left(IL\_pk\_ccm\_var_1 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs \\ \frac{\sum_{i=0}^{200} Vout \cdot \left[\frac{\left(IL\_pk\_ccm\_var_2 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs \\ \frac{\sum_{i=0}^{200} Vout \cdot \left[\frac{\left(IL\_pk\_ccm\_var_3 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs \\ \frac{\sum_{i=0}^{200} Vout \cdot \left[\frac{\left(IL\_pk\_ccm\_var_4 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs \end{bmatrix}$$

Losses in MOSFET due to turn-on overlap of voltage and current:

$$Pq\_ccm\_turnon\_var := \begin{bmatrix} \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\left[\dfrac{\left(IL\_valley\_ccm\_var_0 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_rise)}{2} \right] \right]}{201} \cdot Fs \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_valley\_ccm\_var_1 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_rise)}{2} \right]}{201} \cdot Fs \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_valley\_ccm\_var_2 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_rise)}{2} \right]}{201} \cdot Fs \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_valley\_ccm\_var_3 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_rise)}{2} \right]}{201} \cdot Fs \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_valley\_ccm\_var_4 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot (transistor\_rise)}{2} \right]}{201} \cdot Fs \end{bmatrix}$$

Conduction losses in the MOSFET:

$$Pq\_ccm\_rms\_var := \begin{bmatrix} (Iq\_rms\_ccm\_var_0)^2 \cdot Rdson \\ (Iq\_rms\_ccm\_var_1)^2 \cdot Rdson \\ (Iq\_rms\_ccm\_var_2)^2 \cdot Rdson \\ (Iq\_rms\_ccm\_var_3)^2 \cdot Rdson \\ (Iq\_rms\_ccm\_var_4)^2 \cdot Rdson \end{bmatrix}$$

Diode conduction losses:

$$\text{Pdiode\_ccm\_var} := \begin{bmatrix} \dfrac{\sum_{i=0}^{200}\left[\left(\text{IL\_pk\_ccm\_var}_0\cdot\left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot\text{VFF}\cdot(1-D_i)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(\text{IL\_pk\_ccm\_var}_1\cdot\left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot\text{VFF}\cdot(1-D_i)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(\text{IL\_pk\_ccm\_var}_2\cdot\left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot\text{VFF}\cdot(1-D_i)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(\text{IL\_pk\_ccm\_var}_3\cdot\left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot\text{VFF}\cdot(1-D_i)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(\text{IL\_pk\_ccm\_var}_4\cdot\left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot\text{VFF}\cdot(1-D_i)\right]}{201} \end{bmatrix}$$

Diode bridge conduction losses:

$$Pdiodebridge\_ccm\_var := \begin{bmatrix} \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_ccm\_var_0 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_ccm\_var_1 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_ccm\_var_2 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_ccm\_var_3 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_ccm\_var_4 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \end{bmatrix}$$

$$P1 := Prr\_ccm\_var + Pq\_ccm\_turnoff\_var + Pq\_ccm\_turnon\_var$$

$$P2 := Pq\_ccm\_rms\_var + Pdiode\_ccm\_var + Pdiodebridge\_ccm\_var$$

$$P\_loss\_semi\_ccm\_var := P1 + P2$$

$$P\_loss\_semi\_ccm\_var = \begin{pmatrix} 11.176 \\ 24.342 \\ 40.784 \\ 60.5 \\ 83.491 \end{pmatrix}$$

Calculate losses in the CRM boost.

Let the average Fs for CRM operation be 80kHz.

$$Fs\_crm := 80 \cdot k$$

Losses in MOSFET due to turn-off overlap of voltage and current:

$$Pq\_crm\_turnoff\_var := \left[\begin{array}{l} \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_pk\_crm\_var_0 \cdot \left| \sin\left(i \cdot \dfrac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs\_crm \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_pk\_crm\_var_1 \cdot \left| \sin\left(i \cdot \dfrac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs\_crm \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_pk\_crm\_var_2 \cdot \left| \sin\left(i \cdot \dfrac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs\_crm \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_pk\_crm\_var_3 \cdot \left| \sin\left(i \cdot \dfrac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs\_crm \\ \dfrac{\sum_{i=0}^{200} Vout \cdot \left[\dfrac{\left(IL\_pk\_crm\_var_4 \cdot \left| \sin\left(i \cdot \dfrac{\pi}{200} \right) \right| \right) \cdot (transistor\_fall)}{2} \right]}{201} \cdot Fs\_crm \end{array} \right]$$

MOSFET conduction losses:

$$Pq\_crm\_rms\_var := \left[\begin{array}{l} (Iq\_rms\_crm\_var_0)^2 \cdot Rdson \\ (Iq\_rms\_crm\_var_1)^2 \cdot Rdson \\ (Iq\_rms\_crm\_var_2)^2 \cdot Rdson \\ (Iq\_rms\_crm\_var_3)^2 \cdot Rdson \\ (Iq\_rms\_crm\_var_4)^2 \cdot Rdson \end{array} \right]$$

Diode conduction losses:

$$\text{Pdiode\_crm\_var} := \left[\begin{array}{l} \dfrac{\sum_{i=0}^{200} \left[\left(\text{IL\_pk\_crm\_var}_0 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot \text{VFF} \cdot (1 - D_i) \right]}{201} \\ \dfrac{\sum_{i=0}^{200} \left[\left(\text{IL\_pk\_crm\_var}_1 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot \text{VFF} \cdot (1 - D_i) \right]}{201} \\ \dfrac{\sum_{i=0}^{200} \left[\left(\text{IL\_pk\_crm\_var}_2 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot \text{VFF} \cdot (1 - D_i) \right]}{201} \\ \dfrac{\sum_{i=0}^{200} \left[\left(\text{IL\_pk\_crm\_var}_3 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot \text{VFF} \cdot (1 - D_i) \right]}{201} \\ \dfrac{\sum_{i=0}^{200} \left[\left(\text{IL\_pk\_crm\_var}_4 \cdot \left| \sin\left(i \cdot \frac{\pi}{200} \right) \right| \right) \cdot \text{VFF} \cdot (1 - D_i) \right]}{201} \end{array} \right]$$

Bridge diode conduction losses:

$$Pdiodebridge\_crm\_var := \begin{bmatrix} \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_crm\_var_0 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_crm\_var_1 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_crm\_var_2 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_crm\_var_3 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \\ \dfrac{\sum_{i=0}^{200}\left[\left(IL\_pk\_crm\_var_4 \cdot \left|\sin\left(i\cdot\frac{\pi}{200}\right)\right|\right)\cdot VFF\cdot(2)\right]}{201} \end{bmatrix}$$

Total semiconductor losses in CRM:

$$P3 := Pq\_crm\_turnoff\_var + Pq\_crm\_rms\_var$$

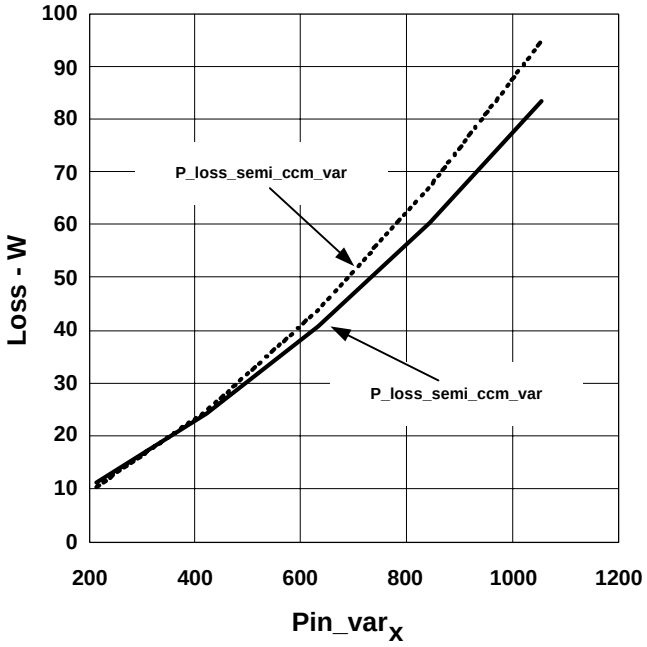
$$P4 := Pdiode\_crm\_var + Pdiodebridge\_crm\_var$$

$$P\_loss\_semi\_crm\_var := P3 + P4$$

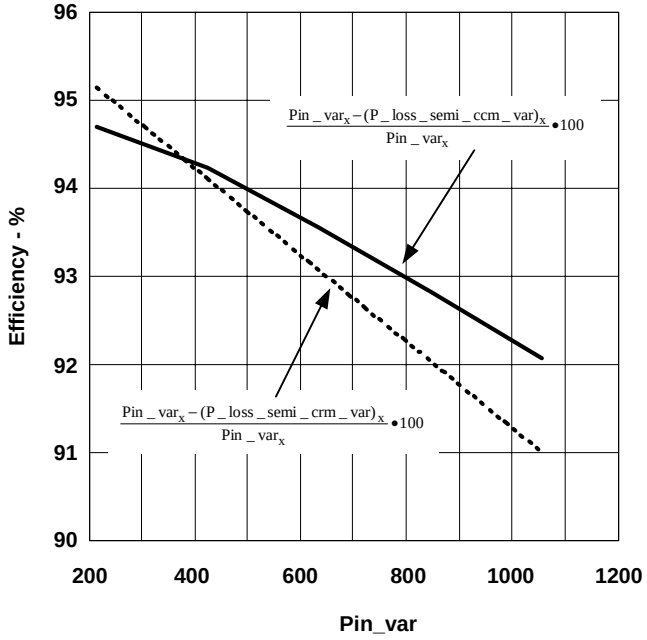
$$P\_loss\_semi\_crm\_var = \begin{pmatrix} 10.238 \\ 24.843 \\ 43.814 \\ 67.15 \\ 94.853 \end{pmatrix} \qquad P\_loss\_semi\_ccm\_var = \begin{pmatrix} 11.176 \\ 24.342 \\ 40.784 \\ 60.5 \\ 83.491 \end{pmatrix}$$

for Fs_crm = 80kHz

This plot compares the semiconductor losses for CCM vs. CRM as a function of input power.



Efficiency comparison of CCM vs. CRM as a function of input power.



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