Analysis, Design, and Experimental Results of a 1-kW ZVS-FB-PWM Converter Employing Magamp Secondary-Side Control

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***Abstract*— The design and breadboard implementation of a constant-frequency, zero-voltage-switched, full-bridge pulsewidth modulation converter delivering a 12-V-at-1-kW output from a 350–450-Vdc input bus is described. The zero-voltage switching characteristic is maintained over a wide operating range by utilizing the transformer magnetizing inductance as an energy storage element. Output voltage regulation is accomplished entirely on the secondary side through magamp control, thus simplifying the methods used for maintaining control and isolation.**

***Index Terms*— Full-bridge pulsewidth modulation converter, magamps, zero-voltage switching.**

I. Introduction

TRADITIONAL methods utilized to achieve zero-voltage switching (ZVS) in full-bridge (FB) constant-frequency pulsewidth modulation (PWM) converters typically rely upon either the energy stored in the isolation transformer leakage inductance and/or the inclusion of a resonant inductor in series with the transformer to act as a supplemental energy storage element. This stored energy is used to charge and discharge bridge switch capacitance during a freewheeling stage created by phase shifting the "on" times of opposite pairs of transistors in the bridge configuration. Assuming sufficient energy storage, the body diode of the switch is forced into conduction before that particular device is turned on, enabling lossless switching. A drawback to this approach is the dependency of the ZVS characteristic on load current. As the required output power decreases, ZVS is lost because not enough energy is stored in the resonant inductor to complete a charge/discharge cycle before device switching occurs [1].

A possible way of minimizing the ZVS load dependency is to utilize the energy stored in the isolation transformer magnetizing inductance, which is independent of the load current. However, in normal operation, the magnetizing current becomes available to the bridge switches only when the reflected load current has decreased to the point where it is less than the magnetizing current. The difference is then available to charge and discharge the switch capacitances and enable ZVS. This difference may or may not be large enough to achieve ZVS, however, by gapping the transformer the useful ZVS range can be increased at light load at the expense of increasing the circulating energy in the converter [2]–[4].

From the standpoint of achieving ZVS by utilizing the magnetizing energy, a more load-independent situation for ZVS can be created by incorporating some form of switching action in the converter secondary [5], [6]. In this scenario, secondary switches are used to prevent the magnetizing current from exiting the primary through the secondary. Consequently, all the magnetizing energy is available for capacitor charge and discharge. No external energy storage element or gapping of the transformer is necessary, and ZVS is obtained through the use of a minimum amount of circulating energy.

In addition to achieving a load-independent ZVS characteristic, the use of controlled switching in the secondary makes secondary-side output voltage regulation and control very attractive. Secondary-side control offers several advantages over its primary-side counterpart, including greatly simplifying the circuit implementation necessary to maintain primary/secondary isolation.

This paper describes the design and experimental evaluation of a 100-kHz 1-kW FB ZVS PWM converter employing secondary-side magamp control. The magamp control enables ZVS to be maintained above about 10% of full load, utilizing just the isolation transformer leakage and magnetizing inductances while simultaneously providing output voltage regulation. As a result of secondary regulation, the primary is switched in an open-loop fashion using constant-frequency constant-phase-shifted PWM.

II. Theory of Operation

As a point of reference, the basic operation of a PWM phase-shifted FB converter employing secondary-side switching is illustrated in Fig. 1. The switches on the same leg of the bridge are switched with a 50% duty cycle and 180° out of phase. The switching time for one leg is then phase shifted relative to the other. In the absence of the secondary-side switches, *S5* and *S6* (i.e., they are replaced with rectifiers), controlling the bridge phase shift (ϕ) varies the volt-seconds applied to the output inductor and, hence, the resulting dc output voltage V_o. However, by incorporating *S5* and *S6* and

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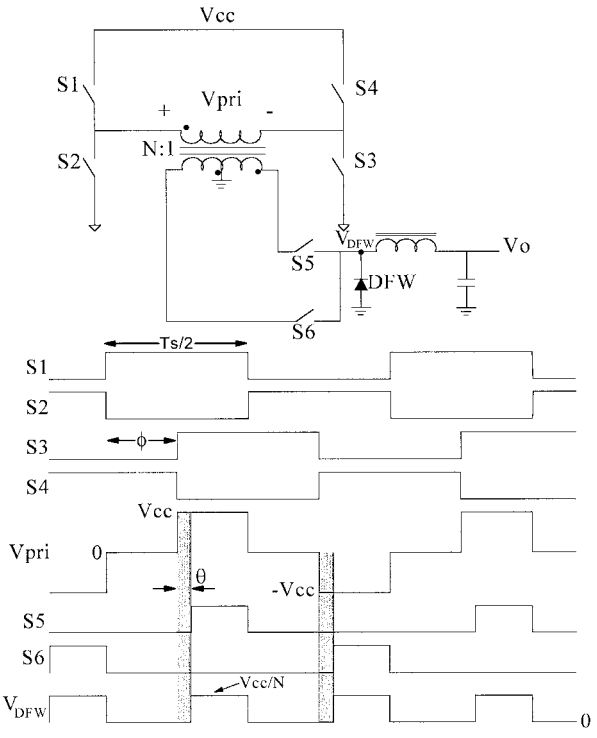


Fig. 1. PWM phase-shifted FB converter with secondary-side control.

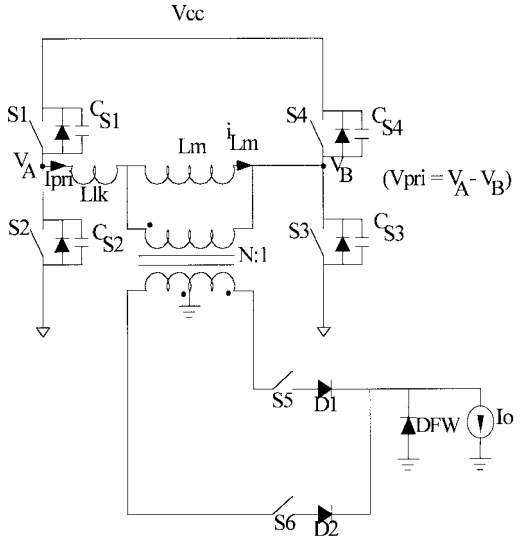


Fig. 2. Idealized ZVS-FB schematic with secondary-side switches.

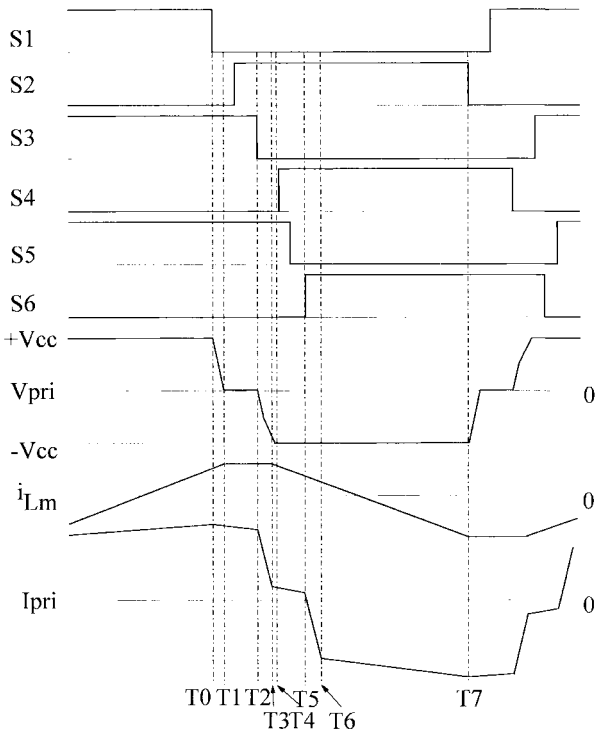


Fig. 3. Idealized ZVS-FB key waveforms.

modulating their turn-on time relative to the bridge switching cycle (θ, the shaded regions shown in Fig. 1), the volts-seconds applied to the output inductor can also be varied to maintain output voltage regulation. In this case, the bridge can be switched with constant phase shift (duty cycle) and the output voltage regulation be accomplished completely on the secondary. The range of regulation is determined by the input voltage, transformer turns ratio, and output voltage. Since the secondary-side switches can only remove volt-seconds from the output inductor, for a given turns ratio and desired output voltage the minimum input voltage is then determined. Similarly, the maximum input voltage is limited by the maximum volt-seconds *S5* and *S6* can block (all else being equal).

Switches *S5* and *S6* also enable the isolation transformer's magnetizing inductance to extend the useful range for ZVS of the bridge switches. To illustrate this, Fig. 2 shows a simplified schematic of an FB ZVS topology incorporating secondary switching (*S5* and *S6*). The isolation transformer is shown with its leakage and magnetizing inductances reflected to the primary. For the purposes of simplifying the explanation of converter operation, the output filter inductor is assumed large enough so that it can be replaced by a current source equal in value to the load current. Because of the presence of switches *S5* and *S6*, catch diode *DFW* is necessary to maintain a circulating path for the output inductor current. Fig. 3 shows the key waveforms and Fig. 4 the principle topological states. In Fig. 4, the darker lines in the secondary schematic indicate the load current path. For the description of the topological states, it is assumed the energy stored in the isolation transformer leakage inductance is insufficient to realize ZVS for *S3* and *S4*, but the combination of leakage and magnetizing inductance energy will achieve ZVS for *S3* and *S4*. (In addition, the delay between turn on and turn off of the complementary side switches in the bridge is sufficient to allow for ZVS as well). Considering all switching components to be ideal, the sequence of steady-state topological modes over one-half of a switching cycle is as follows.

T_0–T_1: At T_0, *S1* is turned off with *S3* still on. *D1* and *S5* are conducting the load current while C_{S1} and C_{S2} are being charged and discharged, respectively, by $Io/N+i_{Lm}$. Because

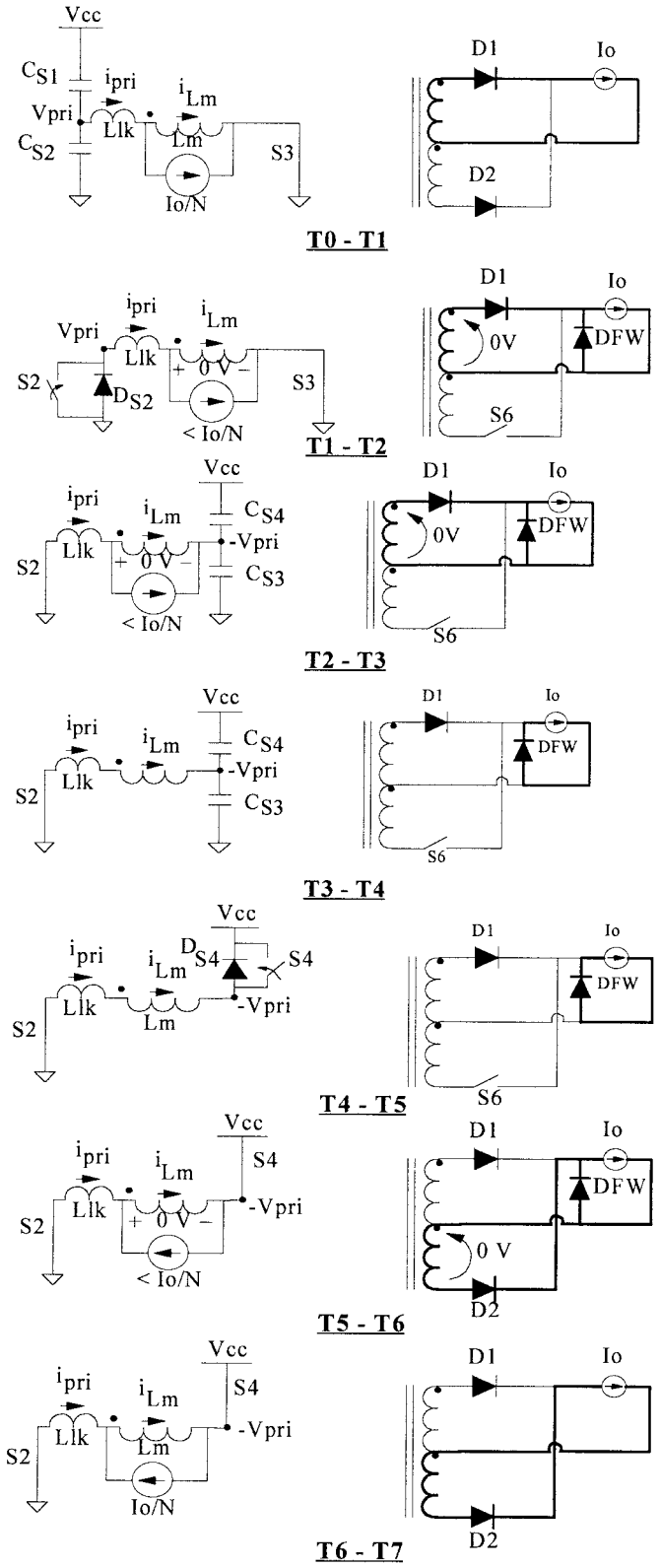


Fig. 4. Idealized ZVS-FB primary and secondary topological states.

the leakage inductance is much smaller than the magnetizing inductance, the decreasing transformer voltage is dropped primarily across the magnetizing inductance. Therefore, the primary current is relatively constant during this transition.

T_1–T_2: At T_1, the body diode of *S2* starts conducting. Since the primary current has decreased to something slightly less than Io/N, the difference on the secondary is picked up by the freewheeling diode *DFW* (*S6* is open). The slope of the primary current remains slightly negative, since, ideally, the voltage across the magnetizing current is clamped to zero by the secondary. Sometime during this interval *S2* can be turned on into 0 V.

T_2–T_3: At T_2, *S3* is turned off. C_{S3} and C_{S4} are charged and discharged, respectively, by the energy stored in the leakage inductance. Because the voltage across the transformer's magnetizing inductance remains clamped at 0 V, the leakage inductance drops all of the decreasing primary voltage. As a result, the primary current decreases very rapidly. On the secondary, the freewheeling diode continues to make up the increasing difference between the reflected primary current and the load current I_o.

T_3–T_4: At T_3, the leakage inductor current has decayed to the point where it is equal in value to the magnetizing current. *D1* unclamps the secondary voltage and all of the load current commutes to the freewheeling diode. Because of the presence of *S6* and the fact that it is open, the (very large) magnetizing inductance is now free to join the resonance with the switch capacitance. In this manner, the useful load range for ZVS is extended below that which could be obtained using only the leakage inductance.

T_4–T_5: At T_4 D_{S4} is forced into conduction and *S4* can then be turned on into 0 V.

T_5–T_6: At T_5, *S6* is closed, allowing *D2* to start conducting. This once again clamps the voltage across the magnetizing inductance to zero and drops the supply voltage across the leakage inductance. The primary current starts decreasing very rapidly. The maximum time delay for the closing of *S6* (i.e., the duration of intervals T_3–T_5) is determined by the volt-seconds required by the output inductor to maintain the desired output voltage. The minimum delay is equal to the duration of the interval between the turn-off of *S3* and the turn-on of S4. A quantitative analysis is given in the Appendix.

T_6–T_7: At T_6, the primary current has decreased to the point where it equals the sum of the reflected load current and the magnetizing current. With *DFW* turning off, *D2* now carries the full load current. During this interval, positive volt-seconds are applied to the output inductor (in the normal manner for a buck converter). At T_7, the cycle is repeated, except with the correspondingly opposite set of bridge transistors.

The presence of the secondary switches not only provides a mechanism through which the ZVS range can be increased, but, as mentioned previously, it provides a convenient means through which output voltage regulation can be accomplished. This can be done by modulating the turn-on time of *S5* and *S6*, which, in turn, varies the applied volt-seconds to the output inductor. The primary advantage of secondary-side regulation is the removal of the need to pass a voltage feedback signal across an isolation barrier. Also, secondary-side control can have the capability to isolate load faults from the primary or, in the case of a multiple output converter, from other outputs (*S5* and *S6* could be left open for the duration of an output short).

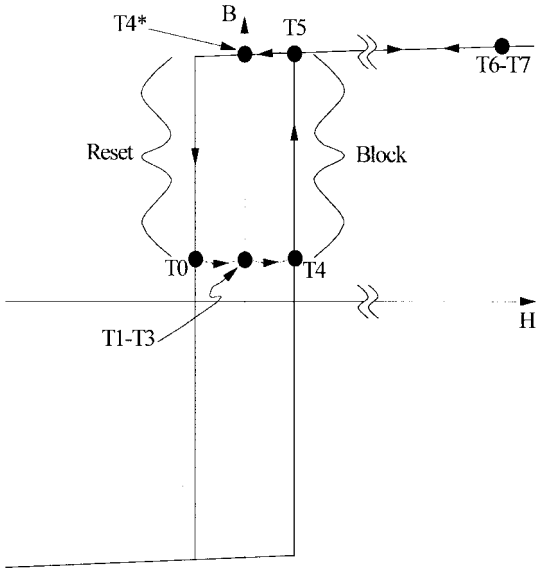


Fig. 5. Square-loop core operation of secondary switch *S6*.

The choice of the type of switch implementation for *S5* and *S6* depends on the application, but, if high output current is required, saturable reactors (magamps) make a good choice. The operation of an ideal square-loop core magamp acting as switch *S6* is illustrated in Fig. 5. The operating point locations shown on the B–H curve in the figure correspond to the topological states outlined in Fig. 4, except for the point marked T_4^*. This is equivalent to the topological state starting at T_4 (as shown in Fig. 4) that occurs during the *opposite* half cycle of bridge operation, i.e., when *D2* is turning off. Reset of *S6* occurs between T_4^* and the turn off of *S1* (which occurs at T_0).

III. Circuit Design

A. Specifications

To provide experimental verification of the operating principles described in the previous section, a 1-kW FB-ZVS-PWM converter was built to the following specifications:

- $V_{\text{in}} = 350$–450 Vdc;
- $V_o = 12$ Vdc at 83 A maximum (P_o max. $= 1$ kW);
- $F_s = 100$ kHz.

The input voltage range was selected to match the output range from a typical off-line power factor correction (PFC) boost converter operating from a universal line input. This would be the case, for example, if the dc/dc converter was operated as a load module in a power distribution system. Because of the high output current required, switches *S5* and *S6* are realized using magamps. Additionally, magamps are well suited for use in this particular application because of the relatively narrow range of input voltage, enabling the use of small cores. One disadvantage to using square-loop core magamps, however, is increased core loss as the switching frequency is increased. The switching frequency of 100 kHz was selected to help minimize this problem.

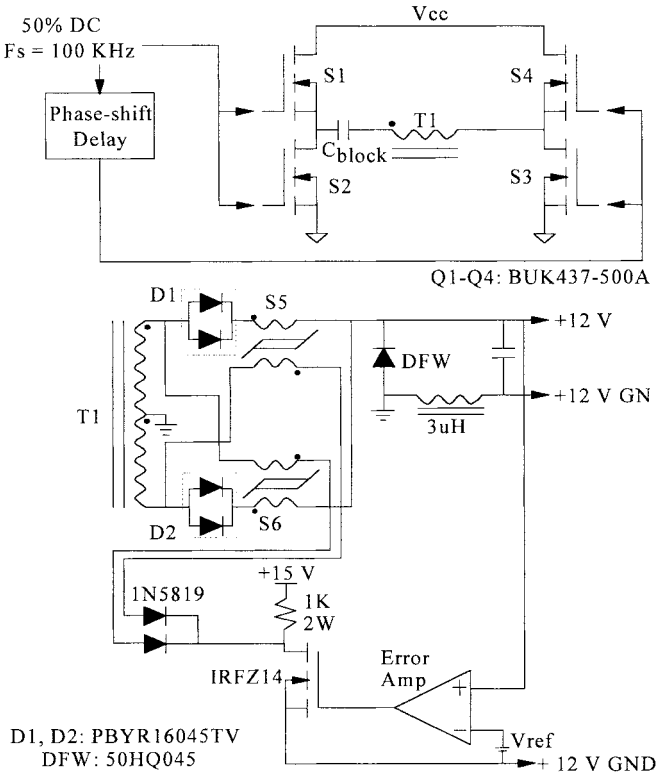


Fig. 6. Simplified schematic of the 1 kW FB-ZVS-PWM converter.

B. Power Stage Design

The simplified schematic for the power stage and primary side control signals is shown in Fig. 6. Except for the magamp portion, the process of selecting the power stage components is identical to that which would be done for a standard phase-shift-controlled FB converter designed to similar power and voltage levels. In the interests of brevity, this is not included in the paper. The isolation transformer (T1) design consists of the following:

1) *core:* Toshiba PC40ETD49-Z;
2) *primary winding:* 22 turns of 7 strands of 26 AWG;
3) *secondary winding:* 1 turn of 4 paralleled sheets of 5 mil $\times$ 1-in wide Cu foil;
4) *winding pattern:* 1/2 primary–secondary—1/2 primary (i.e., interleaved);
5) *magnetizing inductance:* 2.2 mH;
6) *leakage inductance (referred to the primary):* $\sim$4.2 μH.

The transformer was wound with the intent of minimizing leakage inductance and the core was not gapped. Copper foil was used for the secondary winding due to the high output current.

Ideally, for phase-shifted constant-frequency operation, the gate drive signals for the bridge transistors are operated with a 50% duty cycle and transistor pairs are switched 180° out of phase. However, as discussed in Section II, in order to allow the resonant transitions to occur delays are deliberately introduced between the turn-on/turn-off of switches in the same bridge leg. This has the benefit of preventing cross-conduction

problems, but reduces the secondary-side maximum duty cycle (see the Appendix). This delay circuitry is not shown in Fig. 6.

The "phase-shift delay" shown in Fig. 6 is used to introduce a delay in the drive signal of the *S3*, *S4* transistor pair relative to the *S1*, *S2* pair. Since closed-loop control is accomplished entirely on the secondary side, this delay is held constant. Ideally, the delay would be near zero in order to maximize the primary-side duty cycle. However, for experimental purposes, the bridge transistors in the breadboard were switched with a duty cycle of about 85% to more clearly illustrate the converter operation. Also, a high-frequency blocking capacitor is used to keep the volt-seconds on the transformer balanced.

C. Magamp Circuit Design

A simplified version of the secondary-side magamp and control circuitry is also shown in Fig. 6. Because of the physical layout of the secondary, the magamps were placed on the cathode side of the rectifier diodes. This necessitated using the reset scheme shown. The MOSFET pass transistor's "on" resistance is modulated by the control loop, providing the necessary amount of reset voltage to the magamps in order to maintain output voltage regulation. Magamp reset current flows through each output rectifier's *RC* snubber network (not shown in Fig. 6) and the transformer secondary. In the absence of rectifier snubber networks, diode parasitic capacitance can be used to complete the current path. As explained previously, individual core reset can occur only during the opposite half cycles of bridge operation.

Because of the high secondary current, the maximum number of primary turns available for the magamp core is one. This limits somewhat the maximum blocking time available from the core, which is given by

$$t_{\text{block}}(\text{sec}) = \frac{NA_e(B_{\text{sat}} - B_{\text{reset}})}{V_{\text{block}}} \tag{1}$$

where A_e is the core cross section (in m^2), and the flux density B is in tesla. Maximum blocking time occurs at high-line, light load and is about 1.5 μs in this application. The magamp design implemented in the 1 kW breadboard is as follows:

1) *core:* 2× Allied Signal METGLAS #MP1906;
2) *primary winding:* 1 turn of 7 strands of 150/33 AWG Litz wire;
3) *reset winding:* 1 turn of 26 AWG.

To meet the maximum blocking time, two cores were required to realize a single magamp. Maximum core loss can be estimated from [7]

$$P_{\text{core}}(\text{W/kg}) \approx 9.93 \times 10^{-6} \bullet F_s^{1.57} \bullet \left(\frac{B_{\text{sat}} - B_{\text{reset}}}{2}\right)^{1.70} \tag{2}$$

where B is in tesla and F_S is in hertz. This gives a total of about 1.76 W maximum per magamp.

IV. Experimental Results

Transformer primary voltage and current waveforms are shown superimposed in Fig. 7. Operation is at the maximum line and load condition under closed-loop output voltage regulation. ZVS is easily obtained at this operating point, as demonstrated in the oscillogram. With the secondary-side switching, the ZVS range extends down to about 15% of full load (150 W) over the line range. As a comparison, if output voltage regulation is disabled (i.e., the secondary-side duty cycle seen by the output inductor is constant—no closed loop output voltage feedback is utilized) achieving ZVS requires approximately 60% of full-load current. This difference is illustrated in Fig. 8. Both oscillograms show the primary voltage waveform at identical input voltage and load current operating points. In Fig. 8(b), closed-loop control enables the resonant transition to reach the supply voltage as the switch is turned on, while maintaining output voltage regulation. ZVS could be extended to even less load by further delaying *S3*'s turn-on/turn-off time (relative to the turn-off/turn-on time of *S4*, see Fig. 3). However, the effective duty cycle on the secondary is correspondingly reduced, potentially creating problems in obtaining closed-loop regulation during operation at low line, high load. A quantitative discussion is provided in the Appendix. For the breadboard constructed, regulation at full output power was lost when the input voltage dropped below about 360 Vdc.

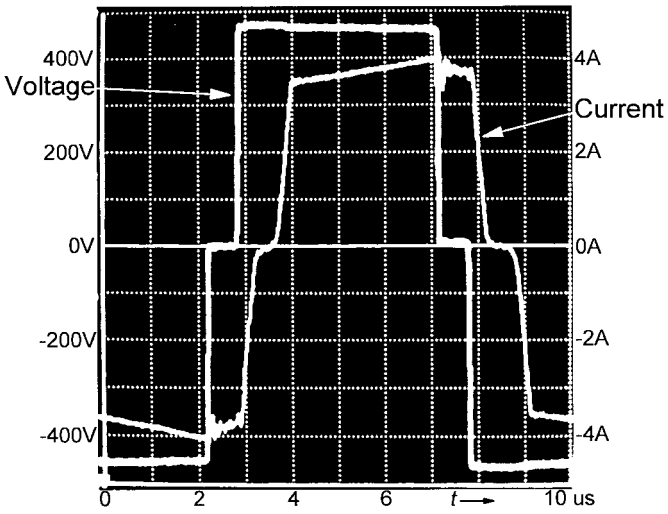
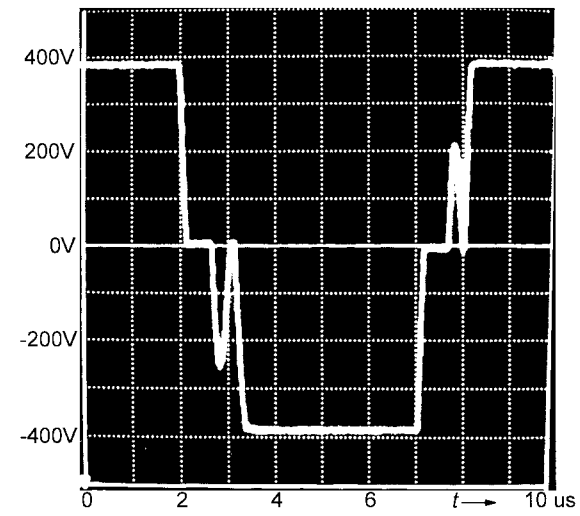
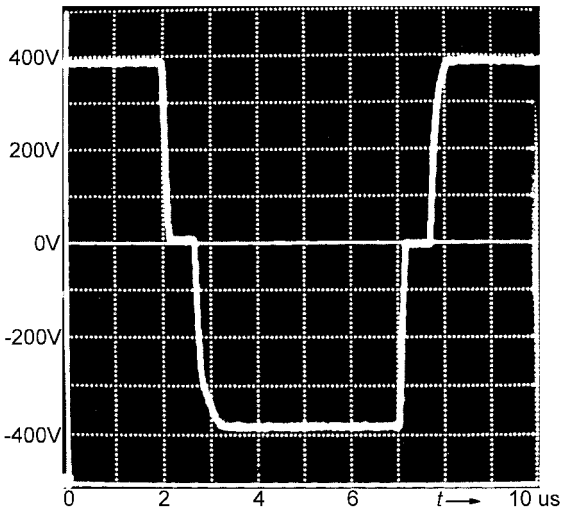


Fig. 7. Transformer primary voltage and current waveforms at $V_{\text{in}} = 450$ Vdc and $P_o = 1$ kW. Time scale is 1 μs/div.

Table I illustrates a comparison between the power dissipation savings incurred due to light-load ZVS of *S3* and *S4* versus the core loss introduced by the magamps used to realize the ZVS mechanism. A load current of 8 A (10% of full load) was used as the point of comparison. The table shows the losses as a function of both supply voltage and switching frequency. For the magamp loss calculations, the induction level (ΔB) was held constant for the three different frequencies (although the volts-seconds required to be blocked increase as the switching frequency is decreased). As is shown in the table, the overall net gain in power dissipation is about break-even until the switching frequency is increased to 200 kHz, at which point the high-line magamp core loss will dominate. However, at 100 kHz and high-line, a significant reduction in *S3*/*S4*



(a)



(b)

Fig. 8. Transformer primary voltage at $V_{\text{in}} = 375$ Vdc and $P_o = 150$ W. (a) "Open loop." (b) "Closed loop." Voltage scale: 100 V/div; current scale: 1 A/div. Time scale is 1 μs/div.

power dissipation can be had by shifting the transistor loss to the magamps. This would typically be desirable from the viewpoint of thermal management and reliability.

Fig. 9 shows experimental efficiencies versus load at different input voltages. The efficiency *decreases* as the input voltage increases (the primary is switched with constant duty cycle, leading to increased circulating energy and magamp core loss as the input voltage increases). The disparity becomes more evident at lighter loads where the required volt-seconds to be blocked are greatest. These efficiency measurements do not include the gate drive or magamp control circuitry power dissipations. The measured gate drive power dissipation was about 3 W. Fig. 10 illustrates the required magamp control current as a function of line and load. These curves include both magamp reset currents.

Oscillograms showing the voltages across the output rectifier (*D1*) and magamp (*SR1*) (together with the primary current) are displayed in Figs. 11 and 12. The rectifier voltage is very clean, with no overshoot at all. The exponential-like decay in the rectifier voltage (when the opposite rectifier is conducting) is due to the magamp reset current flowing through the parallel combination of the rectifier parasitic capacitance and *RC* snubber.

TABLE I
LOSS COMPARISON—*S3*/*S4* ZVS VERSUS MAGAMP LOSSES

Fs	Vcc (V)	P_D Savings in S3 and S4 Due to ZVS	Magamp Core Loss Introduced
	450	2.6 W	2.1 W
50 kHz	400	1.9 W	2.1 W
	350	1.35 W	0.5 W
	450	5.2 W	6.2W
100 kHz	400	3.8 W	3.2 W
	350	2.7 W	1.5 W
	450	10.4 W	18.4 W
200 kHz	400	7.6 W	9.5 W
	350	5.4 W	4.4 W

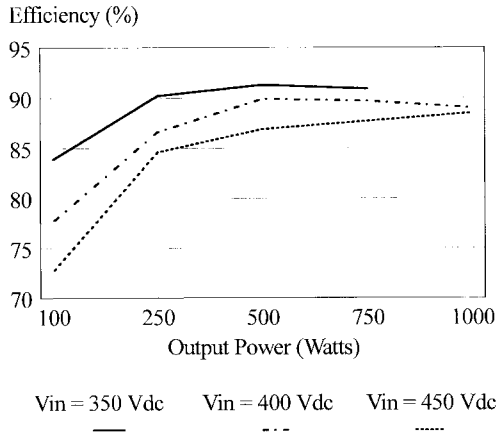


Fig. 9. Experimental efficiencies versus output power.

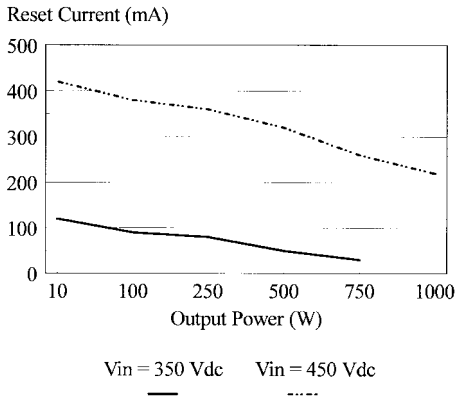


Fig. 10. Magamp reset current as a function of load and input voltage.

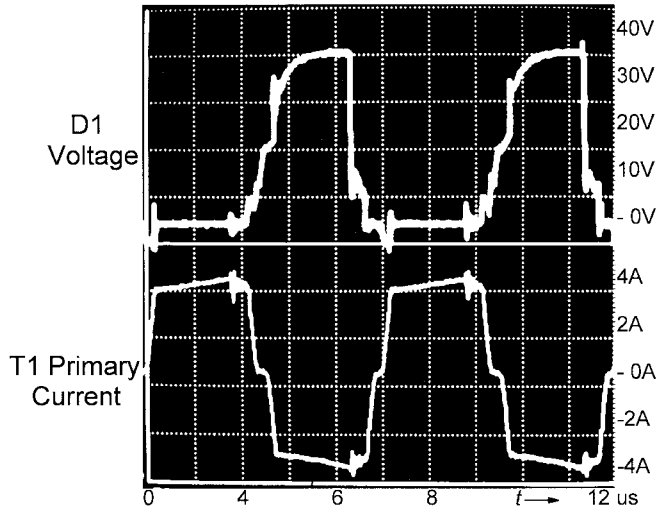


Fig. 11. Output rectifier *D1* voltage and transformer primary current at $V_{\rm in} = 450$ V, $P_o = 1$ kW. Voltage scale: 10 V/div; current scale: 2 A/div; time scale: 2 μs/div.

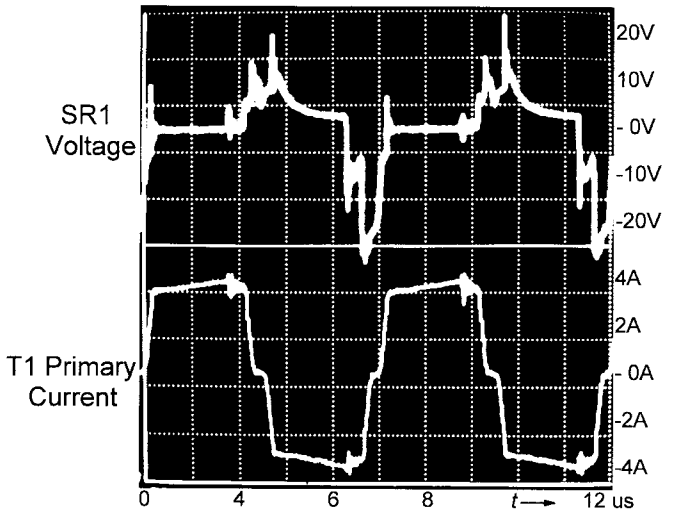


Fig. 12. Magamp *SR1* voltage and transformer primary current at $V_{\rm in} = 450$ V, $P_o = 1$ kW. Voltage scale: 10 V/div; current scale: 2 A/div; time scale: 2 μs/div.

V. Summary

This paper has described the analysis, design, and experimental results of a 100-kHz 1-kW FB ZVS PWM converter incorporating secondary-side control. Operation is from a 350–450-Vdc input with a 12-Vdc output. Utilization of secondary-side switching accomplishes two important tasks: 1) extending the useful load range for ZVS by enabling the transformer magnetizing inductance to join the resonance between the leakage inductance and the bridge switch capacitance and 2) providing output voltage regulation for the secondary. For a low voltage, high current output magamps are the preferred choice for realizing the secondary switches.

Experimental results demonstrate the range of ZVS is extended from about 60% of full load without secondary switching to about 15% of full load when operating under closed-loop control (a factor of four improvement). Isolation transformer design is done to minimize leakage effects, and it was not necessary to add any external resonant inductor in the primary. Experimental efficiencies between 85%–91% were obtained above an output power of about 250 W.

Appendix

This appendix derives the conditions required to achieve ZVS by utilizing the energy stored in the isolation transformer magnetizing inductance (L_m). To simplify the analysis, the following assumptions are made (refer to Figs. 1–4).

- $\phi \rightarrow 0$ (i.e., the primary side duty cycle approaches 100%).
- The delay between turn on/turn off of switches on the same bridge leg is small compared to $Ts/2$.
- $L_{lk} \ll L_m$.
- The energy stored in the leakage inductance (L_{lk}) is insufficient by itself to realize ZVS.

First, for ZVS to be realized utilizing the energy stored in the magnetizing inductance, the following inequality must be satisfied:

$$\begin{aligned} \tfrac{1}{2} L_m i_{Lm}^2 \big|_{\rm S3\,or\,S4\,turn\text{-}off} &\geq \frac{1}{2}\left(\tfrac{8}{3} C_{oss}\right) V_{cc}^2 + \tfrac{1}{2} C_{xfmr} V_{cc}^2 \\ &= \frac{1}{2} C_{eq} V_{cc}^2 \end{aligned} \tag{A1}$$

where $C_{eq} = (8/3)C_{oss} + C_{xfmr}$. C_{oss} is the value of MOSFET output capacitance determined at a drain-to-source voltage of V_{cc} and C_{xfmr} is the isolation transformer's winding capacitance. The factor of 8/3 results from the fact that the value of output capacitance is a nonlinear function of the MOSFET drain-to-source voltage [1], [4], [8]. At the point where *S3* or *S4* turns off, the magnetizing current is given by

$$i_{Lm} = \frac{V_{cc} T_s}{4 L_m} \tag{A2}$$

where T_s is the switching period for the bridge switches. Solving (A1) and (A2) for L_m yields

$$L_m \leq \frac{T_s^2}{16 C_{eq}}. \tag{A3}$$

For the power stage design described in Section III, $C_{eq} \approx 400$ pF, resulting in a maximum magnetizing inductance of 15.6 mH, significantly greater than the 2.2-mH value used in the design.

For ZVS, in addition to the constraint required by (A1), the duration of the T_3–T_4 interval must be of sufficient length to allow the resonance of L_m and C_{eq} to reach the point where V_B (see Fig. 2) equals V_{cc} or ground. If *S3* or *S4* is turned on before the T_3–T_4 interval is completed, ZVS is lost. The duration of the interval is dependent on the value of V_B at T_3, and this, in turn, is dependent on the energy stored in L_{lk}

and the duration of the T_2–T_3 interval. The T_2–T_3 interval terminates when the current in the leakage inductance decays to the point where it equals the magnetizing current. During this interval, the voltage at V_B is given by

$$V_B(t)|_{T_2-T_3\ \text{interval}} = \left(\frac{I_o}{N} + \frac{V_{cc}T_s}{4L_m}\right)\sqrt{\frac{L_{lk}}{C_{eq}}}\ \sin\ \frac{t}{\sqrt{L_{lk}C_{eq}}}. \tag{A4}$$

The current in the leakage inductance during this interval is then

$$i_{Llk}(t)|_{T_2-T_3\ \text{interval}} = \left(\frac{I_o}{N} + \frac{V_{cc}T_s}{4L_m}\right)\ \cos\ \frac{t}{\sqrt{L_{lk}C_{eq}}}. \tag{A5}$$

Therefore, the duration of the T_2–T_3 interval is

$$\Delta(T_2\text{–}T_3) = \sqrt{L_{lk}C_{eq}}\ \cos^{-1}\ \frac{NV_{cc}T_s}{4L_mI_o + NV_{cc}T_s}. \tag{A6}$$

The value of V_B at T_3 is then

$$V_B|_{T_3} = \left(\frac{I_o}{N} + \frac{V_{cc}T_s}{4L_m}\right)\sqrt{\frac{L_{lk}}{C_{eq}}} \cdot \sin\left[\cos^{-1}\left(\frac{NV_{cc}T_s}{4L_mI_o + NV_{cc}Ts}\right)\right]. \tag{A7}$$

For the T_3–T_4 interval, the magnetizing inductance is free to resonate with C_{eq} . Therefore,

$$V_B(t)|_{T_3-T_4\ \text{interval}} = V_B|_{T_3} + \frac{V_{cc}T_s}{4L_m}\sqrt{\frac{L_m}{C_{eq}}}\ \sin\ \frac{t}{\sqrt{L_mC_{eq}}}. \tag{A8}$$

For ZVS, $V_B = V_{cc}$ and this marks the completion of the T_3–T_4 interval. The duration of the T_3–T_4 interval is then given by

$$\Delta(T_3\text{–}T_4) = \sqrt{L_mC_{eq}}\ \sin^{-1}\left(\frac{V_{cc} - V_B|_{T_3}}{\frac{V_{cc}T_s}{4L_m}\sqrt{\frac{L_m}{C_{eq}}}}\right). \tag{A9}$$

Equations (A3) and (A9) serve to define the conditions for achieving ZVS using the magnetizing inductance.

The total duration of intervals T_2–T_3 and T_3–T_4 also serves to set an upper limit on the conversion ratio by limiting the maximum duty cycle seen by the secondary. In particular, during the T_3–T_4 interval, the freewheeling diode (*DFW*, see Fig. 4) is conducting the output inductor current, so the longer the duration of this interval, the greater the loss of secondary-side volt-seconds that could otherwise have been applied to the inductor. Of course, this assumes *S6* (*S5*) was being controlled such that it would be turned on simultaneously with the turn-on of *S4* (*S3*) (i.e., the controller is commanding maximum output voltage). Practically speaking, a tradeoff would normally need to be made with respect to the ZVS range and the maximum conversion ratio.

Under the assumptions outlined above, defining Δ to be the sum of the durations of the T_2–T_3 and T_3–T_4 intervals (A6 and A9), the maximum conversion ratio is

$$\left.\frac{V_o}{V_{cc}}\right|_{\max} = \frac{1 - \frac{2\Delta}{T_s}}{N}. \tag{A10}$$

The minimum conversion ratio is determined by the maximum blocking time of *S5* and *S6*

$$\left.\frac{V_o}{V_{cc}}\right|_{\min} = \frac{1 - \frac{2(\Delta + t_{\text{block, max}})}{T_s}}{N}. \tag{A11}$$

The maximum blocking time of *S5* and *S6*, $t_{\text{block, max}}$, is obtained from (1)

$$t_{\text{block, max}}(\text{sec}) = \frac{NA_e(2B_{\text{sat}})}{V_{\text{block}}}. \tag{A12}$$

REFERENCES

[1] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. Applied Power Electronics Conf.*, 1990, pp. 275–284.

[2] R. A. Fisher, K. D. T. Ngo, and M. H. Kuo, "A 500 kHz, 250 W dc–dc converter with multiple outputs controlled by phase-shifted PWM and magnetic amplifiers," in *Proc. High Frequency Power Conversion Conf.*, 1988, pp. 100–110.

[3] D. M. Sable and F. C. Lee, "The operation of a full-bridge, zero-voltage-switched, PWM converter," in *Proc. VPEC Power Electronics Seminar*, 1989, pp. 92–97.

[4] L. H. Mweene, C. A. Wright, and M. F. Schlecht, "A 1 kW, 500 kHz front-end converter for a distributed power supply system," in *Proc. Applied Power Electronics Conf.*, 1989, pp. 423–432.

[5] R. Farrington, M. M. Jovanovic, and F. C. Lee, "A new family of isolated zero-voltage-switched converters," in *Proc. Power Electronics Specialists Conf.*, 1991, pp. 209–215.

[6] G. Hua, F. C. Lee, and M. M. Jovanovic, "An improved zero-voltage-switched PWM converter using a saturable inductor," in *Proc. Power Electronics Specialists Conf.*, 1991, pp. 189–194.

[7] *Design of High Frequency Mag Amp Regulators Using METGLAS Amorphous Alloy 2714A*, Allied-Signal Company, Parsippany, NJ, 1991.

[8] W. Chen, F. C. Lee, M. M. Jovanovic, and J. A. Sabate, "A comparative study of a class of full bridge zero-voltage-switched PWM converters," in *Proc. Applied Power Electronics Conf.*, 1995, pp. 893–899.

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