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IPC-SM-785

Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

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November 1992 A guideline developed by IPC

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Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

Developed by the SMT Accelerated Reliability Test Task Group of the Product Reliability Committee of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the SMT Accelerated Reliability Test Task Group of the IPC Product Reliability Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

1.0 SCOPE

This document provides guidelines for accelerated reliability testing of surface mount solder attachments and for evaluating and extrapolating the results of these accelerated reliability tests towards actual use environments of electronic assemblies. Background and design information is provided for an understanding of the accelerated test issues.

1.1 Purpose The purpose of accelerated reliability testing is to provide confidence that the design and the manufacturing/assembly processes are capable of meeting the intended goals of product performance. These guidelines provide adequate commonality and validity for accelerated reliability tests:

- To allow comparison of results from different test programs
- To provide the generic technical understanding of the underlying issues necessary to the design for adequate reliability
- To permit the analytical prediction of reliability based on a generic database and technical understanding
- To reduce cost and avoid time-consuming testing of every design iteration
- To establish practical alternatives to replace the excessively long test durations necessary to verify reliability of products subject to severe use environments or low failure tolerances

1.2 Document Organization This document has been organized to provide the reader with consistent information on the various aspects of reliability and identifies the parameters that need to be addressed. Each section serves a specific function in the reliability description chain. Where appropriate, references are provided as to where additional information may be obtained.

- *Section 3, "Requirements"*
  This section provides an overview of the concepts of reliability and all of the characteristics that need to be considered in the validation of a product design. Included are the definitions of the appropriate terms, as well as generic models for fatigue life and failure probability, manufacturing process flow, use environments, and testing methodology.
- *Section 4, "Surface Mount Solder Attachment Fatigue Behavior and Prediction"*
  This section deals with the fatigue life models for solder joints including their behavior when subjected to multiple cyclic loads during large temperature excursions or high frequency cycles at low temperatures. Also discussed are the acceleration factors, the acceleration transforms, and statistical considerations.
- *Section 5, "Design for Solder Joint Reliability"*
  This section details the various design parameters that have a primary influence on solder attachment fatigue reliability. All aspects of the solder joint formation are addressed including component size, lead stiffness, coefficient of thermal expansion, solder joint uniformity, as well as solder composition, grain structure and the value that conformal coating or compliant layers provide to the attachment system.
- *Section 6, "Manufacturing Processes"*
  This section provides the relationship between the assembly and attachment processes, including their control and verification, and the resultant defects or potential defects from the original processes or touch-up, rework or repair actions. Material properties of solder (including volume), components, printed boards, adhesives and conformal coatings are discussed as to their interrelationships and the impact that these characteristics have on the manufacturing processes.
- *Section 7, "Accelerated Reliability Testing"*
  This section deals with the goals of accelerated testing to produce a failure in the shortest time using techniques intended to simulate the use environment in order to establish the appropriate confidence level of product performance. Various types of stress cycling are reviewed and correlated to damage mechanisms. Also discussed is the need for developing a strategy which includes a test plan, sampling methodology, test vehicles, and failure mode analysis.
- *Appendix A, "Step-by-Step Example"*
  This section shows illustrations of applying the principles detailed in the information provided in this publication. Numerical examples are provided that highlight the relationship of the various parameters.
- *Appendix B, "References"*
  This section provides reference to published information that has a bearing on solder joint reliability and is referenced in the body of the text of this document. Details are shown as to Title, Author, and Publisher.
- *Appendix C, "Bibliography"*
  This section provides references to additional published information that could be of use to the practitioner. The references are organized into three major topics

1) Accelerated Life Testing
2) Solder Joint Metallurgy and Etching
3) Vibration and Shock.

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue currently in effect, form a part of this specification to the extent specified herein.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-PC-90 General Requirements for Implementation of Statistical Process Control

IPC-TM-650 Test Methods Manual

IPC-ET-652 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-R-700 Suggested Guidelines for Modification, Rework, and Repair of Printed Boards and Assemblies

IPC-TA-720 Technology Assessment of Laminates

IPC-SM-782 Surface Mount Land Patterns (Configurations and Design Rules)

IPC-SM-786 Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages

IPC-MS-810 Guidelines for High Volume Microsection

IPC-S-816 SMT Process Guideline & Checklist

2.2 Joint Industry Standards[1]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

2.3 Military

MIL-HDBK-217

MIL-STD-810

2.4 Other Publications

American Society for Testing and Materials

ASTM E340-68 Standard Methods for Macroetching Metals and Alloys

ASTM E407-70 Standard Methods for Microetching Metal and Alloys

International Tin Research Institute

ITRI Pub #580 Metallography of Tin and Tin Alloys

ITRI Pub #708 Metallurgy of Solder Joints in Electronics

3.0 REQUIREMENTS

The reliability of the solder joint attachment of electronic components surface mounted to circuit board substrates requires explicit attention in the design phase, as well as during manufacturing. During use, surface mount (SM) solder joints can be subjected to a variety of loading conditions which can lead to premature failure if inadequately designed. The following loading conditions could exist either singly, sequentially or simultaneously:

a) cyclic differential thermal expansion,

b) vibration (transport),

c) thermal shock (rapid temperature change causing transient differential warpages) during cooling from soldering operation or from severe use environments,

d) mechanical shock (high acceleration) from severe use conditions or accidental misuse.

While vibration, thermal shock and mechanical shock are possible in practical applications, they are the exceptions rather than the norm; the failure mechanism of primary concern for SM solder joint reliability is cyclic differential thermal expansion/contraction causing fatigue damage. It should be noted that the resistance against failures induced by vibration fatigue, thermal shock and mechanical shock depends primarily on solder joint strength; this is not the case, however, for thermal fatigue failure resistance.

These thermal expansion differences result from changing temperatures due to power dissipation internal to the component and differences in the coefficients of thermal expansion (CTE) in combination with system internal or external temperature variations caused by component or system load fluctuations or on/off cycles, by diurnal cycles, or by seasonal changes. During operation, SM solder joints can be subjected to considerable cyclic strains caused by different thermal expansions of:

1. The surface mounted components and the substrates to which they are solder-attached.

2. The solder and the materials (component, lead, substrate) to which it is bonded.

To ascertain that the solder joint attachment of SM circuit assemblies meet reliability expectations in their intended use environments, it is necessary to produce a generic reliability data base using accelerated fatigue tests and to confirm the reliability for some specific applications. Because

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of the time dependent creep and stress relaxation properties of solder, the cyclic damage and the fatigue life in accelerated testing are not generally equivalent to those in operational use. Thus, to utilize the results from accelerated fatigue tests, an acceleration transform is necessary. This allows valid comparisons of results from different accelerated test conditions and more importantly, allows the extrapolation of these accelerated test results to predict the reliability of the product in use.

3.1 Terms and Definitions Terms and definitions used herein are in accordance with IPC-T-50, except as otherwise specified.

Note: Any definition denoted with an asterisk (*) is a reprint of the definitions in IPC-T-50.

3.1.1 Accelerated Reliability Test A test in which the damage mechanism(s) of concern for operational use is (are) accelerated to cause failures in less time than in service. The test acceleration results from shorter cycle periods and/or more severe loading conditions; however, the introduction of extraneous damage mechanisms must be avoided. The service life can be characterized by application of appropriate acceleration factors or transforms.

3.1.2 Acceptable Cumulative Failure Probability Maximum percentage of defectives/failures at the end of the service life within acceptable limit.

3.1.3 Bathtub Curve Methodology for quantifying reliability when the failure rate is plotted against time. The result often follows a pattern of failure known as a bathtub curve. Three periods are apparent. These periods differ in the frequency of failure and in the failure causation pattern.

3.1.4 Burn-In Test A test in which finished product is routinely subjected to normal, perhaps worst-case but still realistic, operational environments. In purpose it resembles the shakedown cruise of a ship. Burn-in is not an accelerated reliability test.

3.1.5 Creep The time-dependent visco-plastic deformation as a function of applied stress.

3.1.6 Coffin-Manson Model A predictive model which relates the number of cycles to failure to the applied plastic strain.

3.1.7 Cyclic Differential Expansion Expansion differences developed due to the differences in coefficients of thermal expansion and cyclic temperature changes during operational use or temperature cycling tests.

3.1.8 Cyclic Temperature Range/Swing Temperature amplitude between maximum and minimum temperatures occurring in operational service cycles or temperature cycling tests.

3.1.9 Design Service Life Fully functional duration of operation of a piece of equipment which is exposed to expected environment conditions.

3.1.10 Environmental Stress Screening (ESS) A screening procedure employing environmentally generated stresses to cause overstressing of 'weak' elements of an assembly to the point of failure to prevent these latent defects from reaching field service and possibly causing field failures. The environments producing these stresses may, or may not, be related to environmental conditions experienced by the product during service. Once having failed, the elements can be detected and either repaired, replaced, or discarded; and perhaps redesigned for future product. ESS needs to be accomplished without significant damage to the 'normal' elements of the assembly. ESS is not an accelerated reliability test.

3.1.11 Expected Design Life Life intended for a product by its designer.

3.1.12 Fatigue Ductility Exponent Exponent used in the Coffin-Manson low-cycle fatigue model to define the characteristic slope of the curve defining cyclic life versus cyclic visco-plastic strain energy.

3.1.13 Highly Accelerated Stress Testing (HAST) A stress test used to simulate corrosion related failures mechanisms under electrical bias while subjected to an accelerated stress combination of temperature and humidity. HAST may be used in the context of components and assemblies, but is not an accelerated reliability test for solder attachment.

3.1.14 Hysteresis Loop A diagram of the stress-strain behavior of solder joints obtained during a loading cycle from zero to a positive maximum, to zero to a negative maximum, and back to zero—the area of the hysteresis loop is a measure of the fatigue damage per cycle.

3.1.15 Infant Mortality Failure during burn-in, initial functional testing, and/or early in service associated primarily with manufacturing process or quality related problems.

3.1.16 Limp Home Capability Ability of equipment to function at a minimum level despite limited internal functional failures.

3.1.17 Manson-Coffin Plot A graphic representation which relates the number of cycles to failure to the applied plastic strain for both plastic and elastic behavior of a material.

3.1.18 Maximum Cyclic Strain Range The total strain range experienced after complete stress relaxation during exposure to cyclically induced thermal or mechanical deformations.

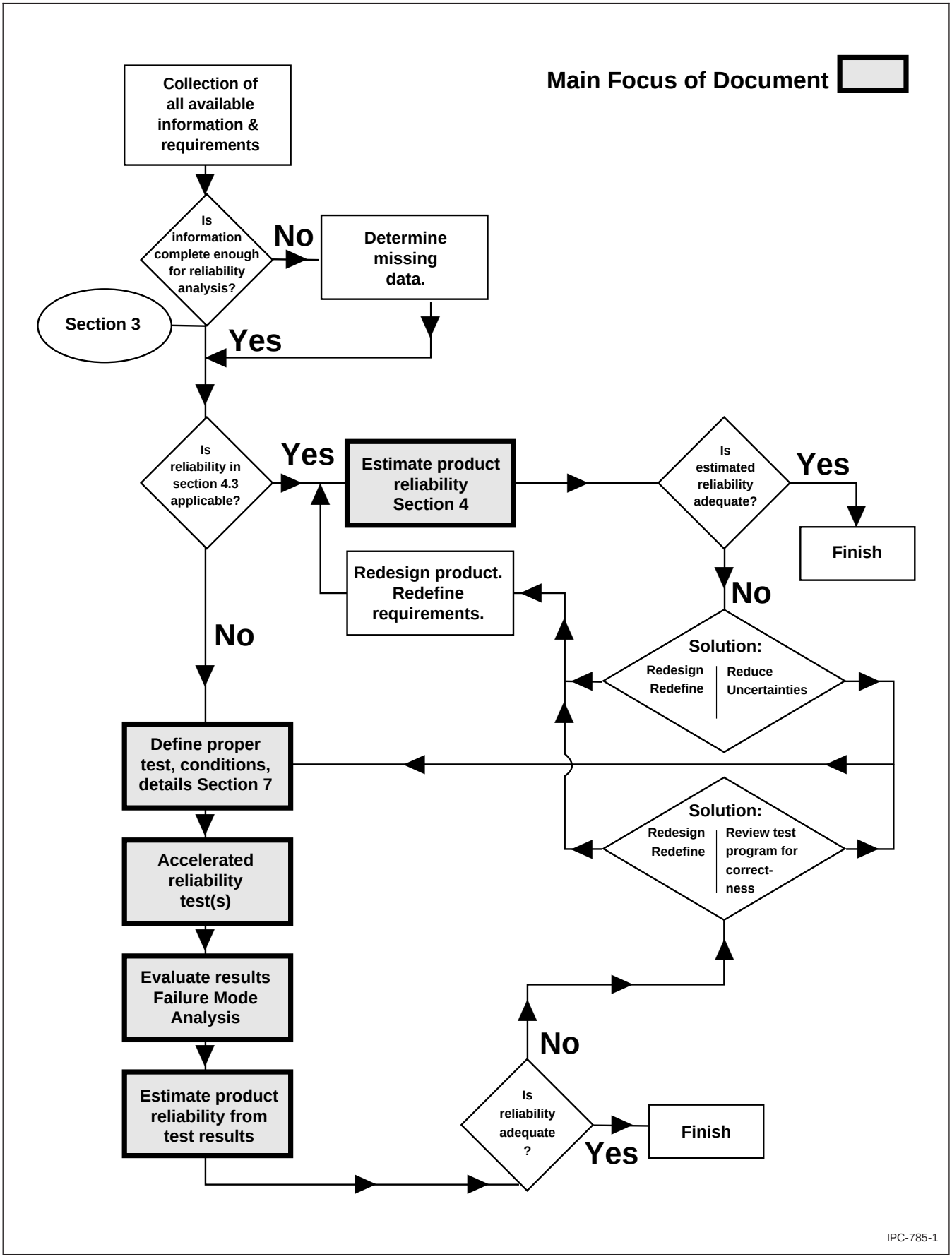

Figure 1 Flowchart for reliability

3.1.19 Mean Fatigue Life The life at which one-half of a given sample of items has failed.

3.1.20 Mechanical Shock A rapid transfer of mechanical energy to a system, which results in a significant change in stress, velocity, acceleration, or displacement within the system.

3.1.21 Process Qualification A special test(s) performed to validate a process capability in terms of producing a product capable of meeting performance specifications.

3.1.22 Process Verification Ongoing evaluation of processes involved in the manufacturing of a product to assure process optimization or to eliminate process deviations.

3.1.23 Random Steady State Period of useful operational life during which failures occur seemingly at random at a low rate weakly related to product complexity.

3.1.24 Reliability The ability of a product to function under given conditions and for a specified period of time without exceeding an acceptable failure level.

3.1.25 Solder Attachment The collection of solder joints (solder connections) associated with a component.

3.1.26 Stress Relaxation The time-dependent decrease in stress due to the visco-plastic deformation as a function of applied displacement.

3.1.27 Thermal Cycling (See 3.4.1) Exposure of assemblies to cyclic temperature changes where the rate of temperature change is slow enough to avoid thermal shock.

3.1.28 Thermal Shock (See 3.4.3) Exposure of assemblies to rapid changes of temperatures causing transient temperature gradients, warpages, and stresses. As a rule of thumb, rates of temperature change in excess of 30°C/minute are required.

3.1.29 Vibration A periodic, typically elastic, motion of a structure in alternately opposite directions from the position of equilibrium.

3.1.30 Visco-Plastic Strain Energy Density A measure of the total energy input into a cyclically loaded structure defined by the boundaries of a hysteresis loop for the applied stress versus strain over a single load cycle.

3.1.31 Wearout The process where the occurrences of failures rise steadily as the product deteriorates due to accumulating (fatigue) damage.

3.1.32 Weibull Distribution A statistical description of the distribution of product failure primarily useful in wearout situations.

3.2 Reliability Concepts and Understanding In the context of this document it is important to have a working definition of reliability:

Reliability is the ability of a product (for this document the products are surface mount solder attachments) to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

Implicit in this definition is the fact that the reliability of SM solder joints is determined by wearout (fatigue), i.e., on a time-to-failure plot (the ''bathtub curve''). Figure 2 shows individual ''bathtub'' reliability plots for SM solder attachments and for a ''typical'' electronic component without the solder attachment. Figure 3 shows the same information in the form of cumulative failure probability plots for the component and the SM solder attachment. The life of the solder attachment is primarily characterized by the right ascending part of the curve, where the failure rate rapidly increases with time due to wearout. This directly implies that manufacturing quality cannot increase the inherent reliability of a design in a given use environment; however, inadequate manufacturing quality can reduce this inherent designed-in reliability by increasing infant mortality failures.

Manufacturing introduces variability into the product. This variability encompasses ranges of all the properties for all the materials in the product, ranges in the dimensions of parts due to tolerance, compositional variations and nonhomogeneities, fluctuations in processing parameters, etc. In good quality manufacturing these variabilities are controlled within ranges that will not significantly degrade product performance. Manufacturing of lesser quality can introduce larger variabilities and/or defects, which can significantly reduce product performance.

Superimposed on these product variabilities (materials, processing, etc.) are differences in the actual use environment, as well as reliability (fatigue) distributions. Even product that is nominally identical when subjected to identical loading conditions will show a statistical failure distribution. Since accelerated reliability testing is time-consuming and costly, it is typically carried out on a rather small number of samples. To capture representative product variabilities and their effect on reliability requires the testing of a sufficiently large number of samples to include these variables. The controlled introduction of artificially created defects that are assumed to have a significant reliability impact would serve the same purpose but is difficult to achieve in practice.

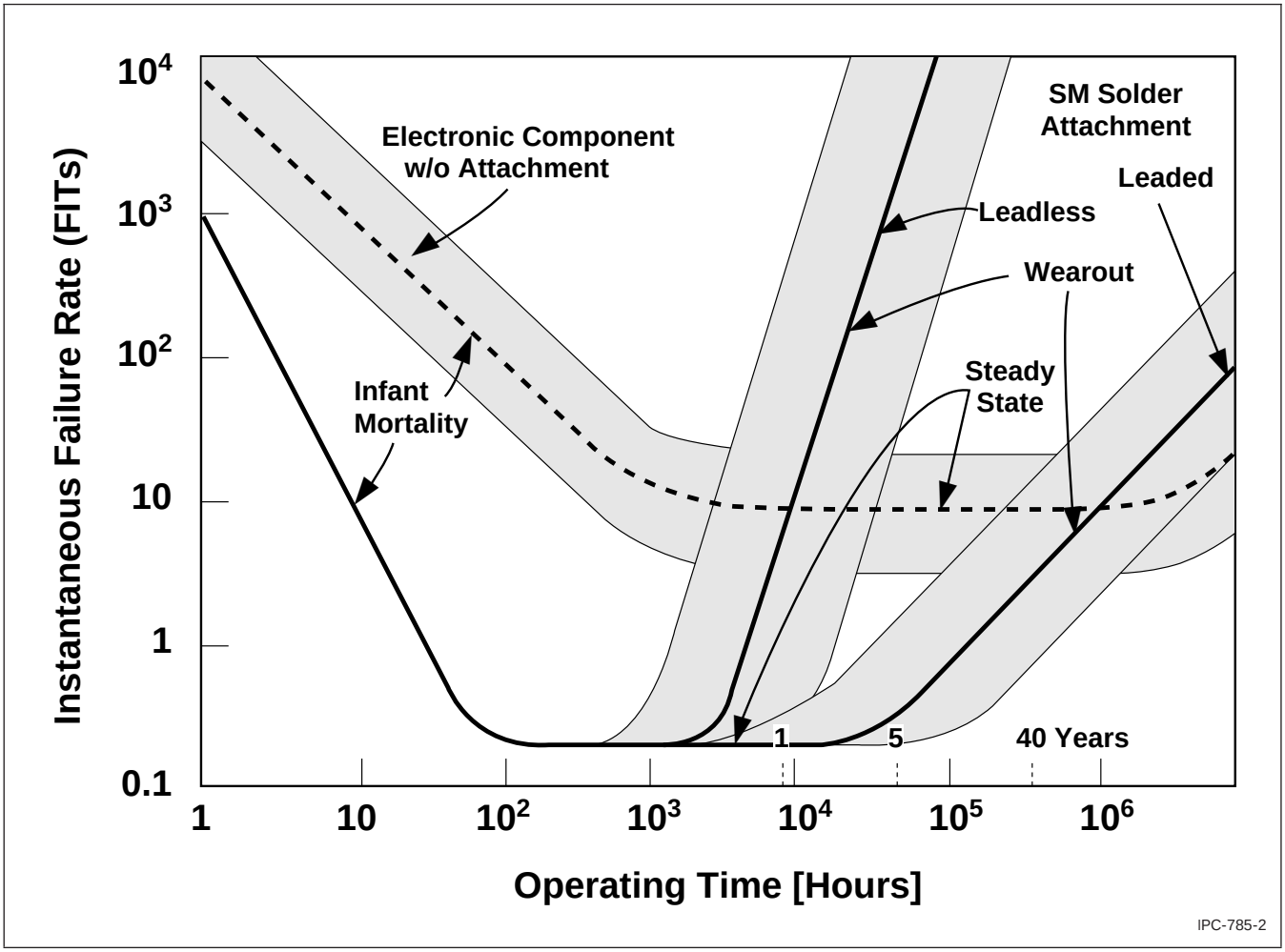

Figure 2 Generic reliability ''bathtub'' curves comparing electronic components and surface mount solder attachment

The reliability ''bathtub'' curves in Figure 2, as well as the resulting cumulative failure probability plots shown in Figure 3, need some explanation. The ''infant mortality,'' ''random steady-state,'' and ''wearout'' regions are defined by which of these three failure modes dominate. The curve intersections in Figure 2 delineate the extent of these regions.

Except for the SM solder attachment wearout regions, the values plotted are rather ''soft.'' Hard data does not exist in adequate quantities for either the component or solder attachment ''infant mortality'' and ''random steady-state'' regions. These plot regions are based on experience and observed trends and some published information. The ''steady-state'' region for components depends to a large extent on the complexity of the component; chip components would fail well below the indicated bathtub band and very complex, high I/O chip carriers would fail at higher rates.

For SM solder attachment, no evidence exists that shows that the ''random steady-state'' failure region even exists; it is entirely possible that ''infant mortality'' and ''wearout'' form the entire failure rate history. It should be noted that for SM solder attachments, the ''infant mortality'' and ''random steady-state'' failure regions are rather unimportant since the failure probabilities are very small even assuming order of magnitude errors. Significant however, is the experience-based observation that the ''random steady-state'' failure rate estimate given in MIL-HDBK-217 is too high by perhaps two or three orders of magnitude. Figures 2 and 3 imply that the reliability of electronic components is determined by the ''random steady-state'' failure region. In contrast, the reliability of the SM solder attachment is established by the ''wearout'' failure region.

The cumulative failure probability of a component and its SM solder attachment is the sum of the component and the attachment failure probabilities. Thus an electronic assembly is more likely to fail due to component failure in the short-term and due to solder joint failure in the long-term.

3.3 Reliability Assurance Surface mount solder joint reliability requires explicit attention in the design phase as well as in manufacturing. An overview of the processes leading to reliability assurance is outlined in the Figure 4 flow chart.

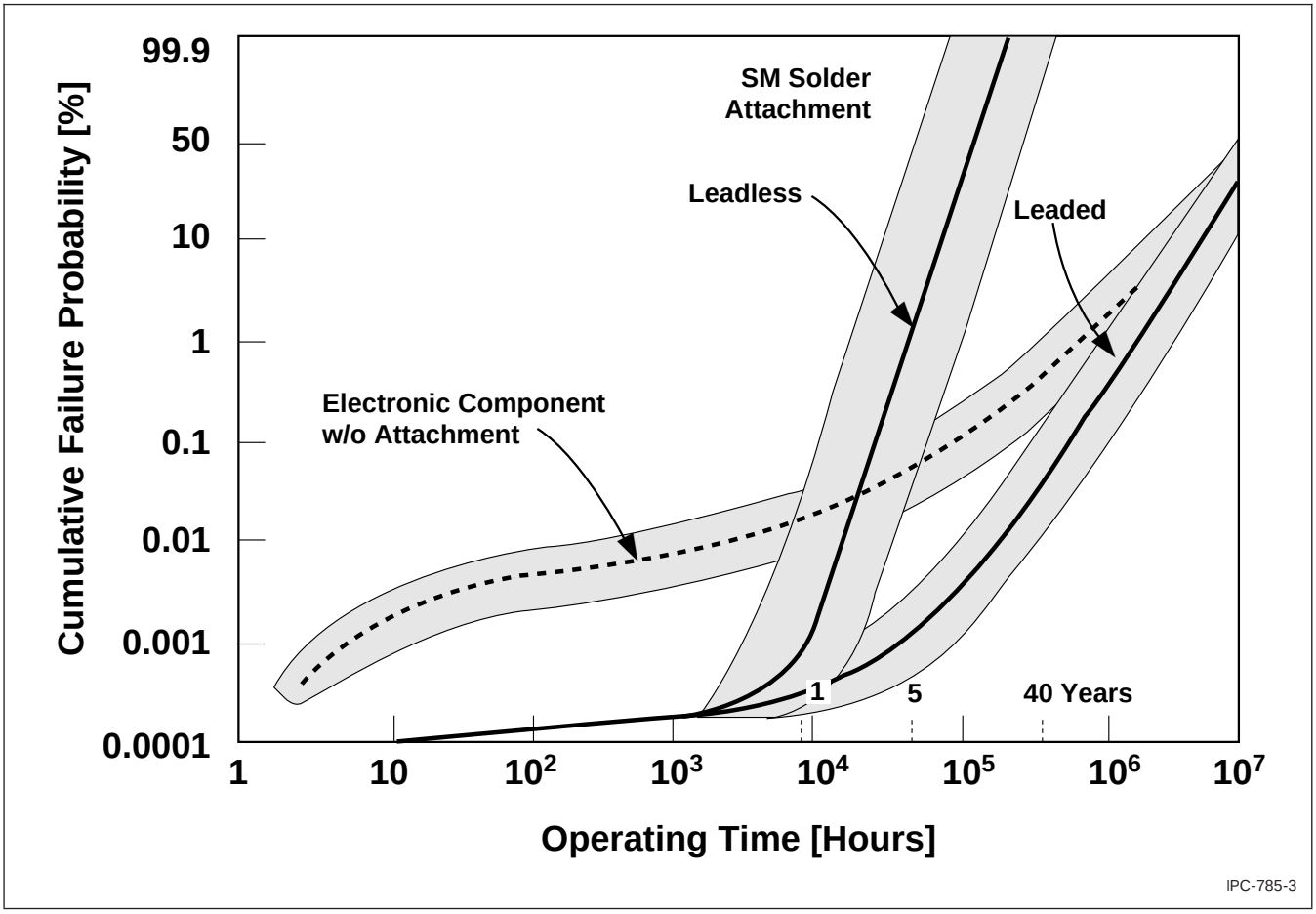

Figure 3 Generic cumulative failure probabilities for electronic component and surface mount solder attachment

3.3.1 Generic Understanding of Solder Attachment Technology Solder is unique due to its temperature-, time-, and stress-dependent behavior. For instance, eutectic tin-lead solder readily creeps and stress relaxes above 20°C, whereas below –20°C solder has long-term load bearing capabilities similar to other metals. The higher the temperature above 20°C and/or the higher the stress level, the faster the solder will creep and stress relax.

A generic understanding of the reliability and failure mechanisms for a given surface mount attachment technology is the first step toward designing and assuring product reliability. For this, a generic database is required. Although failure mechanisms based on cyclic or monotonic overstressing can occur, the most common reliability threat comes from stress-relaxation based fatigue damage. A fatigue failure database must be based on a combination of low acceleration and high acceleration tests.

In this context, low acceleration tests produce mean-times-to- failure of the test vehicles that are about 10 to 20 times shorter than actual life in field use. High acceleration tests are about 100 to 500 times shorter. The higher the test acceleration, the less the test results are representative of performance at field conditions. Thus, low acceleration tests should closely mimic expected field conditions, whereas high acceleration tests are a ''quick and dirty'' compromise necessitated by the reality of the time and resources required for the low acceleration testing.

For accelerated tests, it is imperative that the failures occur as the result of accelerating the proper failure mechanisms. Thermal shock testing does not accelerate the long-term fatigue mechanisms of concern for most surface mount applications, and can result in misleading conclusions. The driving, underlying mechanism causing most of the long-term fatigue damage results from the creep and stress-relaxation behavior of solder. Therefore, accelerated fatigue testing must include well defined dwell times at the cycle extremes to allow for some, albeit incomplete, creep and stress relaxation. The incomplete cyclic creep and stress relaxation in accelerated test cycles is in contrast to most actual field operation environments, where sufficient time is usually available for essentially complete creep and stress relaxation. Thus, the significantly smaller fatigue damage for accelerated test cycles must be accounted for with a fatigue acceleration transform.

The low acceleration tests shown in the leftmost column of Figure 4 call for a highly accurate mimicking of use conditions, with acceleration factors of ten or twenty. For example, if the design life is twelve years, fatigue testing

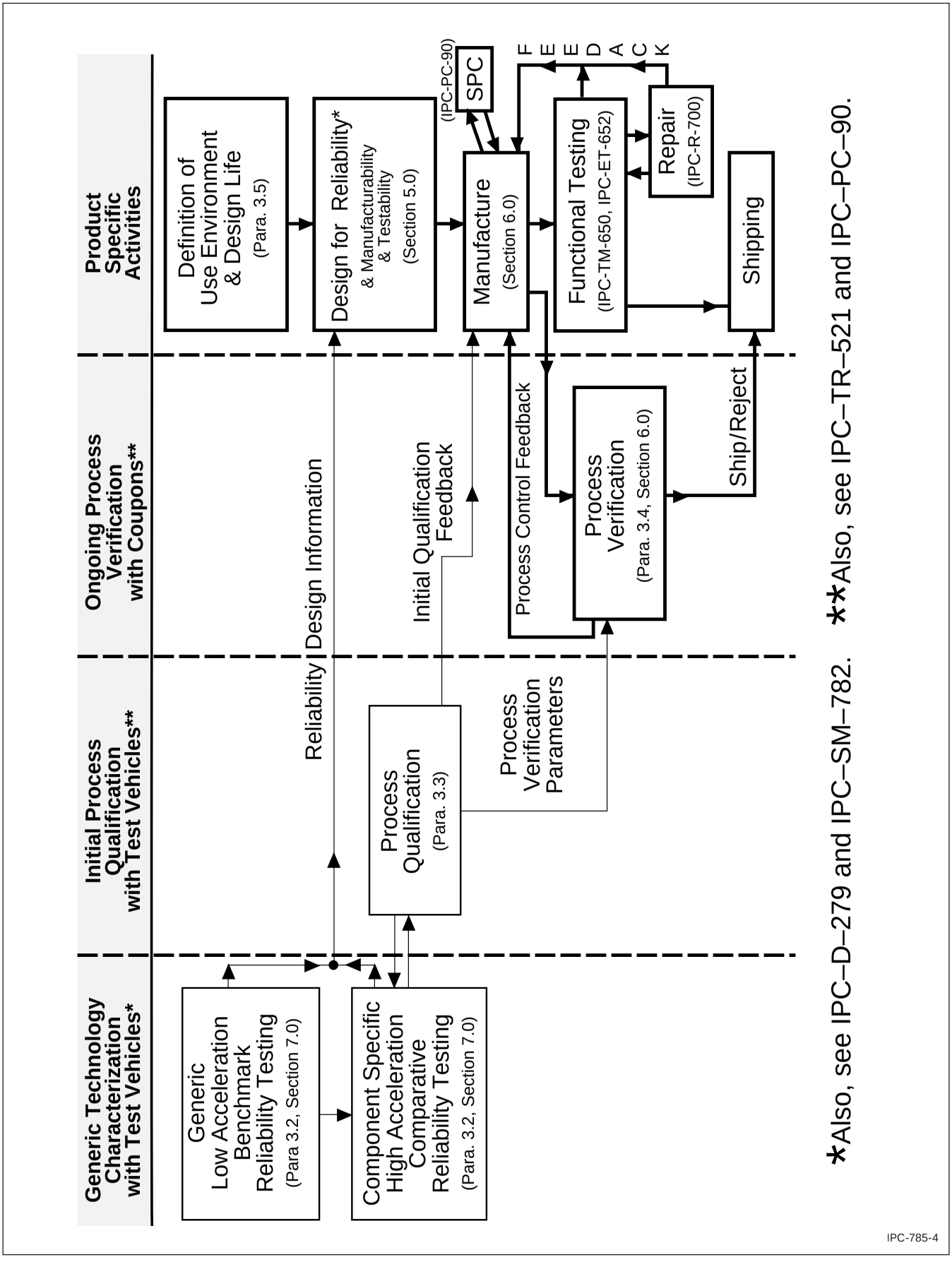

Figure 4 Flow chart for surface mount solder attachment reliability assurance

can be accelerated to the point of completion in about one year. Low acceleration tests are necessary to provide generic, accurate, ''benchmark'' results.

High acceleration tests typically require isothermal mechanical cycling. These tests can provide acceleration factors up to about 500 for mean-time-to-failure (MTTF) for the test, relative to the field MTTF. This is accomplished by testing at elevated temperatures (above 20°C) and applying the cyclic loads mechanically. Mechanical cycling is necessary as the loading technique, because thermal cycling requires substantial transition times between the high and low temperature extremes in order to avoid thermal shock-induced failures not representative of the stress-relaxation fatigue failure mechanism. These high acceleration tests bear relatively little resemblance to use conditions, and the results are useful primarily for relative comparisons. However, by performing both high and low acceleration tests for comparable test vehicles, the low acceleration tests can serve as reliability benchmarks for the more highly accelerated tests. Thus, a limited number of the time consuming low acceleration tests, in combination with the much quicker high acceleration tests, can provide a complete database.

Although the reasons for microelectronic device failures are many, the major cause of failure for solder joints of surface mount components is low cycle thermal fatigue. High cycle fatigue due to vibration can also make some contribution to fatigue damage. Thus, the surface mount technology (SMT) solder joint failures are primarily due to the thermal/mechanical stresses.

The frequency of the thermal cycles for low cycle thermal fatigue usually ranges from a few cycles per hour to one cycle per day or less. The frequency range of equipment vibration is typically from between 10 Hz to 2000 Hz, which results in over one hundred thousand cycles per day. The fatigue damage in vibration is primarily in high-cycle fatigue.

3.3.2 Design The general understanding gained from the accelerated fatigue tests must be translated into reliability design information that can be used for ''Design for Reliability.'' The design information needs to be in the form of simple engineering tools that allow the non-expert designer to assess whether a design meets its reliability requirements. Prior to the ''Design for Reliability'' in the rightmost column of Figure 4, the use environment, the expected design life, and the acceptable cumulative probability of failure at the end of this design life must be established.

3.3.3 Manufacturing Process Qualification The capability of the manufacturing process sequence to produce a reliable product needs to be established in the process qualification of production test vehicles. Some of the test vehicles are run through high acceleration reliability testing and some through the verification process. This qualification activity is relatively complex due to the number and variety of processes used to manufacture and assemble electronic hardware.

Process control parameters and process capability identification are necessary to provide the link between reliability and consistent product. Since each manufacturer has unique combinations of processes, the process control and qualification are different for each manufacturer. In order to ensure that a process is well understood, a manufacturer should characterize those aspects of the process that have the most significant impact on product performance. A properly constructed ''Design of Experiment,'' which evaluates the key variables of the process including their interaction, is paramount to establishing process capability. IPC-PC-90 provides the requirements of the systematic path for establishing process capability. J-STD-001 provides the mechanism for evaluating performance to a strategic plan.

The ''Process Qualification'' step in the second column from the left in Figure 4 also establishes the process verification parameter windows which assure product consistency within the process qualification parameters.

3.3.4 Process Verification Many factors can affect the manufacturing process and may cause changes in the performance of the product in its intended application. A properly characterized process identifies the key variables and establishes the appropriate upper and lower control limits of those attributes which play a significant role on the quality and reliability aspects of the product. If the process changes, a value judgment is required to determine the significance of the change and to determine if the change is an expected variation, a noise factor, or an out-of-control condition.

Ongoing process verification using production boards, production test vehicles, or test coupons that represent the design concepts, together with statistical process control and touch-up/repair feedback, is needed as proof that the process is meeting its projected capability.

Monitoring of product performance through destructive and nondestructive evaluations verifies the relationship between the design, the design reliability expectations and the manufacturing processes.

Although no generic or standard process verification procedure has currently been identified which serves the purpose to an adequate degree, verification of the adequacy of the process is an ongoing activity. The frequency of testing and the type of tests invoked should be commensurate with the maturity of the design and the stability of the process.

3.4 Damage/Failure Mechanisms

3.4.1 Thermal Cycling Damage Mechanisms The primary damage mechanism in thermal cycling is the creep/stress-relaxation-enhanced fatigue of the solder joints. Figure 5 is a stylized representation of the visco-plastic strain energy, proportionally represented by the area of the cyclic hysteresis loops in a stress-strain diagram, expended in one fatigue cycle. This visco-plastic strain energy causes fatigue damage which accumulates from cycle to cycle. When loaded from a zero-stress, zero-strain condition, the solder joint first undergoes elastic deformation followed by plastic yielding if the loading continues beyond the yield strength of the solder. It has to be noted, however, that for solder there is neither a truly elastic deformation nor is the yield strength defined in any physically real sense. The elastic deformation-yielding lines are simplified linearizations of the non-linear stress-strain response that is highly dependent on temperature, loading rate, solder composition and grain structure. Further, the yield strength is a defined artifact for engineering purposes; its definition for solder is equally highly dependent on several variables some of which are controllable (i.e., temperature), and some which are not (i.e., grain structure).

The elastic-plastic yielding portion of the loading response is followed by a temperature- and stress-level-dependent stress relaxation/creep response of the solder joint. Given enough time, which can be minutes at the higher temperatures and days at the lower temperatures, the stresses in the attachment system, of which the solder joints are a part, will essentially completely relax resulting in the maximum possible plastic deformation strains in the solder joints. Dwells beyond this time will not induce further fatigue damage; however, at elevated temperatures the detrimental grain growth in the solder continues.

The primary complication in the damage mechanism arises from the fact that in many applications and, by definition, all accelerated tests, the dwell times are insufficient for complete stress relaxation. The effect of this is illustrated in Figure 5 in the hysteresis loops labeled ‘‘Accelerated Tests’’ for which the loop areas are significantly smaller than the corresponding loop areas for conditions allowing complete stress relaxation. This signifies considerably less fatigue damage per cycle for those accelerated cyclic environments. As a consequence, the number of accelerated test cycles cannot be directly equivalent to the number of operational cycles.

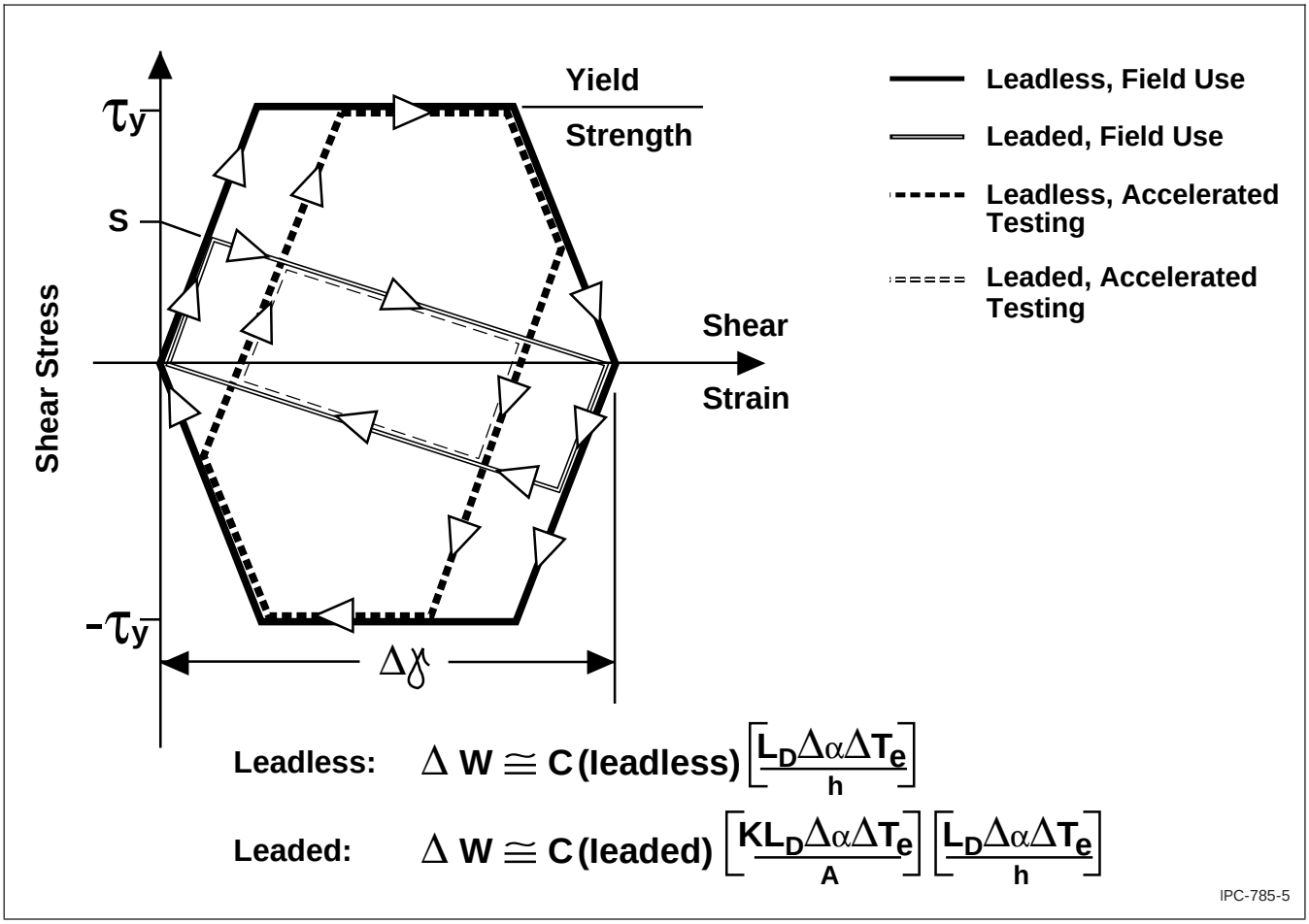

Figure 5 Cumulative fatigue damage

Figure 5 also shows the essential difference between stiff leadless solder attachments and compliant leaded SM attachments. Compliant leaded attachments work because the lead compliancy keeps the maximum stresses in the solder joints significantly below the ''yield strength.'' It should be noted that not all leads are compliant in this context. The diagonal lead stiffness should be below 100 lb/in; above this value, leaded SM attachments become an undefined hybrid between leadless and compliant leaded attachments. While the lead compliance effects complicate the analysis, they substantially reduce the accumulating cyclic fatigue damage even for identical strains at complete stress relaxation. Given the stress-level dependence of the stress relaxation rate and the lower stress levels for solder joints with compliant leads, complete stress relaxation for compliant leaded solder attachment takes significantly longer.

It should be noted that symmetric hysteresis loops as shown in Figure 5 are possible in thermal cycling only if the low temperature dwell times are significantly longer than the high temperature dwells; symmetry, however, is typical for isothermal cycling where the loads are mechanically induced.

The solder joint behavior described in Figure 5 pertains to temperature cyclic environments above about –20°C. The temperature region from about –20 to +20°C is the boundary between primarily a creep/stress relaxation response of the solder to applied loads at the higher temperatures, and a primarily stress-driven solder response at the lower temperatures. The damage mechanism described in Eqs. 3 and 4 is for temperature cyclic environments above about –20°C, which are the more typical use conditions.

For applications in which the stress relaxation and creep in the solder joint is not the dominant mechanism, such as low temperature applications with component operating temperatures of less than 0°C and/or high thermal/mechanical frequency application with frequency of greater than 0.5 Hz or half cycle dwell times of less than 1 second, the direct application of the Coffin-Manson fatigue relationship (see Section 4.3.5) is advised.

Solder joints seeing large temperature swings significantly through the temperature region from –20 to +20°C, in which the change from stress-to-strain driven solder response takes place, do not follow the damage mechanism described in Eqs. 3 and 4 [1]. The damage mechanism is different than that for more typical use conditions and is likely dependent on overstress and recrystallization considerations.

As the fatigue damage accumulates, the grain structure of the solder joints coarsens. After about 25 to 50% of the fatigue life of the solder joints is consumed, microvoids or cavitations form at grain boundary intersections. These microvoids grow into microcracks which, with further accumulating fatigue damage, grow and coalesce into large cracks. For solder joints experiencing non-uniform strain and stress distributions, such as castellated solder joints, a single major crack will lead to failure. For solder joints with uniform strain and stress distribution, such as column-like joints, many multiple cracks will form with one finally failing first.

3.4.2 Vibration Damage Mechanism Vibration induced failures of surface mount solder joints are fundamentally different from thermally induced failures. During thermal cycling, the solder joint is loaded by thermal expansion mismatch. The solder joint strains are dominated by plastic behavior induced by stress relaxation during the cycle hold time. In contrast, vibrations at relatively high frequencies (over 30 Hz), result in elastic behavior in the joint. Stresses are generally smaller and failure occurs over many cycles in the same manner as classic high cycle fatigue in structures.

Vibrations are periodic motion of a body about an equilibrium position. This type of motion is encountered in many applications including automotive, aerospace and military applications. Consequently, electronic enclosures or structures utilized in these environments are also subjected to vibration. Vibrations are transmitted to the printed circuitry through the chassis or primary structure of the enclosure. Relative motion between the board and its edge brackets result in deflections of the board. The stresses induced in surface mounted solder joints are primarily a function of the radius of curvature of the board occurring as a result of the deflection and the position of the part on the board.

Generally, the magnitude of the stresses or cyclic stress amplitude induced by vibration are relatively small. This in combination with the high frequency motion or high strain rates induce elastic behavior in the joint. The rapidly changing loads do not allow for stress relaxation. In addition, the elastic modulus of solders tends to increase with increasing frequency of loading or increasing strain rates. This favors elastic behavior.

However, very high stresses can be induced in solder joints under certain conditions. If the frequency of the external driving force approaches the natural frequency of the board, large board deflections will occur. Hence, large stresses will be induced in joints at certain board locations. The natural frequency is simply the frequency at which the system will vibrate under free conditions. When the external driving frequency approaches this frequency a resonant condition occurs. Generally, electronic equipment is tested over a frequency range representative of the application to ensure there are no undesirable resonant frequencies inherent in the design.

Although the bulk stresses are elastic, failure occurs due to highly localized plastic behavior. Small stress concentrations or defects on the surface of the solder or at interfaces induce localized plastic strains. At some points, the crystal

structure of individual ''grains'' of the solder is oriented so that maximum applied shear stresses exceed the critical stress necessary to induce slip in easy slip planes. Under cyclic loading conditions intrusions and extrusions occur. Eventually well formed intrusions or persistent slip bands form microcracks.

The microcracks grow and coalesce into one larger crack. Crack propagation is generally transgranular as opposed to ''intergranular'' cracking observed in creep dominated thermal fatigue. Stable crack growth occurs by striation formation until the joint can no longer withstand the applied load. Failure of the joint subsequently occurs when the joint is no longer structurally and electrically viable. This process generally occurs in a large number of cycles (10^4 or greater) and is termed high-cycle fatigue as opposed to low-cycle fatigue (10^3 cycles or less) resulting from cyclic strain amplitudes large enough to cause substantial plastic yielding strains; the range in between is a mixed mode.

3.4.3 Thermal Shock Damage Mechanism In thermal shock, the extremely rapid temperature changes (about 30°C/minute and above) result in warping of the surface mount assembly. The warpage is caused by large transient thermal gradients induced by the rapid temperature change when the boards are plunged into a new thermal environment. The warpages result in tensile and shear stresses where the tensile loading dominates over the steady state expansion mismatch. Thus, even assemblies with matched coefficients of thermal expansion will exhibit solder joint failures when subjected to thermal shock. The thermal shock loading mechanism is summarized in Figure 6.

Thermal shock conditions can arise from several sources. Examples of these are as follows:

1. Rapid changes in external environment, e.g., sun-to-shade in space.
2. Sudden and large changes in power status.
3. Various manufacturing/repair processes, e.g., reflow, vapor decrease, rework, repair, etc.

The distinction between thermal shock and thermal cycling is not always addressed in designing reliability experiments. There is a fundamental difference between thermal shock and thermal cycling. The primary differences arise from the mechanism of loading. Thermal shock tends to result in multiaxial states of stress dominated by tensile overstresses and tensile fatigue. On the other hand, as previously discussed, thermal cycling results in shear loads and failure occurs from an interaction of shear fatigue and stress relaxation. Thermal shock is performed in dual chamber test equipment whereas thermal cycling is performed in single chamber cycling equipment. Dual chamber arrangements may produce temperature transition rates in excess of 50°C/minute.

Most single chambers generally do not produce transition rates even close to 30°C/minute which is roughly the minimum rate necessary to induce thermal shock. The results of these two types of testing are generally not correlatable, even through some design measures will prolong life under both conditions. Consequently, thermal shock testing for purposes of evaluating surface mount solder joint reliability is only appropriate if thermal shock is indeed a field condition encountered by the product.

In some specifications, the definitions of thermal cycling and thermal shock are not fully differentiated; the rates of change are more closely associated with what we are calling thermal shock.

3.4.4 Creep Rupture of Solder Joints Creep rupture refers to a condition in which a solder joint has a fixed load applied to it. The application of the load creates an initial deflection in the solder joint. As time increases, the solder in the joint will creep. This results in an increase in deflection while the load on the sample remains constant. Creep rupture occurs when the solder cannot support the applied load any longer and fractures.

When the solder joint fractures in creep rupture, the time to failure can be plotted for a range of applied initial loads or deflections. The latter would be the condition the solder joint sees when components are soldered to a board and the board is put into a bent shape creating a constant strain on each solder joint. If the board remains in this bent shape, the solder joints could fracture in creep rupture. Analysis of the fracture surface would most likely show the usual ductile rupture/fracture surface characteristic of solder.

While creep rupture is similar to stress relaxation in terms of the underlying mechanism, stress relaxation is the condition that occurs when the solder joint is subjected to a fixed deflection. As time increases, the stresses in the solder joint undergo relaxation, but the deflection remains constant. The decrease in load at fixed deflection results in the elastic strains in the solder joint being converted into plastic permanent strains.

3.5 Application Considerations The reliability of a surface mount assembly is dependent on the service environment, the expected cyclic service life, and the acceptable cumulative failure probability at the end of the cyclic service life. The reliability of a surface mount attachment, of course, also depends on the assembly design parameters (including the number and mix of components), which will be dealt with in the section on Design for Reliability.

3.5.1 Service Environment In Table 1 worst-case, but realistic, use environments for SM electronic assemblies are shown in nine major use categories. These use environment categories are listed in order of increasing severity without consideration of the number of expected service years. It should be noted that the cyclic temperature range, ΔT, is not the difference between the possible minimum,

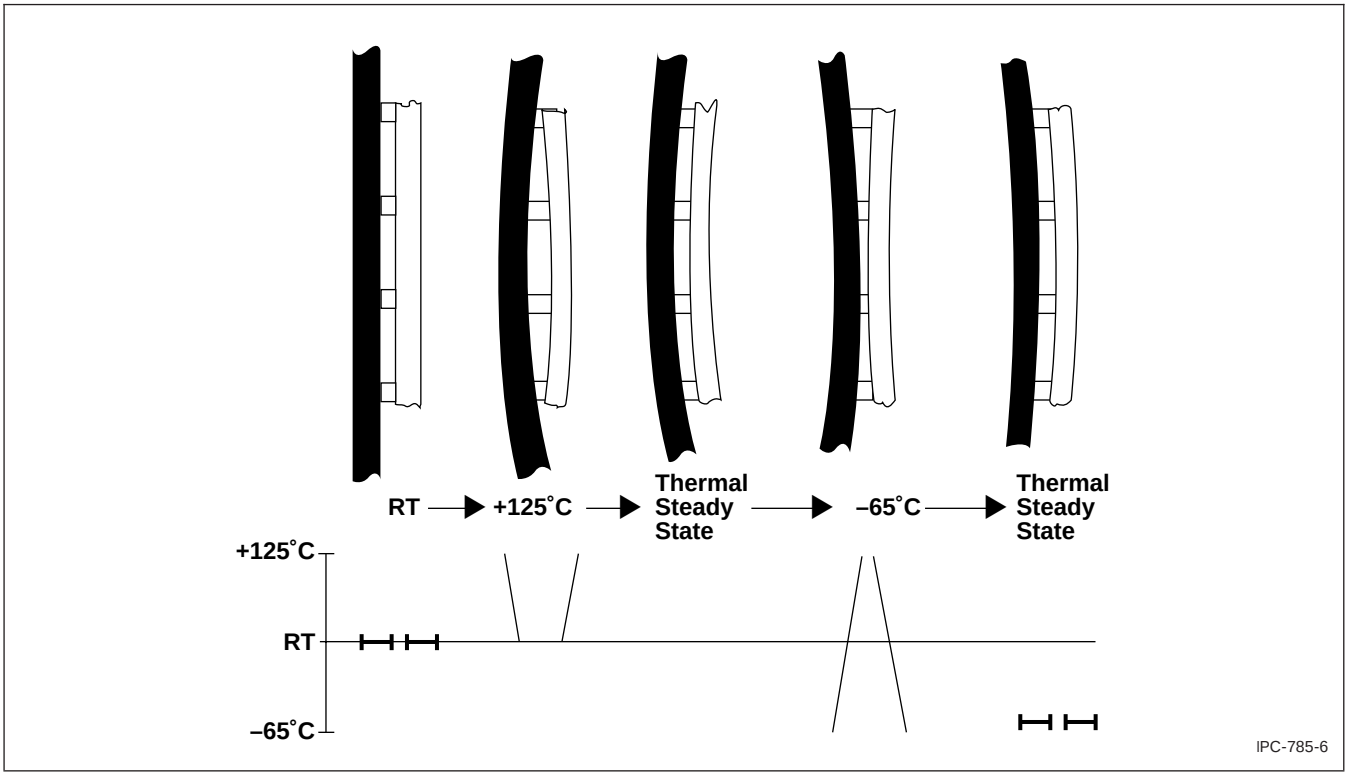

Figure 6 SMT assembly thermo-mechanical deflections resulting from thermal gradients in thermal shock

T_{MIN} and maximum, T_{MAX}, operational temperature extremes; ΔT is typically significantly less. It has to be recognized that these temperature extremes are possible only during different times of the year and then only at significantly different geographic locations. The ΔT values represent the worst-case temperature swings that can be expected during a given operating cycle.

Also given are the expected dwell times, t_D, at operating temperatures; they are significant because they determine the degree of completeness of the stress relaxation in the solder joints and thus determine the amount of cyclic fatigue damage relative to the maximum fatigue damage at complete stress relaxation. Table 1 also gives estimates of the number of operating cycles occurring during a service year. There is an inverse relationship between the cyclic dwell times and the number of service cycles per year. For some of the use categories, the use environments are described in terms of the sum of multiple use environments resulting from either significant seasonal dependence or broadly foreseeable use conditions; the military avionics category is subdivided into three subcategories reflecting differing use conditions due to type of aircraft, location on aircraft, mission profile, geographic effects, etc. The space category contains two different environments for satellites in low-earth orbit (LEO) or geo-synchronous (stationary relative to Earth) orbit (GEO).

Variation of the external (outside of the equipment enclosure) ambient temperature is one of the multitude of factors that will determine the actual temperature cycle a specific surface mounted device will see in a real application. Only very simple equipment which is powered continuously at constant power will see the same variation of temperature as the external ambient. In some cases, assuming the ambient temperature is the cause of temperature variation inside the cabinet, the system designer will introduce built-in means of reducing the temperature swing inside the cabinet by activating fans when the inlet air temperature exceeds certain limits or activating inlet air heaters when the inlet air temperature drops below certain limits. In some applications, the variation of the temperature inside the electronics enclosure is generated by variations of the power dissipated by the electronics. An example of this type of behavior is the telecommunication equipment in which the total power dissipation is a function of the traffic or the number of simultaneous calls passing through the system. Relatively large temperature variations could be generated inside the system between the high traffic periods, mainly during the working hours, and the low traffic periods, usually evening or night hours, even though the system is maintained inside an air conditioned room with practically no ambient temperature variations. A device mounted downstream of a high power dissipator sees a temperature variation related to the variation of the temperature of the thermal wake produced by the power dissipator even though the temperature inside the enclosure is maintained constant.

These examples show that in most cases, the variation in temperature of the equipment external environment is not a

Table 1 Worst-Case Use Environments for Surface Mounted Electronics and Recommended Accelerated Testing for Surface Mount Solder Attachments by Most Common Use Categories
(The actual thermal environments in use need to be established by thermal analysis or measurement.)

	WORST-CASE USE ENVIRONMENT							ACCELERATED TESTING			
USE CATEGORY	Tmin °C	Tmax °C	$\Delta T^{(1)}$ °C	t_D hrs	Cycles/ year	Typical Years of Service	Approx. Accept. Failure Risk, %	Tmin °C	Tmax °C	$\Delta T^{(2)}$ °C	t_D min
1) CONSUMER	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) COMPUTERS	+15	+60	20	2	1460	5	0.1	+25	+100	75	15
3) TELECOM	- 40	+85	35	12	365	7-20	0.01	0	+100	100	15
4) COMMERCIAL AIRCRAFT	-55	+95	20	12	365	20	0.001	0	+100	100	15
5) INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1	0	+100	100 & COLD[3]	15
6) MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	10	0.1	0	+100	100 & COLD[3]	15
7) SPACE leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0.001	0	+100	100 & COLD[3]	15
8) MILITARY AVIONICS a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01	0	+100	100 & COLD[3]	15
9) AUTOMOTIVE UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0.1	0	+100	100 & COLD[3] & LARGE $\Delta T^{(4)}$	15

& = in addition

1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, ΔT, is not the difference between the possible minimum, T_{MIN}, and maximum, T_{MAX}, operational temperature extremes; ΔT is typically significantly less.

2) All accelerated test cycles shall have temperature ramps <20°C/minute and dwell times at temperature extremes shall be 15 minutes measured on the test boards. This will give ~ 24 test cycles/day.

3) The failure/damage mechanism for solder changes at lower temperatures; for assemblies seeing significant cold environment operations, additional "COLD" cycling, from perhaps –40 to 0°C, with dwell times long enough for temperature equilibration and for a number of cycles equal to the "COLD" °C operational cycles in actual use is recommended.

4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain –20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate "LARGE ΔT" testing with cycles similar in nature and number to actual use is recommended.

good indicator of the real temperature cycle at the device level. Different devices inside the same system are likely subjected to different temperature cycles. It is therefore necessary that thermal analyses or temperature measurements be performed to establish the actual temperature swings of the different components. This is best done when the respective component is not powered and the rest of the system is normally activated. When variations of power are involved, the temperature swing related to the power cycling must be added to the variations of the local temperature environment. In most cases, the difference in temperature between the device case and the board underneath the device is not larger than 5°C. In these cases, the simple superposition of the two cycles (local environment and power cycling) is quite adequate for estimating the real temperature cycle the solder joint of a specific device will see in different environments and under different operational conditions.

3.5.2 Service Life The design service life, N, varies significantly for the use categories in Table 1. The design service lives can range from less than one year, barely exceeding the warranty period for consumer products, to 20 years or more for telecommunications equipment and commercial aircraft. For some military applications the service life is measured in thousands of hours.

3.5.3 Acceptable Cumulative Failure Probability The acceptable cumulative failure probability, F(N), at the end of the design service life, N, can vary significantly depending on the specific purpose of the product, the complexity (number and mix of components) of the product and perhaps the design service life. F(N) values could range from 1 ppm for products whose failure has critical consequences, e.g., cardiac pacemakers, to perhaps 10,000 ppm (1%) for consumer products or products which provide redundancy or ''limp-home capability'' in case of electrical systems failure.

4.0 SURFACE MOUNT SOLDER ATTACHMENT FATIGUE BEHAVIOR AND RELIABILITY PREDICTION

The fatigue behavior of surface mount solder joints has been investigated experimentally in numerous studies. The results of the studies that were carried out in a manner to assure the same damage mechanism as the mechanism operative in typical electronic products have yielded a mathematical solder fatigue model. This model has been expanded and augmented to its current form, presented in this section, as additional test results became available.

The model is for uncoated solder attachments. The complexity and vast differences in conformal coatings make it impossible to develop a generic model that considers all the variables. Products with conformal coatings should be evaluated using test vehicles having the same coating and test vehicles without the coating in order to assess the impact of the coating on reliability.

4.1 General Fatigue Life Models A generalized fatigue damage law for metals has been developed on the basis of cumulative stored visco-plastic strain energy density. The cyclic shear fatigue life, N_f, is related to ΔW, the visco-plastic strain energy density per cycle in a stabilized fatigue cycle, by the equation developed by Morrow [6]:

$$\overline{N_f} = C\,[\,\Delta W\,]^{1/c}\,, \qquad (1)$$

where C is a material constant and the exponent c is in the range of –0.5 to –0.7 for most metals. The well-known Coffin-Manson plastic strain-fatigue life relationship [5] can be directly derived from, and is a special stress-limited case of, this generalized fatigue damage function and is:

$$\overline{N_f} = C\,[\Delta\gamma_p\,]^{1/c}\,, \qquad (2)$$

where $\Delta\gamma_p$ is the cyclically applied plastic strain range.

4.2 Solder Joint Fatigue The long-term reliability of a surface mount (SM) solder attachment is governed by the difference between the required design life and the cyclic fatigue life of the solder joint as determined by the combination of component design, assembly design, and use environment. The cyclic fatigue life of a solder joint is determined by the amount of cyclically accumulating fatigue damage. Solder joint fracture occurs when the total accumulated damage exceeds the capability of solder to sustain such damage.

The solder joint response to cyclic displacements is characterized by a hysteresis loop in the shear stress/strain plane (see Figure 4). The area of this hysteresis loop is the visco-plastic strain energy density per cycle, ΔW.

For leadless SM solder attachments, the hysteresis loop is limited by a constant stress envelope (independent of the thermal expansion mismatch) determined by the solder yield strength during the initial elastic loading and plastic yielding, and the stress reduction lines during creep and stress relaxation. For leadless SM solder attachments, analysis is relatively simple since, unlike the response of leaded attachments, it is not complicated by interacting effects between the solder and the compliant lead structures.

For typical leaded SM solder attachments, the maximum solder joint stresses are significantly below the solder yield strength, and depend on the thermal expansion mismatch. Thus the stress reduction lines, except for some initial elastic loading, determine the hysteresis loop in the stress direction. In both leadless and leaded SM solder attachments, the maximum strains are determined by the displacements resulting from thermal expansion mismatch.

For metals used in temperature ranges where time and temperature dependent creep and stress relaxation become significant relative to the initial plastic strains due to yielding (typically in excess of 50% of the absolute melting temperature), the determination of either ΔW or $\Delta\gamma_p$ is not straight-forward. The total plastic strains will increase with time as strain energy elastically stored in the component lead/solder joint/substrate structure will be converted to cumulative unrecoverable visco-plastic strain energy in the structure member (solder) that creep/stress-relaxes. With sufficient time, which for solder at operating temperatures can be quite short, virtually all the elastically stored strain energy accumulates as visco-plastic strain energy in the solder joints. This maximizes the cyclically traversed hysteresis loop in the shear stress/strain plane and thus maximizes the cyclic fatigue damage to the solder joint.

For accelerated fatigue testing, the dwell times during the cycle half-periods are insufficient for full stress relaxation/creep to take place; it is the shortened dwell times which

provide the test acceleration but which also require that the reduced cyclic fatigue damage during accelerated testing be accounted for.

4.3 Fatigue Behavior of Solder Joints It has been shown [2,3,4] that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation [5] developed for more typical engineering metals. For practical reasons and as the direct consequence of the time-dependent stress-relaxation/creep behavior of the solder at typical use environments (see Table 1), the specialized case of the Coffin-Manson equation requires reversion to the more general relationship of Morrow [6]; it also requires that the cyclic strain energy be based on the total possible thermal expansion mismatch and that the exponent is a function of temperature and time to provide a measure of the completeness of the stress-relaxation process.

The fatigue life, $N_f(x\%)$ of surface mount solder attachments at a given acceptable failure probability, x, and thus the reliability of surface mount (SM) solder attachments can be predicted for both isothermal-mechanical and thermal cycling [7]. These predictions are for typical realistic use conditions and representative accelerated tests, and are subject to the caveats listed later in this section.

For stiff leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength, the predictive equation for thermal cyclic loading is

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{h}{L_D\Delta\alpha\Delta T_e}\right]^{-\frac{1}{c}}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \quad (3)$$

It should be noted that in equation 3, as well as equation 4, the parameters to the left of the second bracket represent the physical causes of failure and give the mean cyclic life; the terms in the second bracket reflect the statistical distribution of failures which is represented by a Weibull distribution.

For compliant leaded solder attachments, where the solder joint stresses are below the yield strength and thus are not bounded by it, the predictive equation is

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{(200\ \text{psi})\,Ah}{K_D\,(L_D\,\Delta\alpha\Delta T_e)^2}\right]^{-\frac{1}{c}}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \quad (4)$$

where for metric units the scaling coefficient is 1.38 MPa instead of 200 psi, where for near-eutectic tin/lead (63/37 and 60/40) solders (for other solders the coefficients are expected to have different values)

$$c = -0.442 - 6X10^{-4}T_{SJ} + 1.74X10^{-2}\ln\left(1+\frac{360}{t_D}\right) \quad (5)$$

and where

A = effective minimum load bearing solder joint area (≅2/3 solder-wetted lead area projected to the solder pad),

c = fatigue ductility exponent defined in Eq. 5,

F = empirical ''non-ideal'' factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, brittle intermetallic compounds, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. 3 and 4; 1.5>F>1.0 for column-like leadless solder attachments, 1.2>F>0.7 for leadless solder attachments with fillets (castellated chip carriers and chip components), F≅1 for solder attachments utilizing compliant leads;

h = solder joint height, for leaded attachments h≅1/2 of solder paste stencil depth as a representative dimension for the average solder thickness,

K_D = ''diagonal'' flexural stiffness of unconstrained, not soldered, component lead, determined by strain energy methods [8,9,10,11] or finite element analysis,

$2L_D$ = maximum distance between component solder joints measured from component solder joint pad centers,

N = (design life times cyclic frequency), number of operating cycles during product life,

$N_f(x\%)$ = number of operating cycles to x% failure probability,

T_C ,T_S = steady-state operating temperature for component, substrate, (T_C>T_S for power dissipation in component) during high temperature dwell,

$T_{C,0}$,$T_{S,0}$ = steady-state operating temperature for component substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,0} = T_{S,0}$,

T_{SJ} = (1/4)($T_C + T_S + T_{C,0} + T_{S,0}$), mean cyclic solder joint temperature,

t_D = half-cycle dwell time in minutes, average time available for stress relaxation at T_C & T_S and $T_{C,0}$ & $T_{S,0}$,

x = acceptable cumulative failure probability for the component under consideration after N cycles, %,

α_C,α_S = coefficient of thermal expansion (CTE) for component, substrate,

β = Weibull shape parameter, slope of Weibull probability plot, if unknown, use 4 for leadless attachments and 2 for compliant leaded attachments,

ΔD = potential cyclic fatigue damage at complete stress relaxation,

ΔT_C = $T_C - T_{C,0}$, cyclic temperature swing for component,

ΔT_e = $(\alpha_S \Delta T_S - \alpha_C \Delta T_C)/\Delta\alpha$, equivalent cycling temperature swing, accounting for component power dissipation effects as well as component external temperature variations ($\Delta\alpha \neq 0$),

ΔT_S = $T_S - T_{S,0}$, cycling temperature swing for substrate (at component),

$\Delta\alpha$ = $\alpha_C - \alpha_S$, absolute difference in coefficients of thermal expansion of component and substrate, CTE-mismatch,

ε_f' = fatigue ductility coefficient, $2\varepsilon_f' \cong 0.65$ for near-eutectic tin/lead (63/37 and 60/40) solder (for other solders the value of ε_f' is expected to be different).

Equations 3 and 4 contain all the first-order parameters influencing the shear fatigue life of solder joints and come from a fundamental understanding of the response of surface mount solder joints to cyclically accumulating fatigue damage resulting from shear displacements due to thermal expansion mismatches between component and substrate. These shear displacements, the global thermal expansion mismatch, cause time-independent yielding strains and time-, temperature-, and stress-dependent creep/stress-relaxation strains [7,12]. These strains, on a cyclic basis, form a visco-plastic strain energy hysteresis loop which characterizes the solder joint response to thermal cycling and whose area is indicative of the cyclically accumulating fatigue damage. Hysteresis loops in the shear stress-strain plane have been experimentally obtained [4,13,14,15]. In Eqs. 3 and 4 A, h, K_D, and L_D are physical design parameters; $\Delta\alpha$ depends on the material properties of component and substrate; ΔT_e reflects the component-external environmental and thermal conditions as well as the component-internal power dissipation; c in Eq. 5 accounts for the degree of completeness of the cyclically recurring stress relaxation process in the solder joints (the coefficients in c are dependent on the solder composition—the values given are for 60 Sn/40 Pb and eutectic Sn/Pb solder), and β is the slope of the Weibull statistical failure distribution.

The ''non-ideal'' factor, F, needs to be determined empirically from the difference in the prediction of fatigue life from Eqs. 3 or 4 for idealized solder attachments (F=1), and the fatigue life obtained empirically from accelerated testing. It should be noted that it is not altogether clear whether the F-values obtained from accelerated tests are necessarily the same for cyclic use environments, which typically allow more complete cyclic stress relaxation.

4.3.1 Failure Definition Solder joints subject to cyclic thermal expansion mismatches fail as the result of the accumulating shear fatigue damage, a wearout phenomenon. Depending on the loading conditions, this fatigue damage can be enhanced by tensile stresses (vibration and/or mechanical shock), creep and stress relaxation, corrosion and/or oxidation, and other contributing mechanisms.

Solder joint failure is defined as the complete fracture through the cross-section of the solder joint with the solder joint parts having no adhesion to each other.

A solder joint that fails by fully fracturing typically does not exhibit an electrical open or even a very noticeable increase in electrical resistance. A failed solder joint is normally surrounded by solder joints that have not yet failed and therefore the solder joint fracture surfaces make compressively loaded contact. Electrically, the solder joint failure manifests itself only during thermal or mechanical transients or disturbances in the form of short duration (~ 1 µsec) high resistance spikes (≥300Ω). During thermal changes the solder joints are subject to shear, not tensile, loading; therefore, fracture surfaces of fractured solder joints slide relative to each other producing the characteristic short duration intermittents. Therefore, in this context, the practical definition of failure is the interruption of electrical continuity (≥300Ω) for periods greater than 1 µsec [16].

However, the interval between solder joint failure and the detection of this failure can be in the hundreds of cycles. This can become important for accelerated reliability testing with high test accelerations and expected early (<~ 1000 cycles) failures, where this detection interval can become a large portion of the total life.

4.3.2 Multiple Cyclic Load Histories The different histories of multiple cyclic loading, e.g., ''cold'' temperature fatigue cycles (storage and transport) combined with higher temperature creep/fatigue cycles (normal, as well as air conditioning failure, operating conditions, see Table 1) combined with vibration, all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative (this assumption underlies Eqs. 3 and 4, as well), and that the simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule [17] can be applied,

$$\sum_{1}^{i} \frac{N_i}{N_{f,i}} \leq 1 \qquad (6)$$

where

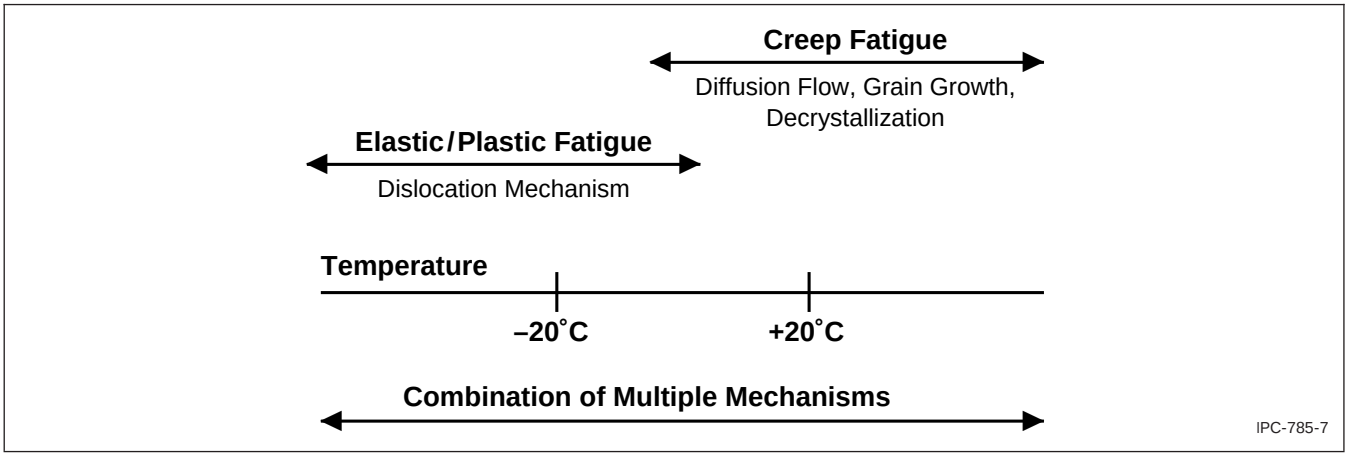

Figure 7 Thermal cycle/fatigue mechanisms for solder

N_i = actually applied number of cycles at a specific cyclic load level i,

N_{fi} = fatigue life at the acceptable failure probability from the same specific cyclic load level i alone.

Equation 6 can be used with the allowable sum of the fatigue damage fractions significantly less than unity to provide greater margins of safety. However, if the number of cycles and the fatigue lives in Eq. 6 already are for low failure probabilities, the margins of safety are more directly provided for and Eq. 4 should be used as shown.

4.3.3 CAVEAT 1—Solder Joint Quality The solder joint fatigue behavior and the resulting reliability prediction relationships, Equations 3 and 4, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the intermetallic compound (IMC) layers. These equations could be optimistic upper bounds if the interfaces become the ''weakest link'' in the surface mount attachments. This would be the case for solder joints for which the solder is not properly wetted or for which layered structures are interposed between the base material and the solder joints. Such layered structures could be: metallization layers that have weak bonds to the underlying material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing proper metallurgical bond of the solder to the underlying metal; brittle intermetallic compound layers too thick due to elevated temperature processing steps, perhaps because of too long durations, too high temperatures, and/or too many such steps.

4.3.4 CAVEAT 2—Large Temperature Excursions Solder joints seeing large temperature swings that include the temperature region from –20 to +20°C where the change from stress-to-strain driven solder response takes place, do not follow the damage mechanism described in Eqs. 3 and 4 [1] (see Figure 7). The damage mechanisms are different and are likely dependent on overstress and strong variations of the properties of the solder.

4.3.5 CAVEAT 3—High Frequency/Low Temperatures For high-frequency applications, $f > 0.5$ Hz or $t_D < 1$ sec, e.g., vibration and/or low temperature applications, $T_C <$ 0°C, solder behaves like an elastic material and the stress relaxation and creep in the solder joint is not the dominant mechanism (see Figure 7). The direct application of the Coffin-Manson fatigue relationship [5] describing non-creep fatigue is advised in this case. This relationship, modified to include the statistical failure distribution, is

$$N_f(x\%) = \frac{1}{2}\left[\frac{\Delta\gamma_p}{2\varepsilon_f'}\right]^{\frac{1}{c}}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \qquad (7)$$

where $\Delta\gamma_p$ = cyclic plastic strain range,

$c \cong -0.6$

$\beta \cong 3.0$

It has to be noted that the determination of $\Delta\gamma_p$ depends on the expansion mismatch displacements and the separation of the plastic from the elastic strains.

4.3.6 CAVEAT 4—Local CTE Mismatch For applications for which the global thermal expansion mismatch is very small, e.g., ceramic-on-ceramic or silicon-on-silicon (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equations 3 and 4 do not address the local thermal expansion mismatch [16, 18]. This reliability problem needs to be assessed using an interfacial stress analysis [19] and appropriate accelerated testing.

4.3.7 CAVEAT 5—Lead-Solder CTE Mismatch For leaded surface mount components with lead materials that have CTEs significantly lower than copper alloy materials, e.g., Kovar, Alloy 42, the results from Eq. 4 will be optimistic since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included. Under some circumstances this mechanism can become dominant.

4.3.8 CAVEAT 6—Very Stiff Leads/Large Expansion Mismatches Equations 3 and 4 differentiate between surface mount solder attachments that are leadless and those with compliant leads. Leadless solder attachments presume substantial plastic strains due to yielding prior to creep and stress relaxation, whereas compliant leads prevent stresses in the solder joints to reach levels where substantial yielding can take place.

However, there is an intermediate region that is not covered by these assumptions. For very stiff leads, perhaps at lead stiffnesses K_D > ~ 500 lb/in and/or for very large thermal expansion mismatches resulting in strain ranges $\Delta\gamma$ > ~ 10%, the damage estimates in Eq. 4 can be substantially in error. In general, caution might be indicated in all instances where the predicted life $N_f(x\%)$ is less than 1000 cycles (see also Section 4.3.1).

For very stiff leads, the stresses calculated in Eq. 4 can exceed the yield strength of the solder. Since yielding will not permit stresses significantly higher than the yield strength, these calculated stress ranges will overestimate the cyclic fatigue damage and thus result in substantially underpredicted fatigue lives. To prevent this analytical error, the stress range in Eq. 4 needs to be bounded by the yield strength in shear. Equation 8 makes an attempt at incorporating such a bound and still provides some influence of the lead compliancy by using lead height H; however, there can be a discontinuity between Eq. 4 and Eq. 8.

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{h}{L_D\Delta\alpha\Delta T_e}\frac{(200\ \text{psi})\ H}{2\tau_\gamma h}\right]^{-\frac{1}{c}} \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}}$$

$$\text{if } \Delta\tau = \frac{K_D L_D \Delta\alpha\Delta T_e}{A} > 2\tau_\gamma \qquad (8)$$

where

- H = lead height from component attachment to solder joint plus h,
- τ_γ = yield strength in shear for solder, assuming τ_γ = ~ 1/5 to 1/10 shear strength @ 50°C and low strain rates => τ_γ = ~ 500 to 250 psi,
- $\Delta\tau$ = cyclic shear stress range.

For very large thermal expansion mismatches the full displacements will not be transmitted to the solder joints; possible exceptions are situations where very stiff leads are present as well, in which case the solder joint reliability is best estimated using Eq. 3 for leadless solder attachments. Under the assumption that a strain range of no more than $\Delta\gamma_{max}$ can be accommodated by creep and stress relaxation in the solder joints, a possible estimate for the reliability for designs with very large thermal expansion mismatches might be

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{1}{\Delta\gamma_{max}}\frac{(200\ \text{psi})\ A}{K_D L_D \Delta\alpha\Delta T_e}\right]^{-\frac{1}{c}} \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}}$$

$$\text{if } \Delta\gamma = \frac{L_D\Delta\alpha\Delta T_e}{h} > \Delta\gamma_{max} \qquad (9)$$

It should be noted that Eq. 9 does not really describe what physically happens at a solder joint under these conditions; it only attempts to limit significant overestimates of the cyclic fatigue damage.

Under these circumstances, Eqs. 3 and 4 will provide lower and upper bounds for the reliability estimates, respectively. The higher the lead stiffness, the closer the expected results will be towards the results given by Eq. 3 for the leadless, infinitely stiff leads, solder attachments. Very high lead stiffnesses can occur in the case of through-hole component leads converted to surface mounting and for connector headers where the male header pins have been simply bent into a gull-wing lead foot without any reduction in the lead cross-section. Very high thermal expansion mismatches occur primarily in accelerated testing and in extraordinary environments like storage and transport for products that are designed for benign operating environments.

4.4 Acceleration Factors/Acceleration Transform In order to relate the results of accelerated tests to use conditions or even to compare the results from different accelerated test conditions, test acceleration factors need to be known. For the typical accelerated tests acceleration factors from test to use conditions are based either on the numbers of cycles

$$A.F.(N) = \frac{N_f\ (\text{use, } 50\%)}{N_f\ (\text{test, } 50\%)} \qquad (10)$$

or the mean-time-to-failure (MTTF)

$$A.F.(t) = \frac{MTTF\ (\text{use})}{MTTF\ (\text{test})} = A.F.(N)\ \frac{f\ (\text{use})}{f\ (\text{test})} \qquad (11)$$

where f(use) and f(test) are the cyclic frequencies during operation and testing, respectively.

Given the complex time-, temperature- and stress-dependent behavior of solder, simple acceleration factors are not possible, and an acceleration transform relationship is required. This acceleration transform allows the extrapolation of accelerated test results to predict the reliability of the product in use. It also makes possible the valid comparison of accelerated test results from tests with different test conditions, as long as the primary damage mechanism, creep-fatigue, is the same.

From Equations 3 through 5, an acceleration transform results if the equations are applied to two thermal cyclic conditions, denoted by (1) and (2), and the equations are divided into each other. These conditions (1) and (2), can be either use or test conditions and the acceleration transform derives a cycle number for condition (2), $N_f(2)$, that is equivalent to the cycle number at condition (1), $N_f(1)$, at the same failure probability:

$$N_f\,(2,50\%) = \frac{1}{2}\left[[2N_f(1,50\%)]^{c(1)}\frac{\Delta D(2)}{\Delta D(1)}\right]^{\frac{1}{c(2)}} \quad (12)$$

where for leadless surface mount attachments

$$\Delta D = \left[\frac{F}{2\varepsilon_f'}\,\frac{L_D\Delta\alpha\Delta T_e}{h}\right] \quad (13)$$

and for leaded surface mount attachments

$$\Delta D = \left[\frac{F}{2\varepsilon_f'}\,\frac{K_D(L_D\Delta\alpha\Delta T_e)^2}{(200\text{psi})Ah}\right] \quad (14)$$

and where ΔD = potential cyclic fatigue damage at complete stress relaxation. Since the damage terms are in ratio form in the acceleration transform, the parameters that are the same for the two conditions which are compared will cancel.

The validity of the acceleration transform has been demonstrated by comparing and correlating the results of accelerated reliability tests carried out at different temperatures and cycle dwell times.

From this acceleration transform the acceleration factor between these two specific conditions can be determined.

$$A.F.(N) = \frac{N_f\,(\text{use, }50\%)}{N_f\,(\text{test, }50\%)} = \frac{[\Delta D(\text{use})]^{\frac{1}{c(\text{use})}}}{[\Delta D(\text{test})]^{\frac{1}{c(\text{test})}}} \quad (15)$$

In Table 2 the information from Table 1 is combined with some hypothetical example use conditions and used in Eqs. 12, 13, and 14 together with the Weibull statistical distributions to determine some equivalent mean cyclic lives for the accelerated test conditions recommended in Table 1 for both leadless and leaded surface mount solder attachments. These equivalent test cycles are determined for the range of Years of Service and the Acceptable Failure Risks in Table 1, but are the expected mean cycles to failure for the test conditions.

The results in Table 2 show that for the more benign use conditions (Use Categories 1 through 6), the test regimes provide high acceleration factors (see also Eq. 11) ranging from 75 to 4. For the more severe use conditions, the test accelerations diminish or disappear entirely. This is the result of a number of reasons, such as severe thermal use conditions, long service lives, and low tolerances for failure acting singly or in concert. This reflects the fact that for these conditions the reliability of the products cannot be experimentally verified; reliability assurance has to depend solely on analytical reliability modeling.

4.5 Statistical Considerations The failures of surface mount solder joints depend equally on the physical causes of the accumulating creep-fatigue damage and on associated probabilities of failure. Like other wearout failures, failures of surface mount solder attachments occur distributed over a relatively large life range. This is not the result of some physical differences between solder joints, at least not on the macro-level, but the result of random chance. Wearout failures typically are best linearized using the Weibull statistical distribution. This is already reflected in Eqs. 3 and 4 where the right-most term represents the Weibull statistical distribution for the complete surface mount solder attachment of a component or connector.

Solder joints are not uniformly subject to the same thermal expansion mismatch, and thus the same amount of fatigue damage, because of their different distances from the neutral point of the component or connector. Therefore, the total number of solder joints cannot be counted as the sample size. For test purposes and depending on size and symmetry, a given component or connector can be partitioned into two or four samples, if the continuity nets are correspondingly designed. However, treating each solder joint as an individual sample assumes incorrectly that they all have the same failure probability.

This is not to say that not all solder joints make a contribution to the failure probability of the entire solder attachment of the component or connector; they indeed do. However, it is very difficult and not very practical to account for these contributions individually. Equations 3 and 4 are written for the solder joints experiencing the most cyclic fatigue damage, the corner joints. The contributions to the solder attachment failure probability of the other solder joints is implicitly included in Eqs. 3 and 4, since these equations are based on experimental results from components for which essentially all solder joints were included in the continuity daisy-chains.

Therefore, the partitioning of the test samples needs to include essentially all solder joints into the continuity daisy-chain with each partition having an equal likelihood of failure. In particular, each partitioned daisy-chain needs to include the same number of corner joints. For tests for which access to the interior of the components is needed for functional powered cycling, solder joints with the least damage contributions, those closest to the neutral point, should be chosen for this purpose and therefore be excluded from the continuity daisy-chain.

Table 2 Equivalent Mean Accelerated Test Cycles for Surface Mount Solder Attachments for the Use Categories in Table 1
(Unless otherwise indicated the use conditions are as shown in Table 1)

	EXAMPLE USE CONDITIONS						ACCELERATED TESTING					
USE CATEGORY	Tmin °C	Tmax °C	ΔT °C	t_D hrs	Yearly cycles	Risk %	Tmin °C	Tmax °C	ΔT °C	t_D min	Service Life Equivalent Cycles,(1) N(test,50%)	
1) CONSUMER	+20	+55	35	12	365	1	+25	+100	75	15	1 year ll 320 ld 170	3 years ll 1050 ld 550
2) COMPUTERS	+25	+45	20	2	1460	0.1	+25	+100	75	15	1 year ll 470 ld 113	5 years ll 2500 ld 600
3) TELECOMM	+10	+45	35	12	365	0.01	+0	+100	100	15	7 years ll 4700 ld 4100	20 years ll 14600 ld 12900
4) COMMERCIAL AIRCRAFT	+20	+40	20	12	365	0.001	0	+100	100	15	1 year ll 280 ld 120	20 years ll 7400 ld 3200
5) INDUSTRIAL AUTOMOTIVE PASSENGER COMPARTMENT	+30 +20 -5 15	+50 +60 +55 +65	20 &40 &60 &80	12 12 12 12	185 100 60 20	0.1	0	+100	100	15	1 year ll 400 ld 660	10 years ll 5000 ld 8000
6) MILITARY GROUND & SHIP	+5 -20	+45 +40	40 &60	12 12	100 265	0.1	0	+100	100	15	1 year ll 740 ld 1120	10 years ll 8500 ld 13000
7) SPACE											5 years	30 years
leo	20	+55	35	1	8760	0.001	0	+100	100	15	ll 5900 ld 77000	ll 350000 ld 460000
geo	+20	+55	35	12	365	0.001	0	+100	100	15	ll 7100 ld 12200	ll 51000 ld 87000
8) MILITARY AVIONICS											1 year	10 years
a	+25 +20	+65 +40	40 &20	2 1	365 365	0.01	0	+100	100	15	ll 870 ld 290	ll 4800 ld 2800
b	+15 +20	+75 +40	60 &20	2 1	365 365	0.01	0	+100	100	15	ll 1020 ld 1600	ll 11900 ld 19000
c	0 +20	+80 +40	80 &20	2 1	365 365	0.01	0	+100	100	15	ll 2300 ld 6100	ll 22000 ld 70000
9) AUTOMOTIVE UNDER HOOD	+20 0 -20	+80 +100 +120	60 &100 &140	1 1 2	1000 300 40	0.1	0	+100	100	15	1 year ll 3500 ld 27000	5 years ll 19000 ld 150000

& = in addition, ll = leadless, ld = leaded

8700 test cycles = 1 year test time

1) The Equivalent Mean Cycles are not the necessary test duration. The actual test durations are reduced by increasing the sample size and larger test accelerations resuting from 1) increased $\Delta\alpha$ for the test vehicles, purposely mismatching the CTEs of components and test substrates, and/or shorter 2) test dwell times, t_D, possible with test facilities designed to provide uniform temperatures even for shorter dwells. The 15 minute dwells are for standard commercial environmental chambers.

For example, a sample size of n = 32 reduces the number of cycles to N(test,3%)= 0.46 N(test,50%) and 0.21 N(test,50%) for leadless SMT attachments with $\beta = 4$ and leaded solder attachments with $\beta = 2$, respectively (see Eq. 17). A doubling in $a\Delta\alpha(2) = 2\ \Delta\alpha(1)$ produces for 0 to 100°C cycling at $t_D = 15$ minutes, $N_f(2,50\%) = 0.19$, $N_f(1,50\%)$ and $0.036\ N_f(1,50\%)$ for leadless and leaded surface mount attachments, respectively (Eq. 12). A decrease in $t_D(1) = 15$ min to $t_D(2) = 5$ min results in a cycle increase of $N_f(2,50\%) = 1.59\ N_f(1,50\%)$, but a decrease in test time MTTF(2) = 0.53, MTTF(1) (see Eqs. 12 and 11).

Results from tests with partitioned components or connectors need to be corrected for this partitioning, however. The correction needs to be carried using

$$N_f(\text{component}) = N_f(\text{m partitions}) \left[\frac{1}{m}\right]^{\frac{1}{\beta}} \quad (16)$$

The sample size depends on the purpose and duration of the accelerated reliability test. For tests for which the test duration is long enough to allow at least half of the samples to have failed, a minimum sample size of 32 is recommended.

Tests of shorter duration to establish certain reliability (maximum cumulative failure probability) levels require the trade-off of larger sample sizes for shorter test times. This trade-off can be made using the equation

$$N(\text{test},n,x\%) = N(\text{test},x\%) \left[\left[\frac{\ln(0.5)}{\ln(1-0.01x)}\right]^{\frac{c(\text{use})}{c(\text{test})}} \left[\frac{\ln\left(1-\frac{1}{n}\right)}{\ln(0.5)}\right]\right]^{\frac{1}{\beta}} \quad (17)$$

where N(test),x%) is obtained from

$$N(\text{test},x\%) = \frac{1}{2}\left[[2N(\text{use},x\%)]^{c(\text{use})}\frac{\Delta D(\text{test})}{\Delta D(\text{use})}\right]^{\frac{1}{c(\text{test})}} \quad (18)$$

and where

N(test,n,x%) = number of minimum failure-free test cycles to confirm a maximum cumulative failure probability of x% with n samples on test,

N(test,x%) = equivalent mean cycles to failure in the test (see Table 2)

x = allowable maximum failure probability, %,

c(use) = fatigue ductility exponent for use conditions from Eq. 5,

c(test) = fatigue ductility exponent for test conditions from Eq. 5,

n = number of independently monitored test samples on test,

β = slope of Weibull statistical failure distribution,

N = product design life with an acceptable cumulative failure probability of x%,

ΔD(test) = cyclic fatigue damage term for test parameters from Eqs. 13 or 14,

ΔD(use) = cyclic fatigue damage term for use parameters from Eqs. 13 or 14.

Equation 17 gives the minimum number of the failure-free test cycles that are necessary to assure a cumulative failure probability, x, with n individually monitored components on test at the end of the product design life.

5.0 DESIGN FOR SOLDER ATTACHMENT RELIABILITY

5.1 Primary Design Parameters The design parameters that have been identified to have a primary (order of magnitude) influence on SM solder attachment fatigue reliability are (also see Nomenclature and Definitions):

5.1.1 Component Size The physical size of the component determines the amount of displacement a solder joint experiences during thermal expansion/contraction of the component and the substrate to which it is soldered. Larger components are larger threats to reliability.

5.1.2 Attachment Type The choice of attachment type (leadless or leaded) determines the maximum stress level that can be experienced in a solder joint during thermal cycling. The stiff leadless attachments typically stress the solder beyond the yield strength, whereas compliant leaded attachments typically do not. This choice determines the reliability model that needs to be applied and affects the statistical failure distribution (Weibull slope). Leaded attachments provide larger reliability margins, which increase with decreasing lead stiffness.

5.1.3 Solder Joint Height The solder joint height determines the strain level experienced in the solder joint for a given component/substrate displacement. It results from the solder-filled gap between the component metallization or component lead and the substrate pad. Higher solder columns reduce the strains in the solder joints and increase reliability. Solder joint height is not the height of the fillet.

5.1.4 Solder Joint Area The solder joint area determines the stresses in a solder joint resulting from a given component/substrate displacement. It is of importance primarily for compliant leaded attachments. Larger solder joint areas reduce the applied stresses and increase reliability; however, the possible range of effective increase in area is very limited.

5.1.5 Lead Stiffness The lead stiffness determines the forces resulting from a given component/substrate displacement. Because the corner solder joints experience the largest displacements and the displacements are in the direction of the component center (neutral point), it is the diagonal lead stiffness which is of primary importance. Lower lead stiffness results in increased reliability.

5.1.6 Coefficient of Thermal Expansion The linear coefficient of thermal expansion (CTE) represents the change in linear dimension of a material due to a change in its temperature. Components and substrates consist typically of a variety of materials all having different CTEs; the effective CTEs are a combination of the individual material CTEs and typically are different in different directions of

components and substrates. CTEs need to be measured for both product and test vehicles to avoid possible large errors in the reliability predictions.

5.1.7 CTE—Mismatch The CTE-mismatch ($\Delta\alpha$) is the difference between the coefficients of thermal expansion (CTE) of two materials or parts joined together; in most instances it is the CTE-mismatch between component and substrate that is most important while the CTE-mismatch between the solder and the materials to which it is bonded (ceramic, Alloy 42, Kovar) plays a smaller, but not negligible, role. In some designs (ceramic component on ceramic or silicon substrate), this CTE-mismatch assumes primary importance (see Solder/Base-Material CTE Mismatch, 5.2.1). Large CTE mismatches pose large reliability threats; the effect of power dissipation within components makes CTE matching not the optimum solution.

5.1.8 Cyclic Temperature Swing The cyclic temperature swing (ΔT) of components and substrate is the difference in the maximum and minimum steady-state temperatures experienced during either externally (daily) imposed temperature variations or operationally (on/off, load fluctuations) imposed variations. It needs to be realized that the temperature swing of the components is typically not the same as the temperature swing of the substrate due to the power dissipated in active devices. An effective temperature swing (ΔT_e) can be used for simplicity by incorporating the CTE-mismatch between component and substrate (see Cyclic Expansion Mismatch, 5.1.9). Smaller ΔTs result in improved reliability.

5.1.9 Cyclic Expansion Mismatch The cyclic expansion mismatch ($\Delta\alpha\Delta T_e$) results from the difference in the thermal expansion of components and substrate which are determined by the respective thermal expansion coefficients (CTE) and cyclic temperature swings (ΔT). Smaller expansion mismatches result in improved reliability.

5.2 Secondary Design Parameters While the effects of secondary design parameters are, by themselves, of second-order (factors of 2 to 3) importance, their additional contribution to the effects of the first-order parameters can be significant. The effect of some of these second-order parameters might be different in accelerated testing and actual operational use.

Design parameters having second-order effects on solder joint reliability are as follows:

5.2.1 Solder/Base-Material CTE-Mismatch The CTE-mismatch ($\Delta\alpha$) between the solder and some base materials (ceramic, Alloy 42, Kovar, silicon) can make substantial contributions to the cyclic fatigue damage (see 5.1.7).

5.2.2 Solder Joint Shape/Fillet/Volume Experimental evidence indicates that solder joint shape/fillet/volume may effect reliability. In some highly accelerated tests cyclic life improvements of about a factor of two have been achieved, but it is not clear whether even these small benefits would result for the slower conditions prevalent in most product operations. The improvements result from the time necessary for crack propagation through the fillet.

5.2.3 Solder Joint Uniformity Some experiments in which solder joints were loaded primarily in a strength-driven mode (high cyclic frequencies, no hold times, very large temperature swings with fast transitions) showed the need for extreme uniformity of all the solder joints of a component to avoid unequal stressing; accelerated tests utilizing test conditions more closely resembling product use conditions did not reveal a need for extraordinary solder joint uniformity.

5.2.4 Initial Solder Joint Grain Structure A fine initial grain structure in solder joints results in cyclic life improvements of about a factor of two in highly accelerated tests. The grain structure of solder is inherently unstable and will grow with time; higher temperatures and cyclic loading accelerate the grain growth. Thus, for most product applications a fine initial grain structure will not result in a significant improvement of fatigue life; the solder joints of accelerated test vehicles should be artificially aged to start the tests with more product related grain structures.

5.2.5 Conformal Coating Conformal coating can have different effects on solder joint life during thermal cycling depending on the type of material, thickness, and location. The advantage of conformal coating is that it slows the absorption of water and oxygen into surface cracks. The presence of oxides on the cracked surfaces may accelerate the crack propagation. Oxidation layers prevent ''re-welding'' of the solder during crack closure.

On the negative side, conformal coats may add another material with a very high thermal coefficient of expansion which may influence reliability. This addition can be significant especially if the coating wicks under components, filling the gap between the PB and component. In addition, some conformal coats can become rigid below the glass transition temperature. This condition can exert considerable stress on the components and solder joints during the thermal cycles.

Because of the large variation in conformal coating material properties, thickness applied, methods of application, etc., the effect of conformal coating, in general, needs to be evaluated empirically for each application.

5.2.6 Compliant Substrate Surface Layers Compliant layers at substrate surfaces can provide additional reliability margins, but by themselves are not adequate to counteract the effects of large expansion mismatches.

5.2.7 Solder Composition The most widely used solder compositions are eutectic and 60-40 tin-lead solder. Solder compositions other than these can have somewhat higher or lower fatigue reliability and are, on the whole, significantly less well characterized.

6.0 MANUFACTURE/PROCESSES

6.1 Process Control and Verification Visual inspection of SMT solder joints is not only difficult, it is also not very effective. It is unlikely that more than 70% of the defects can be found. This means that even double inspection will not catch more than 91% of the defects.

The best way to control the product is by process control, and specifically, by statistical process control (see IPC-PC-90). By applying SPC the product can be made acceptable in the low part per million range (e.g., 50 ppm – 0.005%), which is far below the level of inspectability.

To do this, process capability studies must be performed, which provide information on all parameters affecting the process. The process effects of every variable must be assessed and its influence on the product distribution determined. The process controls are then set-up to bring the distribution within acceptable limits, by adjusting the variables and keeping these within the appropriate limits. This way, the product is controlled by the process, rather than by inspection or measurements on the product.

Verification is accomplished by monitoring trends and distributions, to be well within the control limits. Sampling of the product is possible but should concentrate on the details of the control parameters, rather than on visual inspection.

6.2 Consequences of Defects The consequences of defects, either in the fabrication of the test substrate or the solder joints, must be taken into consideration in the construction of the test (see J-STD-001). If the purpose of the test is to verify a new design or fabrication process then the presence of defects could potentially mask the actual performance of the test vehicle (e.g., partial non-wetting could cause premature solder joint failures which could be misconstrued as a failure of the original design).

On the other hand, if the purpose of the test is to determine the effect of a given defect type on hardware reliability, the presence of certain types of defects may not only be desirable, but required. It should be noted, however, that this type of testing is difficult to control. The defects under study must be produced in a manner that mimics the actual situation while at the same time assures a sufficient number of defects to allow a statistically significant test.

6.2.1 Wetting Defects Poor wetting of the components or conductors can impact reliability test results in a number of ways (see IPC-S-816, J-STD-001, J-STD-002 and J-STD-003):

a) Poor wetting can cause insufficient solder joint formation yielding poor reliability in mechanical or fatigue testing.

   Additionally, ''spotty'' wetting can result in the formation of stress risers which can greatly influence life test results.

b) Poor wetting is an indication of poor metallurgical bonding between the items being soldered. As a result of this incomplete bonding, poor mechanical test results will be observed in mechanical and fatigue tests.

c) In extreme cases, non-wetting will allow for unprotected base metal to be exposed to subsequent processing. This can result in subsequent failures related to corrosion and metallurgical/chemical contamination.

Inadequate wetting can be caused by solderability problems due to surface contamination and oxidation, by inadequate formation of intermetallic compounds due to reflow processes with inadequate temperatures and/or time, and by improper choices of materials.

6.2.2 Surface Contamination Effects Contamination of component terminations or surface mounting pads, before soldering, may prevent a good solder joint from being formed.

Typical detrimental contaminants are silicone oils, mineral oils, vegetable oils, waxes and greases, which may originate from handling, finger prints, hand lotions, foods (chocolate, oranges, soft drinks, etc.), oxides, sulfides, and carbonates from atmospheric corrosion.

Contaminants on the solder joint, after soldering, may cause corrosion (halides, flux activators, cleaning agents).

6.2.3 Effects of Solder Contamination Contamination of the solder can radically effect the visual and mechanical characteristics of the solder joint. This contamination may come from a variety of sources:

1. Initial contamination of the raw materials, such as solder or solder paste.
2. Component termination metallizations such as gold or silver, or base metals such as copper, may dissolve in the solder during soldering and further build up the contamination level as more components pass through the solder.
3. Subsequent diffusion of the metallization or base metals into the solder may increase the intermetallic diffusion layer.

4. Tooling, such as un-anodized aluminum solder fixtures, may dissolve in the solder during the soldering process.

5. Metallurgical contamination of the substrate, such as the copper electroplating of the printed board (PB), may affect the solder joint, e.g., cause dewetting.

Contamination	*Effects*
Copper (>0.3%)	Sluggish solder flow, increased hardness with corresponding decrease in fatigue life.
Gold (>0.2%)	Solder becomes increasingly brittle and granular in appearance.
Aluminum (>0.006%)	Solder becomes increasingly porous and takes on a frosty appearance.
Silver (>5%)	Dull appearance and decreased flow during solder operations.
Nickel (>0.1%)	Can form blisters in solder and create hard intermetallic compounds which can, in turn, act as stress risers during fatigue cycling.

6.2.4 Solder Volume Increases over the ''norm'' in the volume of solder will affect the apparent properties of the solder joints in a number of ways:

Type of Increase	*Effects on Apparent Properties*
Joint Height	Fatigue life would increase due to the decreased strain seen in the solder joint. Mechanical strength results may decrease somewhat due to the diminished effect of the intermetallics formed at the junction of the solder and the base material.
Fillet Volume	Performance in both mechanical and fatigue tests can be increased with solder volume. Increased solder volume increases both mechanical strength (especially in shear testing) and fatigue life (due to increased crack length required to achieve fracture.) However, large fillets may fracture components, such as chip capacitors, as the result of higher stresses on the components.

Similarly, decreases over the ''norm'' in the volume of solder will affect the apparent properties of the solder joints in a number of ways:

Type of Decrease	*Effects on Apparent Properties*
Insufficient solder (fillet)	Insufficient solder fillet volume will decrease the mechanical strength of the solder joint. It should be noted that properly wetted solder joints have ample mechanical strength. Thus, any decrease in mechanical strength is not likely to be significant.
Voids	Voids in the fillet area can decrease the mechanical strength and heat transfer properties of the solder connection. The extent of this effect is a function of the size, and the number and location of the voids. It should be noted that when thermal characteristics of the solder joint are critical, the presence of solder voids can be rather important. This effect is most noticeable on thermal pads under components with no external fillets.

6.2.5 Effects of Solder Joint Touch Up, Printed Board Assembly (PBA) Rework, and Repair ''Touch up'' is the application of heat and solder to a solder joint which is deemed cosmetically imperfect. Rework is the correction of a defect before the SM PBA leaves the plant. Repair is the correction of a defect found in the field. Information on rework and repair may be found in IPC-R-700. Each correction requires the heating of one or more solder joints above the liquidus temperature of lead-tin eutectic solder (183°C) and may involve the removal and replacement of a component. Note that this temperature of 183°C is well above the following critical temperatures in an SM printed board assembly:

Paragraphs 6.2.5.1 through 6.2.5.6 deal with temperature influences; paragraphs 6.2.5.7 through 6.2.5.11 deal with other related rework and repair concerns.

6.2.5.1 Glass Transition Temperature for Printed Boards The glass transition temperature (T_g) of most epoxy-glass boards is ~125°C. This T_g is greater for polyimide glass printed boards which have a T_g of ~270°. There are many other printed board materials that fall between these two extremes. Exceeding the T_g of the printed board results in significant expansion of the board in the Z plane, hence in stresses in the barrels of plated through-holes and vias; the result can be barrel fractures causing intermittent or permanent opens. The intermittent opens can generally be detected during temperature changes of the PBA. Exceeding the T_g of the printed board also results in expansion of the printed board assembly in the X-Y plane, which puts strain on solder joints.

Printed boards with a lower T_g, such as epoxy-glass boards, when heated locally, as during component removal or component replacement, to temperatures $>T_g$, will tend to bulge in the heated area. The solder joints of the replacement component will be under tension and may fail when the assembly cools down.

6.2.5.2 Intermetallic Compound Growth The copper in the printed board conductors and component leads has excellent solubility with the tin in the solder. As a consequence, clean copper has excellent solderability. Tin and copper react rapidly to form intermetallic compounds (IMCs) such as Cu_3Sn and Cu_6Sn_5 at elevated temperatures. Extended exposure to elevated temperatures leads to the formation of excessive amounts of IMCs. The original solder adjacent to the IMC layer will be depleted of tin leading to a lead-rich layer. For thin solder layers, the lead-rich layer is exposed and oxidized; this lead oxide renders that surface unsolderable.

In solder joints the brittle IMC layer will tend to act as a shear plane under tensile overload conditions.

If the molten solder is removed from the land by wiping, the exposed IMC layers can rapidly oxidize and become unsolderable.

If the heat source is solder (wave or fountain), the intermetallics will be carried away as they form and in the extreme, the copper land will be dissolved.

6.2.5.3 Glass Transition Temperature for Plastic Encapsulates The T_g range of most moulding compounds used in the plastic encapsulation of semiconductors and passive networks is ~ 150°C-180°C.

Exceeding the T_g of the moulding compound of the components during component removal results in internal stresses to the metallization and passivation of the silicon chip. This damage can hinder failure analysis of the removed component and can also be suffered by a neighboring component. Disruption of the metallization can result in opens and dysfunction of the chip. Damage to the passivation can result in long term corrosion of, and opens in, the metal. Exceeding the T_g can also cause delamination of the moulding compound from the surface of the silicon chip or the surfaces of the leadframe; condensed moisture can pool in the delaminated sites and lead to dendrites and corrosion. Where the delamination coincides with bonding pads and wire bonds, bond shear can occur.

When using hot gas or IR systems to remove or replace components, if subsequent failure analysis is to be performed on the removed component, dry the component prior to removal. Keep the heat away from neighboring components and joints with hot air deflectors and IR shielding panels.

6.2.5.4 Vapor Pressure Effects on Plastic Encapsulated Components Condensed water vapor at the interfaces within a plastic encapsulated surface mount component (PSMC) rapidly turns into steam and can cause delamination between the moulding compound and various elements such as the leadframe, the bonding fingers, or the chip/die surface. This phenomena normally occurs at ~ 220°C. In extremely susceptible components, the threshold temperature is expected to be lower than 220°C. In the worst case the delamination of the moulding compound can progress to a continuous crack between the die and the exterior surface of the package, permitting materials such as flux and cleaning solvents to enter the package.

These materials, in the presence of water, corrode the metallization of the die; in the additional presence of DC bias, dendrites can form between conductors. Even when there are NO external cracks, ionizable substances can be extracted from the moulding compound or from the surface of the chip (such as from phosphorous doped oxide); these materials, together with condensed water are trapped in the delaminated regions and over time, result in corrosion and dendrites.

When using hot gas or IR systems to remove or replace components, particularly if subsequent failure analysis is to be performed on the removed component, dry the component prior to removal. Hot air deflectors and IR shielding keep the heat away from the neighboring components and joints. Where hot gas or IR has been used to remove a component and the body temperature has exceeded ~ 260°C for 10 seconds, the re-use of that component is not advised, particularly if the component is susceptible to plastic package cracking and has NOT been dried out prior to removal.

Characterize replacement parts for plastic package cracking susceptibility by the procedures in IPC-SM-786 or IPC-TM-650, method 2.6.20.

6.2.5.5 Vapor Pressure Effects on Printed Boards The glass-epoxy or glass-polymer interface can separate or delaminate, resulting in ''measling,'' when heated above ~ 260°C for extended periods. This phenomena occurs at the 260°C temperature for glass epoxy boards and lower temperatures for glass polyimide boards that have been exposed to moist environments. Conductive Anodic Filaments (CAF) can form low or high resistance conductive paths between the barrels of the vias or PTH. Most glass-polymer printed board materials should have been evaluated at 260°C for measling during the ''solder float test.'' Increased susceptibility to measling or delamination is noted when the polymer has a significant moisture content; polyimide or polyimide-based substrates should be dried prior to high temperature exposure.

When using hot gas, IR, or manual iron systems to remove or replace components, oven dry the substrate at 125°C for 24 hours prior to high temperature exposure and minimize printed board time at temperature. Use thermometry to measure and control the temperature of the substrate and

the component during removal and replacement; gas stream temperatures >350°C have been noted in systems setup for rapid component removal.

6.2.5.6 Solder Melt Temperature Effects At the temperatures required to melt solder, the adhesive binding the copper conductor to the printed board weakens. Aggressive use of a soldering iron to move or remove solder or to move a component lead by lifting, prodding or twisting before the solder is completely melted can result in the bending, tearing or complete failure of a land or conductor; conductor repair is then necessary. The same land or conductor damage follows premature lifting or twisting of a component prior to complete solder melting.

6.2.5.7 Temperature Excursion (ΔT) and Temperature Rate of Change (dT/dt) If molten solder contacts the termination of a multilayer ceramic capacitor (MLCC), multilayer ceramic inductor, or multilayer ceramic filter network, during ''touch up,'' rework or repair, and results in a thermal transient exceeding about 4°C/second, cracks may result due to thermal shock. The crack occurs in the ceramic body under the termination, hidden from visual inspection but capable of being a site for dendriting under conditions of moisture and bias. Most MLCC suppliers recommend a ΔT <100°C. Some soldering irons, set at 800°F or 427°C, with sufficient thermal mass in the tip, and with a tip wet with solder will transfer heat so rapidly that the ceramic under the termination will crack. Preheating of the component above 150°C may be required to avoid this kind of cracking but may result in damage to other components or the printed board. The issue of thermal shock cracking for MLCCs is worst case for capacitors with high values and high thickness; other parameters which correspond to thermal shock susceptibility are high layer count, high dielectric constant or low working voltage rating. Require your component supplier to provide data regarding the ΔT and dT/dt to which the particular capacitor (dielectric type, value, working voltage, case style, temperature coefficient of capacitance) is robust; this data may restrict your choice of component values (parameters) or suppliers.

6.2.5.8 Printed Board Assembly Cleanliness Where water soluble or other fluxes are used, assure that the PBA is cleaned at least to the ionic contamination levels expected of a first-pass board. Otherwise, long term failure mechanisms may result, corrosion stress cracking of the solder joints may occur, together with dendrites on the surface of the printed board and loss of surface insulation resistance performance (particularly important in high impedance linear applications). See also the comments on cleaning under ''Conformal Coating.''

6.2.5.9 Printed Board Assembly Flexure Excessive flexure of the PBA due to shock, vibration or handling during rework or repair can result in a cracked component body, a detached termination, or overloaded and failed solder joints.

6.2.5.10 Tooling Impact Impact of a hard tool on a ceramic component body or termination can result in a cracked or fractured component body.

6.2.5.11 Electrostatic Discharge (ESD) Observe ESD precautions while handling, testing, and transporting the PBA to avoid the introduction of infant and latent defects.

6.3 Material Properties Materials commonly used in the fabrication of printed wiring assemblies often exhibit widely different material properties, as a function of the temperature at which the material is being used. As a result, the tester must be careful in choosing an environment for accelerated testing that will not cause unexpected changes in material properties and impact test validity.

6.3.1 Solder Properties Solder exhibits large variations in shear strength, elongation and creep rupture life as a function of both temperature and strain rate. An example of this variation is shown in Figure 8, comparing the shear strengths of 60/40 solder at various temperatures and strain rates. Solder typically loses strength and gains ductility with increasing temperature and decreasing strain rate.

The solder must be given adequate time for the stress in the joint to dissipate for the full impact of a thermal cycle to be felt. As a result, dwell times at low temperatures have to be significantly higher than high temperature dwells to allow for the complete stress relaxation of the solder joints.

6.3.2 Conformal Coating Materials Some conformal coating materials such as silicone or paraxylene are reported to improve the life of solder joints in temperature cycling, presumably by performing either as a mechanical reinforcement or as a gas-tight seal.

Some diodes with glass bodies which were conformally coated have cracked when the ambient temperature exceeded the glass transition temperature, T_g, and the material did not soften enough to cushion the stress on the glass. Some flip chip assemblies use very soft gels with very low T_g to minimize expansion stresses on the solder joints. Conformal coating materials are generally unfilled. This condition usually results in a very high CTE, particularly above T_g, which is important if your product must survive excursions into this temperature range, either during service or qualification testing.

The conformal coating/junction coating material suppliers usually have data on the T_g and CTE of their material; if this data does not appear on the data sheet, you may have to ask for it specifically. CTEs below T_g for acrylics and

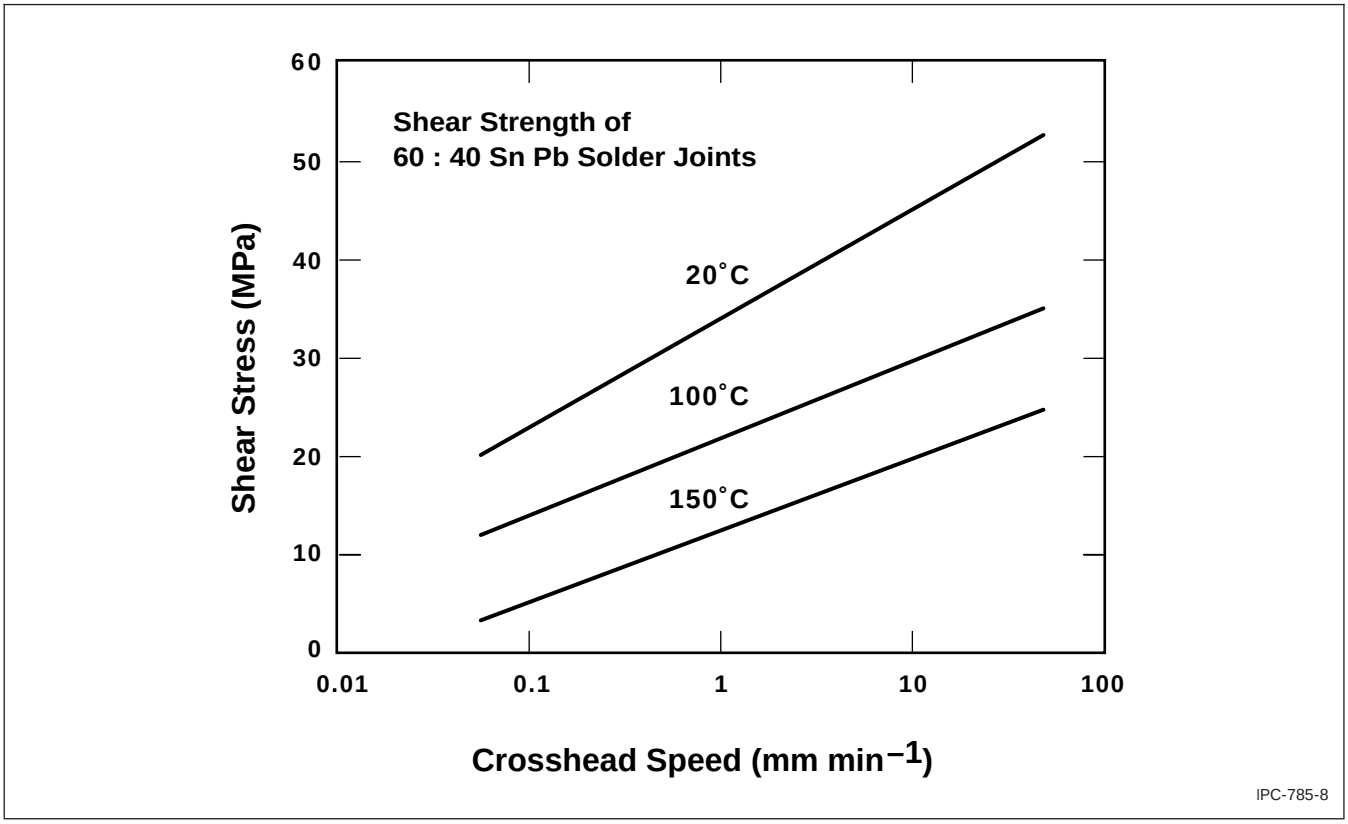

Figure 8 Shear strengths of 60:40 SnPb solder as a function of temperature and strain rate

epoxies range from 40–90 ppm/°C while CTEs for polyurethanes and silicones range from 100–300 ppm/°C. Examine data on modulus and hardness as a function of temperature over your range of interest, since these parameters increase with decreasing temperature for most polymers. The hardness of some silicones changes very rapidly below –20°C.

Before re-application of any conformal coating, the surface of the PBA and the components must be free of material (water-soluble, greasy, oily or particulate) which might act as a release or parting agent; otherwise, mealing or vesication will occur with subsequent corrosion and dendriting where conductors are exposed or bridged.

6.3.3 Component Properties Required for assessment and prediction of solder attachment reliability are CTE values for materials common to components and their packaging. These values are listed in Table 3 and should be taken as guidelines only. Actual CTE values need to be obtained by measurement.

The CTE values (ppm/,°C) were taken from material in ''Technology Assessment of Laminates,'' IPC-TA-720, Materials for High Density Electronic Packaging and Interconnection, ''Thermal Expansion Properties,'' chapter of ''Electronic Materials Handbook, Volume 1, Packaging,'' and commercial literature.

The CTE ''value'' of a packaged component can vary depending on the geometry, the ratio of polymeric materials to inorganic materials, and orientation axis along which the CTE is measured.

Package CTE values may be evaluated on small physical samples with a thermal-mechanical analyzer. CTE values may have to be evaluated on larger size samples and complete packages with a dilatometer, available from several companies who can, in many cases, also provide measurement services. These systems require cooling (mechanical refrigeration or vaporization of liquified gases) to be sufficiently thermally stable at temperatures near 25°C or to function down to the -55°C range.

Also required for assessment and prediction of solder attachment reliability is the lead stiffness, K_D, for the leads of leaded components. These data may be obtained from the component supplier. The lead stiffness can be computed (see Refs. 8 to 11).

6.3.4 Printed Board Materials Required for the assessment and prediction of solder attachment reliability is the coefficient of thermal expansion (CTE) of the substrate in the x-y plane. Typical values are presented in Table 3 as guidelines only. Actual CTEs require measurement.

The CTE of the substrate must be well defined for effective modeling to take place. ''Textbook'' or literature data should not be used for this purpose as they often do not take into account the actual lay-up and materials used in the construction of a functioning printed board nor the

actual resin content achieved and may, therefore, lead to erroneous results.

A means of obtaining this information is through the use of strain gauging in both the x and y directions (significant differences have been measured) a representative printed board and passing the sample through a thermal excursion allowing the CTE to be measured directly (see IPC-TM-650, 2.4.41 and 2.4.41.1). Care should be taken to ensure that a representative printed board is used and that both sides of the part are measured to check for warpage effects as a result of unbalanced construction or delamination of the constraining member from the active part of the printed board.

The glass transition temperature of the material being used should also be known and should not be approached at any time during the test. The glass transition temperature is the temperature at which an amorphous polymer (or the amorphous regions in a partially crystalline polymer) will experience a rapid change in its mechanical properties (including CTE, yield and tensile strengths). Testing above this temperature will result in the material not only exhibiting non-representative mechanical properties during that portion of the test cycle but also, will often result in the overall degradation of the polymer during the test cycle.

Table 3 Typical Values for Coefficients of Thermal Expansion (PPM/°C)

Insulator/Substrate Material/System		CTE lower	CTE typical	CTE upper
E Glass			5.5	
S Glass			2.6	
Glass-Ceramic			>3.0	
Silicon			2.6	
Diamond			0.9	
Aluminum Nitride			4.5	
Silicon Nitride			3.7	
Quartz, fused silica		0.5		0.6
Kevlar 49			–5	
Beryllia			6	
Cubic Boron Nitride	X–Y Z		3.7 7.2	
E Glass/Epoxy	X–Y Z	14 55		20 90
E Glass/Polyimide	X–Y Z	12	 60	16
E Glass/PTFE	X–Y Z		24 260	
Kevlar/Epoxy	X–Y Z	 5.1		 7.1
Kevlar/Polyimide	X–Y Z	3.4	 83	6.7
Quartz/Polyimide	X–Y Z	5.0	 68.4	8.0
Quartz/Bismaleimide, 35% Resin	X-Y Z	6.2	 41	6.3
Alumina (90%) TFSubstrate			7.0	
Alumina (Ceramic Chip Carrier)		5.9	6.5	7.4
Epoxy (70% Silica) Plastic Packaging		20		23
Mullite Co-Fired			4.2	
Alloy 42			4.4	
Aluminum (40% Silicon)			13.5	
Aluminum, T6061			23.6	
Boron Aluminum (20%)			12.7	
Copper, CDA 101			17.6	
Copper/Invar/Copper 20/60/20 Thick		5.7		5.8
Copper/Molybdenum/copper 20/60/20 Thick			7	
Gold			14	
Graphite/Aluminum		4		6
Invar 36			1.6	
Invar 42			4.5	
Kovar			5	
Lead			29	
Lead (95%) Tin Solder			28	
Lead-Tin Solder 60/40		23		25
Molybdenum			4.9	
Ni-clad Molybdenum		5.2		6.0
Silver			19	
Tungsten/Copper (90/10)		6.0		6.5
Tungsten			4	

7.0 ACCELERATED RELIABILITY TESTING

The goal of an accelerated test is to produce failure or to accumulate damage by the same damage mechanism but in less time than would be required during the product use. There are several general ways of achieving this. The magnitude of the life controlling variable can be increased to decrease the life. The magnitude of the life controlling variable can be maintained at the value expected in a life test but applied more frequently, so that the test duration is decreased. It is also possible to do a combination of these two things.

It is important to understand what the life controlling variable (or variables) is, how it is influenced by the nature of the test being run, and how varying the rate and/or range of application of this variable influences the life. It is critical to understand the relationship between the accelerated test and the actual service condition being accelerated. Often the accelerated test produces a different type of failure or does not properly correspond to the actual service condition. As such, it would not be a valid acceleration and

should not be employed without a complete understanding of how this accelerated test correlates with the service condition. Without such an understanding, any inferences drawn from the accelerated test are likely to be highly misleading and should, therefore, not be used. As an example, it would be inappropriate to test from –55 to +125°C, if the service environment is within –20 to +100°C.

Although the use of accelerated testing can be dangerous because of the introduced uncertainties, it is generally unavoidable because the design life is too long to permit more realistic testing. It is therefore imperative to fully understand what the actual life controlling phenomenon is and how the accelerated test is related to the service condition.

Several different types of tests are available to emphasize different failure processes. Thermal fatigue, thermal shock, and/or vibration tests can be performed to accelerate failure mechanisms controlling the solder joint life. The selection of test type and test conditions should be based on the appropriate damage/failure mechanisms and service environment identified in Sections 3.4 and 3.5.

7.1 Reliability Program/Strategy Before embarking on a reliability program it is important that an understanding is reached as to the purpose of the program. The testing and analytical strategies can vary dramatically for different purposes. The definition of purpose will depend on how much is already known, what new information is required, what resources and how much time is available, what are the use conditions for the product, the design life, the tolerable failure risk, etc.

Figure 1 shows a flow chart with the steps and decisions that might be followed to carry out an appropriate reliability program.

For some use and loading conditions the quantitative understanding is not as yet adequate for analytical reliability prediction; even relating the results from accelerated tests to product reliability is beyond current capabilities for some loading conditions. For this reason, generic investigations into damage mechanisms might be necessary to develop appropriate reliability prediction models and acceleration factors/transforms.

7.2 Generic Damage Mechanism Investigations Investigations to gain qualitative and quantitative understanding of damage mechanisms threatening reliability are fundamentally different from accelerated reliability tests. While both types of testing requires damage accelerations, their different objectives impose different requirements on the level of control on parametric variations, sample size, test arrangements, measurement techniques, necessary time and resources.

For example, while for reliability testing the definition of failure should properly be related to the functional failure of the product, i.e, electrical discontinuity in a solder joint, the failure definition for generic investigations can take forms such as a decrease in strength, an increase in electrical resistance, an increase in thermal resistance, or a damage in characteristic frequency.

Generic investigations of this type are necessary because they lead to the required understanding that is necessary for the development of reliability models, as well as the most effective working conditions.

7.3 Thermal Cycling The damage mechanisms invoked by thermal cycling are described in Section 3.4.1. It is important that the thermal cycling test chosen produces damage in the solder joints by the same mechanism as in the use of the product. There are three basic types of thermal cycling that can be employed: functional cycling, temperature cycling, and thermal shock. The damage mechanism for thermal shock is discussed in Section 3.4.3. These different test types are discussed in the following sections.

7.3.1 Functional Cycling Functional cycling, as the name implies, involves simulating operational conditions as closely as possible. This is done to eliminate intractable effects on the test results of the many highly temperature-dependent material properties. In this manner, the results of the accelerated test will exclude extraneous damage mechanisms and reflect the conditions product experiences in operation. The mimicking of operational conditions should include power dissipation internal to the components, component-external temperature variations, heat transfer and thermal management conditions, and mounting arrangements.

Only one or two parameters should have well-controlled deviations from the operating conditions to facilitate test accelerations and minimize uncontrolled influences. The parameter that can be varied most easily, results in practical test accelerations, and does not introduce undue concern about different material behaviors is the dwell time at the steady-state temperature extremes. Decreasing the dwell time results in significantly decreased degrees of completeness of solder stress-relaxation and, therefore, less fatigue damage per cycle. While this results in more fatigue cycles necessary to cause failure during the test than in operational use, the mean-time-to-failure in the test is significantly less because many more cycles are possible in the same time frame.

Another acceleration option is an increase in the cyclic fatigue loads by an increased mismatch between component and substrate coefficients of thermal expansion and/or using test components larger in size than the product components. Increasing the cyclic temperature swing, ΔT, is *not* a good acceleration option for solder joint; in many cases, the increase in ΔT necessary for substantial test-acceleration also causes the introduction of new damage

Table 4 Properties of Printed Board Laminates

Material	Conductivity W/M-K	CTE X, Y Dir. ppm/°C	CTE Z Dir. ppm/°C	Max. Use Temperature °C	Glass Transition Temp. °C	Tensile Strength MPa	Yield Strength MPa	Elongation %
Polymer Composites:								
Polyimide Glass	0.35	12-16	40-60	215-280	250-260	345	—	—
Epoxy Glass[a]	0.16-0.2	14-20	65	130-160	125-135	276	—	—
Modified Epoxy Glass[b]	—	14-16	—	—	140-150	—	—	—
PTFE[e] Glass, Non-Woven	0.1-0.26	20	—	230-260	—	38-52	—	—
PTFE[e] Glass, Woven	419-837	10-25	—	248	—	68-103	—	—
Epoxy Aramid	0.12	6-8	66	—	125	—	—	—
Epoxy Quartz	—	6-13	62	—	125	—	—	—
Polyimide Aramid	0.28	5-8	83	—	250	207	—	—
Polyimide Quartz	0.35	6-12	35	—	188-250	—	—	—
Epoxy-Cordierite	0.9-1.3	3.3-3.8	—	—	—	—	—	—
Modified Epoxy Aramid	—	5.5-5.6	100	—	137	—	—	—
PTFE[e]	—	7.5-9/4	88	—	19[d]	—	—	—
Polyimide	4.3-11.8	45-50	—	260-315	—	345-965	—	6.7
Metal Composites:								
Cu/Invar/Cu (20/60/20)	15-18[c]	5.3-5.5	16	—	N/A	310-414	170-270	36
Cu/Invar/Cu (12.5/75/12.5)	14[c]	4.4	—	—	N/A	380-480	240-340	—
Cu/Mo/Cu	90-174	2-6	—	—	N/A	—	—	—
Ni/Mo/Ni	129.8[c]	5.2-6	5.2-6	—	N/A	621	552	50

a. FR-4, G-10 b. Polyfunctional FR-4 c. Z-direction d. Polymorphic p e. PTFE Polytetrafluoroethylene

mechanisms and different material behavior putting the test results in question (see Section 4.0)

7.3.2 Temperature Cycling Temperature cycling involves subjecting the test vehicles alternately to high and low temperatures for predetermined dwell times. The change in temperature should be accomplished at rates of less than 20°C/min to avoid thermal shock. To produce creep/fatigue damage the suggested temperature cycles are +25 to +100°C or 0 to +100°C depending on the application of the product (see Table 1) with 15 minute dwells at the temperature extremes.

Depending on the application, ''Cold'' cycling from perhaps –40 to 0°C with dwells large enough to reach thermal equilibrium can be employed. This kind of cycling produces fatigue damage that does not involve stress relaxation and creep of the solder.

For applications where large cyclic temperature swings can occur in product, e.g., Use Category 9 – Automotive-Underhood (see Table 1), ''Large ΔT'' cycling similar in nature and number to the temperature swings expected for the product are recommended. The damage mechanisms invoked are numerous, interactive and not well understood; test results from this kind of temperature cycling cannot, at this point in time, be related to different temperature cyclic conditions.

It is important that these temperatures, and heating and cooling rates be measured on the specimen and not just inside the thermal cycling apparatus. There can be large differences in the response of a specimen and that of the apparatus used for heating and cooling. Furthermore, these differences will depend upon variables such as the total thermal loading, which is a function of the number of specimens being tested, the thermal mass of each specimen and that of the apparatus, the specimen distribution, as well as the flow rate of the air.

7.3.3 Thermal Shock Cycling For a discussion of the thermal shock mechanism see 3.4.3.

In this type of test a heating and/or cooling rate of 30°C/minute or greater is employed. The severity of the test increases as the temperature range gets larger and/or the rates of temperature change increase. The mean temperature change developed in this type of test leads to severe temperature gradients which distort the printed board and the component, and leads to the development of tensile stresses in the solder joints. In addition, shearing stresses will develop from the thermal expansion mismatch between the component and the printed board. Long hold times can allow these distortions to be relaxed by creep in the solder joint between the component and the printed board. This adds to the damage of the joint and shortens the cyclic life. Increasing the temperature range increases the thermal stresses and also decreases the life, as does an increase in the mean temperature which increases the solder creep rate.

The distinction between thermal shock and thermal cycling is not always addressed in designing reliability experiments. There is a fundamental difference between thermal shock and thermal cycling. The primary differences arise from the mechanism of loading. Thermal shock tends to result in multiaxial states of stress dominated by tensile overstresses and tensile fatigue. On the other hand, as previously discussed, thermal cycling results in shear loads and failure occurs from an interaction of shear fatigue and stress relaxation. Thermal shock is performed in dual chamber test equipment, whereas thermal cycling is performed in single chamber cycling equipment. Dual chamber arrangements can produce temperature transition rates in excess of 50°C/minute. Most single chambers generally do not produce transition rates even close to 30°C/minute which is the rate necessary to induce thermal shock. The results of these two types of testing are generally incompatible. Finally, thermal shock testing for purposes of evaluating surface mount solder joint reliability is only appropriate if thermal shock is indeed a field condition encountered by the product.

In some specifications, the definitions of thermal cycling and thermal shock are not fully differentiated; the rates of change are more closely associated with what we are calling thermal shock.

7.4 Mechanical Cycling In mechanical cycling the attempt is made to produce solder joint failures by the same damage mechanism as in temperature cycling, but at significantly higher test accelerations. Mechanical cycling is carried out at constant temperatures; higher temperatures produce larger test accelerations. Because isothermal mechanical cycling is not subject to the relatively long times required to reach, and the uncertainties associated with, thermal equilibrium, cycle frequency can be very high with dwell times at the cyclic motion extremes as short as a few seconds.

A way to accelerate the mechanical cycling test is to increase the applied loads. This is a simple matter because the loads are applied by mechanical deformation of the test vehicle substrate or external loading of the components. Care must be taken during the test to prevent changes in solder joint failure due to overstressing, high strain rate, or changing from predominant shear to tension fatigue.

Practically, the test specimen consists of a surface mount component soldered on a printed board, with the assembly modified to allow for a mechanical loading. The printed board can be pulled or bent and it is possible, with a suitable adhesive, to pull on the component. Since the temperature is kept constant, the thermal properties of the specimen are not critical.

Because this type of testing neglects all thermo-mechanical effects, this test is useful for comparisons of different solder attachment designs. However, it cannot produce information that can be used to directly produce reliability predictions for product. Mechanical cycling can be benchmarked with thermal cycling, not including thermal shock, to allow some estimate of product performance. The neglect of all thermo-mechanical effects, which do play important roles in solder fatigue, as well as the high acceleration factors reduce this type of test to a ‘‘quick and dirty’’ compromise necessitated by the realities of limited time and resources.

7.5 Vibration

7.5.1 Vibration Environment

7.5.1.1 Random Vibration The majority of vibration experienced by electronics has been determined by analysis to be broadband in spectral content. That is, all frequencies are present at all times in various combinations of intensity. Controlled experiments have demonstrated that random vibration effectively simulates broadband in a test situation.

Random vibration spectra are defined in terms of acceleration spectral density (also referred to as power spectral density, or PSD) profiles, which relate energy density levels to specific frequency bands. The vibration is defined over a relevant frequency range.

The use of g-rms values alone to describe vibration tests is not valid, since a g-rms value does not characterize a specific vibration profile. An infinite combination of frequency bandwidths and spectral shapes can satisfy one g-rms value. Therefore, vibration measurements and test spectra should always relate energy content to specific frequency bands.

7.5.1.2 Source Dwells In some cases, the vibration environment is characterized by periodic excitation from reciprocating or rotating structures and mechanisms. This excitation may be transmitted through fluids (air or liquid) or structures. When this form of excitation predominates in a critical frequency band, source dwell vibration is appropriate. A source dwell excitation is characterized by broadband random, narrowband random, or one or more sine waves.

This technique differs from the traditional sinusoidal resonance dwell test. A resonance dwell emphasizes those frequencies at which the test item resonates. A source dwell emphasizes those frequencies which predominate in the platform environment. Obviously, the source dwell spectrum provides a more realistic test.

7.5.1.3 Sinusoidal Vibration The service vibration environment in some propeller aircraft and helicopters contains excitation which is basically sinusoidal in nature. The excitation derives from engine rotational speeds, propeller, and

turbine blade passage frequencies, rotor blade passage and velocity, and their harmonics. Environments such as this may be best simulated by a sinusoidal test. Caution must be exercised to assure that the frequency range of the sinusoidal exposure is representative of the platform environment.

7.5.1.4 Mechanical Impedance Effects Allowance should be made for mechanical impedance effects whenever the benefits of increased realism are worth the time, effort, and cost required for implementation.

Equipment structures dynamically influence their own response to an external forcing function. At structural natural frequencies where the response stresses are high, the structure will load the adjacent supporting structures (i.e., notch the acceleration spectral density at these frequencies). The magnitude of loading effects is related to the relative impedance of the equipment structure and support structures. As a rule of thumb, the resonant element exhibits a loading force in proportion to its dynamic weight multiplied by the corresponding amplification factor.

Mechanical impedance effects can be accounted for in establishing vibration test spectra. The depths of notches are determined by measurement or by calculation.

7.5.2 Vibration Acceleration Vibration testing is recommended to be performed only with careful fixturing or on complete systems in order to include accurate natural frequency responses and use conditions.

There are three different types of vibration tests, each having a different purpose.

1. The vibration functional test is to verify that the equipment functions at the maximum expected service vibration level. The duration of the functional test is typically only long enough to verify equipment function or a total of one hour per axis, whichever is greater.

2. The endurance test is conducted to demonstrate that the equipment has a structural and functional life compatible with contract requirements. Endurance test levels and durations are established by raising functional levels and extending the test duration to generate an equivalent lifetime fatigue damage. This results in vibration test levels higher than maximum expected service levels, in some cases much higher. The endurance test does not necessarily establish fatigue life since the equipment is not tested to destruct. The endurance test is only conducted for a prescribed period of time. Statistically the sample size is also too small to adequately determine fatigue life.

3. In accelerated life testing the equipment is tested to failure by raising functional levels as in endurance testing, but the test is continued until failure. Multiple test vehicles must be used to gain a statistical confidence in the accelerated fatigue life.

A simplified fatigue relationship is often used to scale vibration levels, test durations, and derive acceleration transforms when the loading is random vibration. The equation relates two test conditions, 1 and 2,

$$\left[\frac{PSD_1}{PSD_2}\right]^M = \frac{t_2}{t_1} \qquad (19)$$

where

PSD = acceleration power spectral density (G^2/Hz)
t = time (consistent units of seconds, minutes, or hours)
M = material constant

and represents a linear log-log relationship between PSD and time, where the negative slope is 1/M when time is plotted on the horizontal axis. Equation (19) can be related back to Basquin's high cycle fatigue relationship or the commonly recognized S/N curve, linear log-log relationship between stress and cycles to failure. Care must be exercised when comparing the two relationships since the slopes of the two curves vary by a factor of two. For equation (19), a starting value of M for solder attachments is 3 to 4.

Small variations in the exponent value M used in equation (19) can make dramatic variations in the predicted life of an assembly when the equations are used to scale from one condition to another. A potential for extrapolation error is particularly true when the lives of the two conditions vary by more than a decade.

The simplified fatigue relationship in equation (19) is also questionable under high vibration levels due to structural nonlinearities. During accelerated testing, use as long of a test duration as practical to keep vibration levels low. More sophisticated analysis techniques can be used when warranted.

7.6 Creep Rupture Tests Creep rupture tests are generally performed under constant load conditions. A load is applied to the specimen and the time dependent strains are measured with an LDVT or extensometer. A typical creep rupture test is shown in Figure 9.

Generally, metals will show three distinct regions in a creep test. Region I is primary creep. This region tends to be very small in solder alloys. Region II is steady-state creep in which the strain rate is relatively constant. The steady state region is of particular interest in the analysis of creep-fatigue interaction since steady state creep occurs during hold times.

Region III is tertiary creep in which cracking in the grain boundary occurs rapidly until failure. The test specimens are very important. Microstructure has a primary effect on creep behavior of solders. The test joint dimensions (thickness) must be representative of joints in service. Plug and

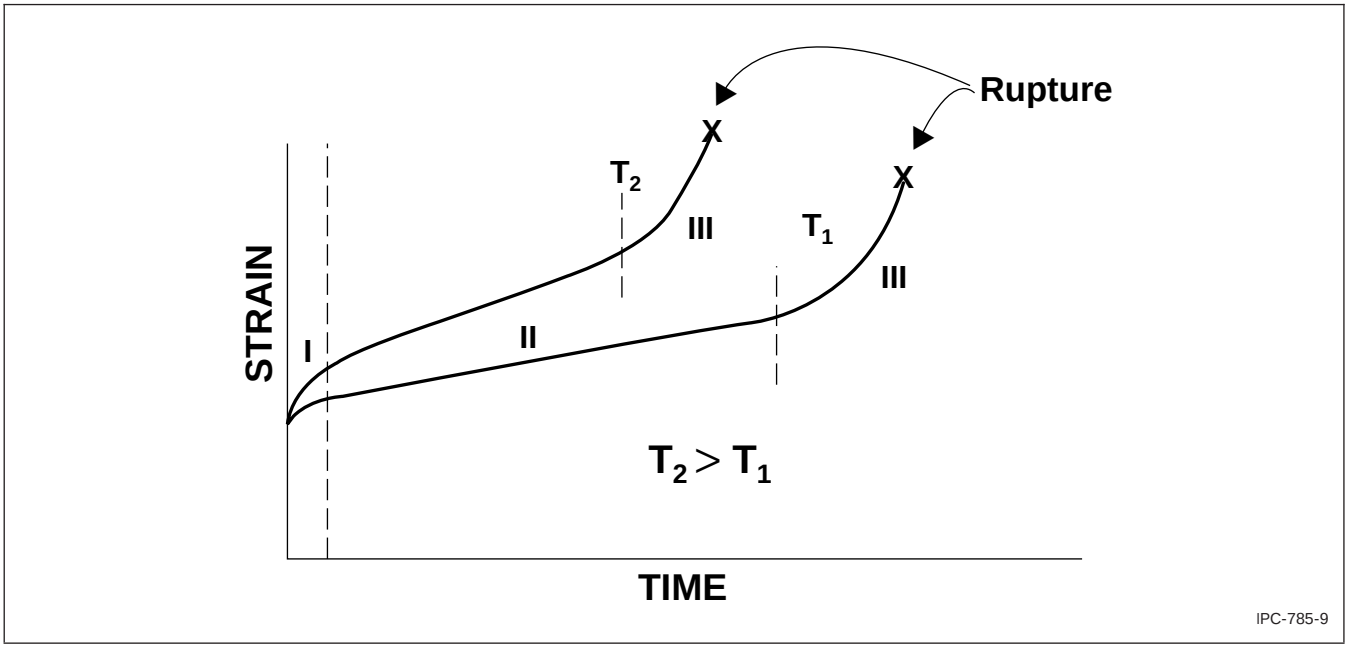

Figure 9 Creep behavior of solder

ring joints or lap joints provide the best configurations for creep testing of solder alloys.

7.7 Mechanical Shock Testing Mechanical shock tests are high acceleration tests that simulate severe use conditions or even accidental misuse. These conditions include suddenly applied loads or abrupt changes in motion caused by rough handling, transportation, or field operation. Shocks in this category may disturb operating characteristics or cause damage similar to that resulting from excessive vibration.

In a mechanical shock test, very rapid and sharp cycling is arranged. Typically, the shock pulses are 500 to 30,000g with a pulse duration between 0.1 and 1.0 milliseconds. This rapid mechanical cycling enables tests to be run with very small applied loads or displacement ranges.

Mechanical shock is characterized by peak amplitude, duration, and time rate of change and is generally applied to a system in the form of a pulse, impulse or step. The system response to the shock is dependent upon the nature of the shock, the architecture and materials of the system, the orientation of the system with respect to the shock and the natural frequency or frequencies of the system. Where the duration of the pulse or step is short, the system can vibrate at its own natural frequency or frequencies; the amplitude of that free vibration will decrease with time depending upon the damping available in the system to dissipate the mechanical energy as heat.

Mechanical shock tests are intended to quantify the performance of the product or component under controlled laboratory rather than actual field conditions because:

1. The shock waveform can be controlled and reproduced for comparison purposes and can be varied over a range which is representative of a wide distribution of field conditions.
2. The laboratory environment permits the realtime recording and analysis of the shock and responses, possible improvement of the assembly, and rapid reassessment of the new construction.
3. Many laboratory tests can be performed for the same cost and time required to run several field tests.

The shock waveform of mechanical shock machines can be affected by the mass and mass distribution of the SM printed board assembly particularly if the mass of the test specimen is significant compared to that of the machine; the shock machine should be as rigid as possible with its natural frequencies well above those expected in the test specimen.

The shock waveform can be specified as that expected to be applied to the test specimen or as that expected when a specific shock machine is employed.

Shock machines range from simple drop table and inclined planes testers to high acceleration gas and air gun testers.

7.8 Failure Criteria for Solder Joint Fatigue Tests The definition of failure of a solder joint and its subsequent detection are not as straight-forward as might be expected (see Section 4.3.1). Frequently, comparison of test results has been made difficult, if not impossible, by failure criteria which cannot be related to each other. These criteria have included visual inspection for cracks in the solder joints at periodic intervals, destruction of solder joints at periodic intervals searching for decrease in the original

strength, monitoring the stress-strain hysteresis loops of individual solder joints and defining failure in terms of some hysteresis loop characteristic, monitoring electrical resistance for some amount of increase in original resistance, and monitoring for electrical resistance with the capability of detecting even short electrical discontinuities.

Failure criteria that require the periodic interruption of the test may significantly prolong the time required for the test, may disturb the experiment, and influence the results. Choosing arbitrary failure definitions can serve as damage indicators if they are carried out consistently. However, given the many different failure definitions and measurement techniques used do not make comparison easy.

For the purpose of accelerated reliability testing, the following failure criteria are recommended. Failure is defined as the first interruption of electrical continuity that is confirmed by 9 additional interruptions within an additional 10% of the cyclic life.

Failure detection shall be by continuous monitoring of daisy-chain continuity test loops such that:

1. At least one continuity interruption of 1 microsecond or less duration can be recorded for each test loop during any polling interval of 2 seconds or less;
2. At least 10 such interruptions can be recorded per test loop to confirm the first failure indication;
3. The monitoring current does not exceed 2mA at no more than 10V and that an electrical discontinuity is indicated by a loop resistance of 1000 ohms or more. False failure indications due to electrical noise can be a problem, particularly for loop resistance thresholds lower than 1000 Ω.

These guidelines reflect the limitation of available continuity monitoring devices, as well as the observed behavior of daisy-chain test loops with fractured solder joints. It needs to be pointed out that multiplexed monitoring, no matter how fast, is *not* continuous monitoring and will lead to failure detection significantly later than when solder joint fracture occurs.

7.9 Accelerated Life Test Planning Determining the methodology for an accelerated life test is similar to any design of experiment concept used in industry to evaluate a process of a product. In reliability performance it is important to establish the correlative parameters of the accelerated stress exposure to the end-use environment.

In the design of an accelerated life test experiment it is important to test one or more independent variables and compare those to a dependent variable. In solder joint reliability testing the single dependent variable is the number of cycles to which an equipment is subjected. Cycles mimic the electronic equipment operation, and are related to the conditions of the end-use environment. The independent variables can then be equated to:

- Temperature Swings, e.g., +25 to +60°C
- Component Size
- Coefficients of Thermal Expansion
- Solder Joint Height
- Lead Stiffness
- Failure Probability

7.9.1 Test Variables A design of experiment should define all the appropriate parameters that are part of the experiment. This includes identification of the response variables being studied.

The test objective should be defined by detailing the test question, null hypotheses, optimization, etc. There should be no doubt what the purpose of the test is or why the experiment was conducted.

Independent variables need to be characterized and identified in great detail with specific emphasis placed on the relationship of the variables to the dependent variable being studied. The independent variables fall into four categories. These are:

- Design Parameters
- Process Parameters
- End Product Parameters
- End-Use Environmental Parameters
- It is important to define the rational for selection and why each independent variable is included in the plan.

7.9.2 Test Plan The test plan should indicate the level(s) or range of values at which the independent variables are evaluated.

These levels(s) are the test setting and the reason for setting the ranges needs to be defined.

The test plan should describe the experimental design (full factorial, fractional factorial, etc.) used for the study and the method in which the experiment is performed (randomized, stratified, production equipment, laboratory, etc). The measurement method is identified in this plan. This is usually the physical method used for measuring the dependent variable (e.g., solder joint fracture giving the fatigue lives.)

An example of a test plan is the IPC Round Robin Program ''Evaluation of Surface Mount Land Patterns,'' defined in IPC-SM-782,'' August 1988.

7.9.3 Sampling Methodology The sample size and frequency is identified in the plan. Included are the number of observations on the dependent variable and the time interval between samples at a single test condition. The reason why the sample size and frequency were selected is defined.

Due to typical failure distributions associated with fatigue testing, a minimum of 32 data points has been found to be

required, per test condition, to allow for test results (e.g., mean cycles to failure) to be calculated with reasonable statistical certainty.

Some care should be taken in the use of the term ''data point.'' If testing is concerned with the relative merits of one land pattern design vs. another, then 32 parts using each of the two test land pattern designs would be required and individually monitored to allow for reasonable differentiation. It should be reasonable and in fact desirable, that these test land concepts coexist on the same substrate(s) to rule out any other random effects.

If on the other hand, another macro variable was being considered, say, printed board construction or reflow process parameter, then each data point would consist of an entire assembly run separately through the process. In this instance, it may be more cost effective to fabricate a large number of small, simple assemblies.

7.9.4 Test Vehicles The test vehicles (TV) must be designed to accommodate continuous electrical monitoring, during the complete thermal cycle. (See Figure 10)

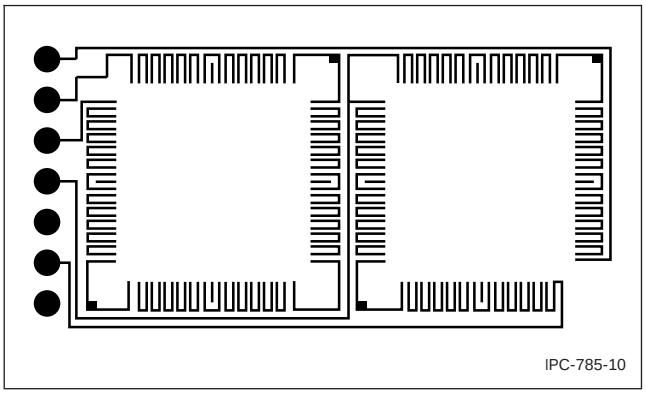

Figure 10 Example of circuit layout

All components will be specially prepared to have leads internally interconnected so that in conjunction with the TV substrate pattern complete test loop daisy-chains are formed. It is preferred that these lead connections be accomplished internal to the packages wherever possible. However, for some components (e.g., chips, MELFs) these lead connections are only possible external to the package. It is imperative that these internal or external lead connections do not become a source of continuity disruptions and thus falsely indicate surface mount attachment failures.

The lead connection scheme depends on the number of I/Os of the component and is as follows:

2 I/O:
Connect the two terminals.

3 I/O:
Connect all three terminals together (as shown in Figure 11).

4 or more I/Os:
Connect only leads on the same component side. Starting at the corners, alternate lead pairs should be connected internally working towards the center of the respective component side. For component sides that have an odd number of leads, the center lead is not connected into the test loop and is skipped in the connection scheme (See Figure 11).

Test vehicles should represent the product to be evaluated in as great a detail as possible within the confines of the variables being considered. For example, in the consideration of solder joint design, testers often opt for deleting the constraining core (and thus increasing the CTE) as a means of accelerating failure. This technique is valid, but care must be taken that in deleting the core other variables besides the CTE are kept as close to the product as possible. Measurement of the CTE values is absolutely necessary.

7.9.5 Sample Conditioning Test vehicles should be assembled and processed as similarly as possible to actual product. Product-similar test vehicles should reflect product solder joint characteristics such as grain structure, composition, and intermetallic compound layers and their thickness. Solder grain structure is inherently unstable; it will coarsen with time and temperature, particularly in the presence of cyclic strains. In product, significant coarsening of the solder grain structure has been observed within one year of storage.

Fine grain structures in the solder joints will result in longer fatigue lives in accelerated testing, which does not allow the time for these time dependent processes to occur to the same degree as they would in product use over many years. The changes in the structure of solder, which undergoes and accumulates fatigue damage, appear to follow the sequence of grain structure coarsening, micro-voiding/cavitation-formation at grain boundaries, micro-cracking with 50 to 70 percent of life remaining, coalescence of micro-cracks, and fracture. Therefore, it stands to reason that accelerated test vehicles should start with a solder grain structure that is more representative of the grain structure in product after some period of operation. This becomes particularly important for more highly accelerated tests.

After assembly, the test vehicles should be subjected to an accelerated thermal aging (e.g., 300 hours at 100°C for FR-4, 100 hours at 125°C for polyimide) in air to simulate a reasonable use period and to accelerate such possible processes as solder grain growth, intermetallic compound growth, and oxidation. Storing the test vehicles after this artificial aging for some additional time at room temperature before commencing with the fatigue testing serves to further stabilize the solder structure.

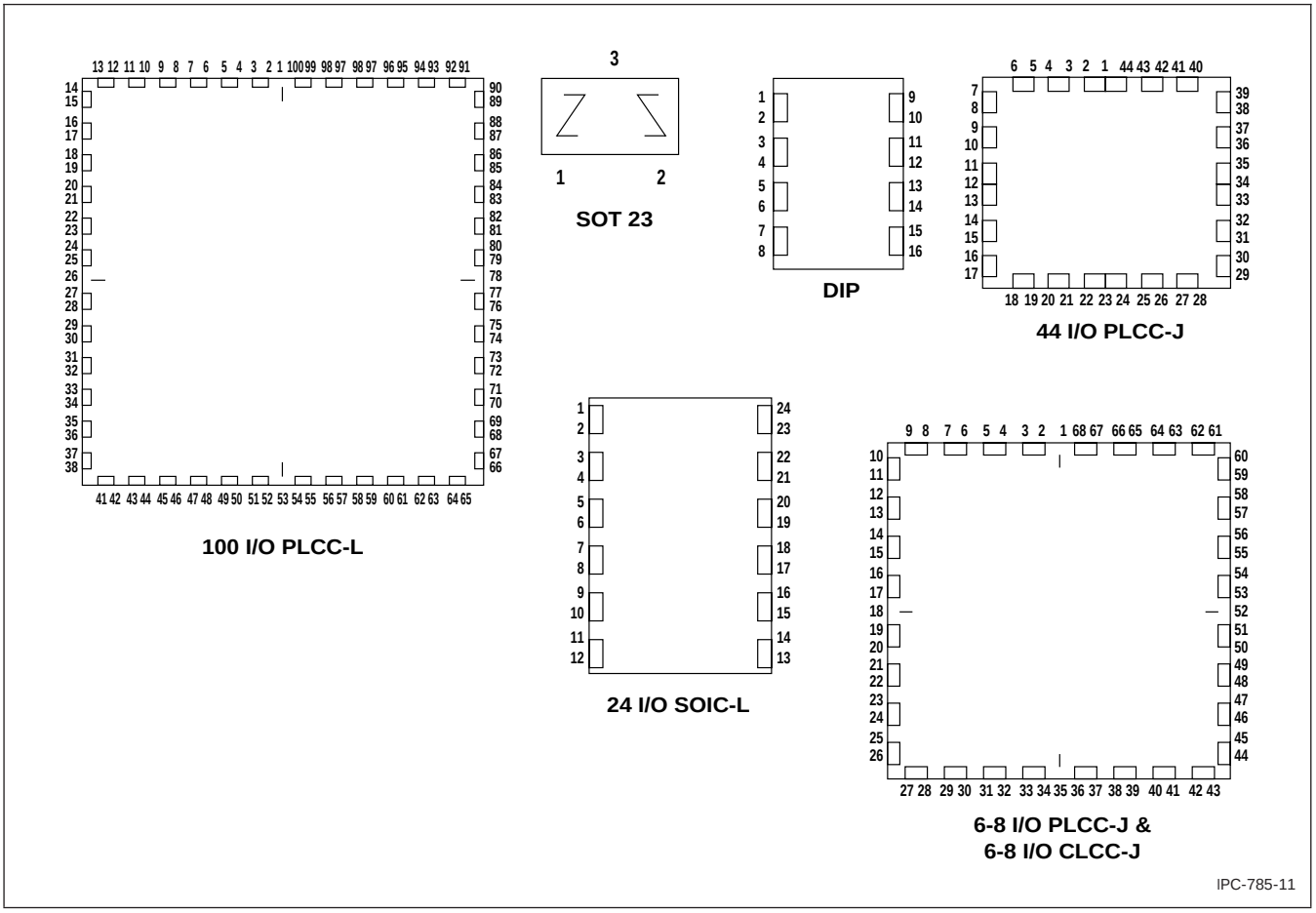

Figure 11 Internal lead connection schemes for odd lead numbers per side

7.9.6 Temperature Cycle Selection and Monitoring The cyclic temperature profiles are a very important part of the test conditions. They should be measured on different parts of the test vehicles and the thermal load, as well as for the chamber environment itself. This is necessary because 1) cyclic temperature profiles can vary significantly for different parts (component versus printed board, center versus edge of thermal load, etc.), and 2) chamber environment can be significantly different for different locations within a chamber.

Temperature extremes in thermal cycling may be increased over those seen in the field, but only where no major change of material properties is seen as a result of the increase. Appropriate temperature regimes are suggested in Table 1. Examples of poorly selected extremes are:

a) The low temperature selected is greatly below that seen in the field, and as a result, the solder has substantially different material properties than it would have in the use environment (for example, little, if any, creep/stress relaxation).

b) The high temperature selected comes close to the T_g of the laminate material being tested.

Selection of sufficient dwell times is essential to allow for significant stress relaxation in the joint before beginning the next thermal transition.

Because thermal shock tests involve different damage mechanisms than creep/fatigue, ramp rates should be measured at the printed board assembly surface during testing and should not exceed 20°C/minute for thermal cycling.

7.9.7 Sample Fixturing and Placement Within the Chamber Attention should be given to the fixturing of the samples under test, as the effect of position and orientation within the chamber can often have major impacts on the ramp rates and temperatures seen by a given printed board assembly during test. It is recommended that a number of printed board assemblies be measured during test set up to ensure uniform temperature and air flow in the chamber during the test. As a further safeguard, samples undergoing testing should not be grouped by test condition but rather should be randomly arranged to prevent contamination of the data by an uncontrolled or unanticipated chamber variability.

Finally, care should be taken to see that the printed board assembly is tested within the environment in which it will see service. If a truly representative test is needed, this may

require that a chassis representing the actual use environment be used within the chamber as this can greatly affect the ramp rates and dwell times seen by the printed board assembly under test.

Connectors within the test chamber should be avoided since during thermal cycling the connector connections can give false failure indications. If connectors cannot be avoided within the test environment, the connectors need to have high-quality, gold-plated connections not subject to significant movement during thermal cycling.

7.9.8 Data Analysis The test results need to be analyzed and evaluated using statistical considerations to determine failure distributions, variable independence or interaction, anomalies, etc. Further, the data needs to be analyzed using the information in Section 4, to verify corroboration with original predictions, determination of differences in the ''non-ideal'' factor, F, correlation of the effects of the different independent variables, etc.

Anomalies and deviations need to be examined as to their possible causes to separate and identify the affects of test variations from those caused by test vehicle differences.

7.10 Failure Mode Analysis Failure mode analysis (FMA) can give valuable information as to the underlying cause(s) of failure. This is equally true for product failures and for evaluating the results of accelerated reliability testing. For accelerated reliability testing FMA is especially valuable to determine the cause(s) of unexpected results and anomalies. FMA starts with visual analysis with increasing magnifications, progresses to metallographic examination, and, if necessary, to analytical techniques or SEM, EDX and Auger.

The metallographic study of solder joints and the elucidation of the cause(s) of failure are complicated. Coarse grains and colonies may arise from very long exposure at relatively low temperatures or from short exposures at higher temperatures under cyclic stress. Intermetallic compound (IMC) layers may be formed during the initial soldering process, during rework to neighboring components, or during long service under relatively mild temperatures. The physical analyst is expected to comment on the location and quantity of intermetallics, the nature and relative dimensions of the grains, the possible sequence of events that led to the joint failure and methods of avoiding such failure in the future. Selective etching of the failed surface can develop structures characteristic of rapid grain growth in molten solder or slow grain growth by diffusion in the solid state. SEM/EDX (Energy Dispersive X-Ray) or Auger Scanning Electron Microscopy techniques can augment optical microscopy by providing quantitation of the relative abundances of tin, lead, copper and other constituents of the solder joint; this data can identify those metals and their source(s) which can lead to loss of ductility.

The fracture surface appearance provides additional information on the fatigue mechanism. A transgranular fracture surface is characteristic of over-stress fatigue. Over-stress dominated fatigue occurs when the solder joint has been exposed to high stress levels, typically due to very high strain-rate loading. An intergranular fracture surface is more characteristic of creep-fatigue failure. Creep-fatigue failure occurs at low stress levels. See Volume 12 of the Metals Handbook for examples of these fracture surfaces.

SEM/EDX is discussed in ''Solder Joint Reliability,'' Chapter 6. See Volume 9 of the Metals Handbook, 9th Edition, for a discussion of metallography; Volumes 10 and 12 in the same series discuss materials characterization and fractography.

7.10.1 Optical Microscopy Interpretation of the cut/polished or etched solder joint specimen requires:

a. accumulated experience on the part of the analyst or,

b. access to, and comparison with, representative photomicrographs of solder and solder joint specimens resulting from known applied stress and carefully described, reproducible specimen preparation technique.

Photomicrographs of these kinds of specimens are available from the International Tin Research Institute (ITRI) or Tin-Information Center publications #580 and #703. Other photomicrographs are available in ''Solder Joint Reliability,'' Chapter 6 and 7.

7.10.2 Metallographic Preparation Preparing tin-lead solder joints for metallographic evaluation requires extra care. The samples are composed of high hardness (Copper-Tin) intermetallic compound particles dispersed in a very soft (Lead, Lead-Tin) matrix. This heterogeneous mass is coated on a hard basis material of copper or iron alloy. The lead-tin matrix can recrystallize at temperatures achieved during the curing of some epoxy mounting materials or hardening of some thermoplastic mounting materials; polyester or acrylic mounting materials with as LOW a temperature rise during cure or setup as possible are recommended. Great care is required in revealing the undeformed, undamaged structure under the superficial layer.

General comments on metallographic sample preparation, mounting, and polishing can be found in IPC-TM-650, 2.1.10 and 2.1.1.2, in IPC-MS-810, ''Guidelines for High Volume Microsection,'' and in Leco Corporation's ''Metallography Principles and Procedures'' which also contains reprints of ASTM E407-70 and ASTM E340-68. In addition, pages 5–12 in the ITRI publication 580 are instructive in dealing with tin-lead solder joint destructive physical analysis (DPA).

7.10.2.1 Cutting The initial step for metallographic preparation is the isolation of the component or solder joint

for mounting. This entails the use of a jeweler's saw, router abrasive saw, or similar cutting device to remove the specimen. Several factors should be considered during this initial step:

1. *Cut Location:* Care must be taken to remove the specimen without cutting too close to the solder joint of interest. The cut should, however, be close enough that excessive grinding is not required. If in doubt, leave a little extra material. Usually 1/10 inch of material around the area of interest is sufficient.
2. *Fixturing:* Care must be taken to ensure that damage is not done to the specimen while holding it for cutting.
3. *Cutting Speed:* A smooth, consistent feed rate and pressure should be maintained to avoid damaging the specimen. Vibration of the specimen during cutting must be avoided.
4. *Cutting Fluids:* Oil, water, or other types of coolant should be used with abrasive blades, especially diamond blades. The cutting fluid serves two main purposes:
    1. Removal of the cutting debris, allowing for efficient material removal.
    2. Removal of heat generated during cutting. When a situation requires dry cutting, extreme care must be taken to avoid generating heat which may affect the specimen, particularly solder joints or polymeric materials.

    A coolant should be chosen which can be cleaned off of the specimen easily and completely, so that the encapsulating epoxy can bond to the sample surface.
5. *Ceramic Precautions:* Due to their hardness, aluminum oxide ceramic specimens require the use of diamond bonded cutting equipment during both cutting and grinding. Also, beryllium and beryllium oxide materials produce toxic dust and must never be cut dry.

7.10.2.2 Mounting The specimen should be encapsulated in some rigid medium for grinding and polishing, so as to achieve a flat, uniform surface and to protect the solder joint. Caution must be used to ensure that the mounting procedure does not change the solder joint microstructure. Overplating with copper or nickel can help to protect highly deformable materials. Two mounting methods are:

1. *Quick Mounting:* This method utilizes a thermoplastic material such as polymethylmethacrylate, and typically is not entirely transparent. Filling of small cavities and adhesion to the sample may be inferior to the results of slow mounting. However, one mount can usually be prepared in approximately 5–15 minutes. The heat generated by quick mount systems varies widely from product to product.
2. *Slow Mounting:* This method typically utilizes epoxides as the mounting media. Vacuum impregnation techniques can be used to remove air bubbles and improve flow of the encapsulant into confined spaces. Some encapsulants must be cured at temperatures ranging from 60 to 90°C, while others are room temperature curing, but can generate even higher temperatures by exothermic reactions. Experimentation with empty molds will reveal whether this is a problem. Curing in a water bath helps to remove excess heat. Mounting times can vary from 1 to 8 hours depending upon the product and the curing conditions.

7.10.2.3 Preparation for Mounting When mounting a specimen, it is important that it be oriented properly. Proper orientation depends upon your grinding and polishing equipment and technique. Practice will determine what works, and what does not. Here are two basic mounting methods:

1. *Vertical Mounting:* The sample is held vertical relative to the bottom of the mold either by gluing it to the mold floor or by using special clips. The encapsulant can then be poured into the mold until it is full.
2. *Half-Mounts:* The sample is placed horizontally into a mold which is half full of previously cured encapsulant. The mold is then filled with encapsulant and allowed to cure. The sample is then ground from the side, and may not fit into some automatic machines. If this is a problem, then vertical mounting should be used.

Note: The grinding and polishing sections of this procedure were written from the point of view of manually grinding and polishing the sample. Most of the concepts are applicable, however, to automatic processing. Attempts have been made to reconcile the differences between the two procedures.

7.10.2.4 Grinding The third step of sample preparation involves removing material from the specimen to expose the areas of interest. Grinding is an abrasive process to slowly remove deformed surface material and reveal underlying, nondeformed regions. Grinding is typically done using silicon carbide papers, progressing from 120 to 1000 grit depending on the amount of material removal required. Several factors should be considered during this step:

1. *Pressure:* Sample hardness dictates, to some extent, the amount of pressure required. Pressure should be kept light to avoid excess deformation of the specimen surface.
2. *Time:* The grinding time for each piece of grinding paper should be kept short. Excessive grinding time can cause faceting as the grinding paper wears down and the particles get dull. Faceting is usually corrected by switching to a new, sharp piece of grinding paper.
3. *Cutting Fluid:* As with the cutting operation, fluid is used to remove debris and prevent the specimen from overheating. Water is the most common cutting fluid.

4. *Ceramic Materials:* Due to the hardness of ceramics, components, packages and substrates made of ceramics such as aluminum oxide (alumina) or beryllium oxide (beryllia) require the use of diamond bonded cutting wheels and grinding disks. Mechanical processes such as grinding and polishing of beryllia pieces create a dust defined as a hazardous material; this dust must be suppressed by sufficient coolant and cutting fluid. OSHA and EPA handling requirements will supersede any technical handling or use requirements. The beryllia dust mixed with the fluid is defined as a hazardous material; this aspect must be considered during disposal.

5. *Viewing Window:* Often during precision grinding it is helpful to look clearly at the sample from above. This can be accomplished by grinding and polishing a flat area on the surface of the epoxy perpendicular to the sectioning plane. Some automatic equipment does not allow mounting of these irregularly shaped samples, however.

6. The hard intermetallic compounds such as Cu_6Sn_5, Cu_3Sn, Ni_3Sn_2, Ni_3Sn_7, AuSn, $AuSn_2$, $AuSn_4$, FeSn, $FeSn_2$, and Ag_3Sn can cause grooves and channels in the soft lead or lead-tin matrix when the particles break free and roll downstream. Manually or automatically moving or rotating the sample counter to the wheel rotation will minimize grooves and channels.

7.10.2.5 Polishing The next stage of metallographic preparation following the grinding step is polishing the sectioning plane. Polishing is a less severe continuation of the specimen surface abrasion. Polishing media can include diamond, aluminum oxide, silicon oxide, or chromium oxide. Polishing media particle size progresses from about 9 µm to as fine as 0.05 µm to produce a uniform, scratch-free surface. This is usually divided into coarse (9 to 1 µm) and fine (1 to 0.05 µm) polishing. Again several factors should be considered during this step:

1. *Cleanliness:* WASH THE SAMPLE FREQUENTLY. It is extremely important that the sample and anything that comes near it (including hands and work benches) be as clean as possible at all times during polishing. The sample should be washed and rinsed with warm soapy water before beginning to polish the sample and after each step. Brief ultrasonic cleaning is the most effective way to clean out small cavities such as cracks or voids.

2. *Polishing Cloth Selection:* The primary difference between grinding and polishing is that while grinding grit is fixed in place, polishing uses freely flowing particles in a slurry. This slurry is held on a cloth which determines the extent of the surface relief and the polish quality. Lower nap cloths will produce a flatter surface than high nap cloths, but may not remove all scratches as effectively. Special low nap fine polishing cloths can produce a very flat, nearly scratch-free surface.

3. *Polish Extenders:* Extenders play an analogous role in polishing to that of the cutting fluid in grinding, removing debris and minimizing heat generation. An extender also ensures proper dispersion of the polishing media.

   Care must be taken to use the proper amount of extender. Too much extender will allow the sample to float, causing excessive relief. Too little extender may allow the encapsulant to soften and absorb polishing media, especially diamond particles. The extender used is a function of the polishing medium, and is usually either deionized water or a special polishing oil.

4. *Pressure:* Polishing pressure should be very light. Excessive pressure causes excessive surface relief.

5. *Direction:* Coarse polishing can be done either of two ways. Trial and error will indicate which is best for you, and results may vary for different types of samples.

Omni-directional polishing involves rotating the sample around the polishing wheel either counter to, or with the wheel rotation. In this way the polishing is performed in all directions. Uni-directional polishing is where the sample is held stationary, and the polishing scratches are all aligned in one direction. This is particularly useful on layered structures. Fine polishing is almost always performed omni-directionally. Most automatic machines function only in the omni-directional mode.

7.10.2.6 Etching Etching is the final step in metallographic sample preparation. The specimen should be examined before the etching step is performed for defects, inclusions, porosity, cracks, intergranular corrosion, intermetallic compound development, and other anomalies. Etching removes a thin layer of abraded surface deformation, revealing the microstructural details of the specimen. Etching requires the use of an acid or a base to chemically attack the sample surface. Many enchants are available for etching a variety of materials. The disposal of the wastes generated may be a problem due to the presence of heavy metals such as the chromates and of toxics such as beryllia dust.

See ASTM E407-70 for safety cautions. The chemicals used should be USP or NF or better. See ITRI publication 580 for enchants specific to tin and its alloys and for photomicrographs of the resulting sample surfaces.

Lead-Tin phases:
Nital (1–5 ml HNO_3 100 ml ethanol (95%) or methanol (95%) Immerse 5–40 seconds in 5% HNO_3 solution. To remove stain, immerse 25 seconds in 10% HCl-Methanol solution.

A variety of etches for

Copper-Tin IMC:
95 ml H_20
10 ml 10% Chromic Acid
2 ml HCl
5 ml H_2SO_4

or

7 grams $FeCl_3$
75 ml HCl
200 ml H_20

or

100 ml H_20
100 ml H_20_2, 3%

or

100 ml NH_4OH, 35%
100 ml H_20_2, 3%

Solder:
Solder can be chemically etched using a dilute (5% maximum) hydrochloric acid solution, but acceptable results can usually be obtained by extensive final polishing using extremely light pressure. Solder is extremely reactive to most etches, and care must be taken not to destroy its structure.

Copper:
50 ml Ammonium Hydroxide
50 ml Water
3 to 5 gm Ammonium Persulfate

Stainless Steel or Kovar:
10 gm Copper Sulfate
50 ml Hydrochloric Acid
50 ml Water

7.11 Reporting Results The following construction, design, process, and supplemental testing data should be included as part of all test reports:

a) Purpose of the test and brief description of test objective(s), sample identification scheme and statistical data analysis.

b) Details of the construction and design of the test vehicle with deviations from product design identified and defended (based on availability, cost, or test acceleration). Specifics include board/module raw material composition and thicknesses, including prepreg and layup, metals, ceramic, etc.

Board/module design features including: manufacturer, pad patterns, PTH drill diameters, and minimum wall thickness, inner and outer copper layer thicknesses, board cross-section including % copper and locations of signal and ground/power planes, core composition (if present), and composite design CTE, including material CTEs utilized.

Component package features including: manufacturer and part number, raw part preparation (including pretinning procedure if utilized), and internal part description (daisy chain or die configuration).

Assembly processes and features including: solder type and application method; component placement method; bakeout and other pre-processing; reflow method; cleaning process; and conformal coat type, application method and thickness (if used).

Supplemental measured data (including pictorials if applicable) should include: solder joint height (for leadless packages, if not controlled by design); solder joint fillet form; board top and bottom X and Y CTE data, both before and after thermal cycle testing; package CTE data.

c) Sample preparation/pretreatment details (if used).

d) Temperature profiles of the specimen under test, as measured on the specimen, and chamber test records showing chamber functionality.

e) Analysis of electrical failure data including statistical plots, confidence bands, and treatment of outliers. These are discussed in the books, ''Accelerated Testing: Statistical Models, Test Plans, and Data Analysis'' and the earlier ''Applied Life Data Analysis.'' Other good references include ''Accelerated Testing Handbook,'' ''Applied Reliability,'' ''How to Plan and Analyze Accelerated Tests,'' and ''How to Analyze Reliability Data.''

1) Method of electrical test used including method of application of test current (continuous or sampled), test current level, clamping voltage on current supply, response time of voltage or resistance measurement instrument, definition of ''open'' and response time of ''opens'' detector.

2) Plotting of the data is recommended to check for ''goodness'' of the data by eye; use paper with a Weibull scale for probability and a log scale for data (time), which is available from various suppliers or copyable from a book. This graphical analysis tool provides a qualitative check on the data and a quick, rough quantification of various parameters. There are different graphical treatments for data with an observed or exact time of failure (complete) and for data where only the number of failures during an inspection period is available; see ''How to Plan and Analyze Accelerated Tests.'' Analytical methods provide an indication of the uncertainties in the data by means of standard error estimates and confidence intervals.

3) Confidence intervals and limits are treated in ''How to Plan and Analyze Accelerated Tests'' and in chapter 5 of ''Accelerated Testing.''

4) Analysis and discussion of specialized treatment of any ''outliers'' (failures which occur much earlier than the balance of the data at the same stress) encountered in this dataset.

5) Discussion of CENSORED data where some of the test items do NOT provide the critical data which is the time or number of cycles to failure; the data or tests are censored on the right or truncated when the items are taken from test or service prior to failure or in connection with some other failure mode or the items have not yet failed at the time the test ended or the data was analyzed.

f) Metallurgical analysis of failed components with macro and micro-graphs attached. (*Note:* Samples undergoing fatigue failure must be handled with extreme care to avoid further damage or contamination of failed areas. DO NOT ''FIT'' FAILED SECTIONS BACK TOGETHER TO ''RECONSTRUCT'' FAILURE AS THIS WILL TOTALLY DESTROY THE FRACTURE FACE OF THE SOFT SOLDER).

g) For typical vibration recorded test data, MIL-STD-810 lists the following:

1) Prior test history of the specified test item.

2) Inspection and test procedures, including inspection requirements, test criteria, instrumentation, data requirements, and failure criteria.

3) List of all test equipment, including vibration generating and analysis equipment, mounting arrangements, and fixtures.

4) Orientation of test item, including axes of applied vibration.

5) Location of accelerometers used to control and measure vibration.

6) Resonant frequencies, including those selected for test, as applicable.

7) Isolation characteristics, including sway amplitudes and transmissibility versus frequency.

8) Applied test levels, durations, and frequency ranges.

9) Results of all performance measurements, including overall test results.

10) Analysis of each failure and corrective action proposed.

11) Analysis bandwidth.

This data should be used to support a failure mode analysis. Sections should be maintained for further analysis if required or requested.

Appendix A
Step-by-Step Example

To illustrate the utilization of the relationships in Sections 4.3 through 4.5, a numerical example is provided.

The following information is assumed:

Product:

Computer for Navy artillery—Use Category 6 in Table 1,

Design life = 10 years (N = 3650 thermal cycles),

Component-external daily temperature cycles:

ΔT = 40°C for 100 days/year and 60°C for 265 days/year,

Acceptable cumulative failure probability at end of 10 years x = 0.5%

Largest leaded component:

68 I/O 50 mil pitch ceramic chip carrier (LCCC), α_C = 6.3 ppm/°C, dissipating 0.8 W, with side-brazed copper alloy compliant leads with a diagonal lead stiffness of K_D = 52 lb/in,

Largest leadless component:

CC1820 chip capacitor, α_C = 6.8 ppm/°C,

Substrate:

Low CTE multilayer board, α_S = 10.5 ppm/°C,

Conformal coating: Low CTE epoxy-type (not considered in this reliability analysis).

Test Vehicles:

Components:

8 chip carriers (LCCC), 68 I/O 50 mil, α_C = 6.3 ppm/°C (measured), internally daisy-chained to allow independent monitoring of each LCCC side (1/4 of LCCC), with side-brazed copper alloy compliant leads with a diagonal lead stiffness of K_D = 52 lb/in (calculated), 256 chip capacitors CC1820, α_C = 6.8 ppm/°C (measured), with metallization caps shorted with conductive epoxy on capacitor top,

Substrate:

FR-4 multilayer board, α_S = 16.0 ppm/°C (measured), for greater CTE-mismatches and greater test acceleration laid out to provide common ground and individual signal conductors to allow independent continuity monitoring of each side of each chip carrier and of groups of 8 chip capacitors daisy-chained together.

Test vehicles (TVs):

not conformal coated

Test Parameters:

Temperature cycling from 0°C to 100°C at 24 cycles/day,
t_D = 15 min, ΔT_e =100°C and T_{SJ} = 50°C

Reliability Estimates:

From Accelerated Test Results:

Ceramic Chip Carrier: Using Equations 5, 12, and 14 and the following parameters:

(use): $\Delta\alpha$ = 4.2 ppm/°C, t_D = 715 min, ΔT_e = 28 and 48°C and T_{SJ} = 67 and 57°C at ΔT = 40 and 60°C, respectively;

Table 1A Results of Accelerated Reliability Test

	Cycles-To-Failure for Daisy-Chains							
Failure No.	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*
1/4 LCCC	146	196	388	418	486	540	568	628
8 CC1820	2718	3463	3826	4161	4397	4631	4738	5022
Failure No.	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*
1/4 LCCC	676	684	690	820	850	878	902	926
8 CC1820	5206	5372	5489	5598	5823	5978	6073	6223
Failure No.	*17*	*18*	*19*	*20*	*21*	*22*	*23*	*24*
1/4 LCCC	1038	1044	1096	1122	1206	1214	1298	1350
8 CC1820	6397	Test terminated at 6,400 cycles						
Failure No.	*25*	*26*	*27*	*28*	*29*	*30*	*31*	*32*
1/4 LCCC	1386	1480	1536	1602	1716	1840	2002	2432
8 CC1820	Test terminated at 6,400 cycles							

$N_f(50\%)$ = 982 and 6310 accelerated cycles-to-failure for the LCCC sides and the 8 CC1820 daisy-chains, respectively. Applying the partition correction from Equation 16 results in $N_f(50\%)$ = 491 and 10612 accelerated cycles-to-failure for the LCCCs and the CC1820s, respectively.

(test): $\Delta\alpha$ = 9.7 ppm/°C, t_D = 15 min, ΔT_e = 100°C and T_{SJ} = 50°C.

$\rightarrow N_f(50\%)$ = 1,500,000 and 183,000 cycles at ΔT = 40 and 60°C, respectively, and applying the statistical distribution from Equation 4

$\rightarrow N_f(0.5\%)$ = 128,000 and 15,500 cycles at ΔT = 40 and 60°C, respectively.

CC1820 Chip Capacitor: Using Equations 5, 12, and 13 and the following parameters:

(use): $\Delta\alpha$ = 3.7 ppm/°C, t_D = 715 min, ΔT_e = 40 and 60°C and T_{SJ} = 65 and 55°C at ΔT = 40 and 60°C, respectively,

(test): $\Delta\alpha$ = 9.2 ppm/°C, t_D = 15 min, ΔT_e = 100°C and T_{SJ} = 50°C

$\rightarrow N_f(50\%)$ = 149,000 and 73,000 cycles at ΔT = 40 and 60°C, respectively, and applying the statistical distribution from Equation 3

$\rightarrow N(0.5\%)$ = 43,300 and 21,400 cycles at ΔT = 40 and 60°C, respectively.

From Reliability Prediction Model:

Ceramic Chip Carrier: Using Equation 4 and the following parameters:

L_D = 0.674 in, K_D = 52 lb/in, h = 0.005 in, A = 6 x 10^{-6} in^2, F = 1.0, β = 2, $\Delta\alpha$ = 4.2 ppm/°C, T_C = 93°C, T_S = 85°C, $T_{C,0} = T_{S,0}$ = 45/25°C.

$\rightarrow N_f(0.5\%)$ = 127,000 and 15,500 cycles at ΔT = 40 and 60°C, respectively

CC1820 Chip Capacitor: Using Equation 3 and the following parameters:

L_D = 0.080 in, h = 0.005 in F = 0.7, β = 4, $\Delta\alpha$ = 3.7 ppm/°C, $T_C = T_S$ = 85°C $T_{C,0} = T_{S,0}$ = 45/25°C.

$\rightarrow N_f(0.5\%)$ = 43,300 and 21,400 cycles at ΔT = 40 and 60°C, respectively.

Conclusion:

Excellent agreement between the reliability estimates from analytical model reliability predictions and from accelerated testing. The two components analyzed have large reliability margins for these use environments; a system with 33 chip carriers and 100 CC1820s would just reach a cumulative failure probability of 0.5% after 10 years.

If the conformal coating has been shown in separate tests to increase the number of cycles to failure, then the cycles to failure in product use are likely higher than indicated here.

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How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:
Jeanette Ferdman, Membership Manager
tel 847/790-5309 fax 847/509-9798
e-mail: JeanetteFerdman@ipc.org www.ipc.org

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Application for Site Membership

Thank you for your decision to join IPC. IPC Membership is **site specific,** which means that IPC member benefits are available to all individuals employed at the site designated on the other side of this application.

PLEASE CHECK APPROPRIATE CATEGORY

To help IPC serve your member site in the most efficient manner possible, please tell us what your facility does by choosing the most appropriate member category.

■ **INDEPENDENT PRINTED BOARD MANUFACTURERS**

Our facility manufactures and sells to other companies, printed wiring boards or other electronic interconnection products on the merchant market.

WHAT PRODUCTS DO YOU MAKE FOR SALE?

☐ One-sided and two-sided rigid printed boards
☐ Multilayer printed boards
☐ Flexible printed boards
☐ Flat cable
☐ Hybrid circuits
☐ Discrete wiring devices
☐ Other interconnections

Name of Chief Executive Officer/President_____

■ **INDEPENDENT PRINTED BOARD ASSEMBLERS EMSI COMPANIES**

Our facility assembles printed wiring boards on a contract basis and/or offers other electronic interconnection products for sale.

☐ Turnkey
☐ SMT
☐ Chip Scale Technology
☐ Through-hole
☐ Mixed Technology
☐ Consignment
☐ BGA

Name of Chief Executive Officer/President_____

■ **OEM – MANUFACTURERS OF ANY END PRODUCT USING PCB/PCAS OR CAPTIVE MANUFACTURERS OF PCBS/PCAS**

Our facility purchases, uses and/or manufactures printed wiring boards or other electronic interconnection products for our own use in a final product. Also known as original equipment manufacturers (OEM).

IS YOUR INTEREST IN:

☐ purchasing/manufacture of printed circuit boards
☐ purchasing/manufacturing printed circuit assemblies

What is your company's main product line?

_____

■ **INDUSTRY SUPPLIERS**

Our facility supplies raw materials, machinery, equipment or services used in the manufacture or assembly of electronic interconnection products.

What products do you supply?

_____

■ **GOVERNMENT AGENCIES/ ACADEMIC TECHNICAL LIAISONS**

We are representatives of a government agency, university, college, technical institute who are directly concerned with design, research, and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

Please be sure to complete both pages of application.

Application for Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Company Name

Street Address

City | State | Zip | Country

Main Phone No. | Fax

Primary Contact Name

Title | Mail Stop

Phone | Fax | e-mail

Senior Management Contact

Title | Mail Stop

Phone | Fax | e-mail

Please check one:

❑ $1,000.00 Annual dues for Primary Site Membership (Twelve months of IPC membership begins from the time the application and payment are received)

❑ $800.00 Annual dues for Additional Facility Membership: Additional membership for a site within an organization where another site is considered to be the primary IPC member.

❑ $600.00** Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than $1,000,000.00. **Please provide proof of annual sales.

❑ $250.00 Annual dues for Government Agency/University/not-for-profit organization

TMRC Membership ❑ Please send me information on Membership in the Technology Marketing Research Council (TMRC)

AMRC Membership ❑ Please send me information for Membership in the Assembly Marketing Research Council (AMRC)

Payment Information

Enclosed is our check for $_____

Please bill my credit card: (circle one) MC AMEX VISA DINERS

Card No. _____ Exp date _____

Authorized Signature _____

Mail application with check or money order to:

IPC
Dept. 851-0117W
P.O. Box 94020
Palatine, IL 60094-4020

Fax/Mail application with credit card payment to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Tel: 847 509.9700
Fax: 847 509.9798

PLEASE ATTACH BUSINESS CARD OF OFFICIAL REPRESENTATIVE HERE

ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

Standard Improvement Form

IPC-SM-785

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798

1. I recommend changes to the following:

___ Requirement, paragraph number _____

___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name Telephone

Company E-mail

Address

City/State/Zip Date

ASSOCIATION CONNECTING
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