A Digital Current-Mode Control Technique for DC–DC Converters

Souvik Chattopadhyay and Somshubhra Das

***Abstract*—The objective of this paper is to propose a simple digital current mode control technique for dc–dc converters. In the proposed current-mode control method, the inductor current is sampled only once in a switching period. A compensating ramp is used in the modulator to determine the switching instant. The slope of the compensating ramp is determined analytically from the steady-state stability condition. The proposed digital current-mode control is not predictive, therefore the trajectory of the inductor current during the switching period is not estimated in this method, and as a result the computational burden on the digital controller is significantly reduced. It therefore effectively increases the maximum switching frequency of the converter when a particular digital signal processor is used to implement the control algorithm. It is shown that the proposed digital method is versatile enough to implement any one of the average, peak, and valley current mode controls by adjustment of the sampling instant of the inductor current with respect to the turn-on instant of the switch. The proposed digital current-mode control algorithm is tested on a 12-V input and 1.5-V, 7-A output buck converter switched at 100 kHz and experimental results are presented.**

***Index Terms*—Current-mode control, dc–dc converters, digital control, digital current-mode control, steady-state stability, voltage-mode control, voltage regulator (VR), voltage regulator module (VRM).**

I. Introduction

ONE OF THE advantages of a digital controller is that it is programmable. It is also immune to component changes that may arise due to changes in the ambient conditions. If the digital controller is coded in the hardware description language (HDL) such as VHDL then it becomes independent of the process technology. The same design can therefore be integrated with other digital systems without any modification. It is shown that for power factor corrector (PFC) systems implementation of advanced control techniques in digital hardware result in improved voltage loop dynamic responses. The digital controller can precisely match the duty ratios of interleaved dc–dc converters for voltage regulator module (VRM) applications. In general, it is well accepted that digital controller offers more functionality to the system compared to the analog controllers.

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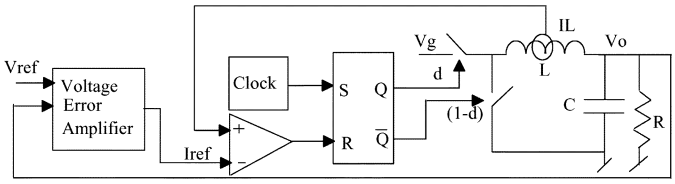


Fig. 1. Block diagram of the analog current-mode control of dc–dc converter.

However, in the past, most of the power electronic converters employed analog control methods. The reason is that the components such as microprocessors, analog to digital converters (ADCs), and digital to analog converters (DACs) that are required for digital implementation were expensive. Moreover, the digital controllers of the previous era had bandwidth problems due to the lower clock speed of the microprocessors. As a result, usage of digital control methods was limited to low switching frequency high power applications such as motor drives. The applications such as control of high frequency dc–dc converters were considered to be unsuitable for digital implementation.

In the last ten years the situation has changed significantly. The digital signal processors (DSPs) and the ADCs and the DACs have improved their performances in speed and functionality. They are now available at a much lower cost. The hardware cells of field programmable gate array (FPGA) devices can be configured by HDL based design, simulation, synthesis, and verification tools to function as a digital controller for a wide range of applications. Efforts are being made to implement a single chip digital controller with optimized hardware for low voltage high current dc–dc converter application, such as a voltage regulator module (VRM). The current trend shows that even for a high frequency application such as dc–dc conversion the digital control option is quite feasible.

Most of the digital controllers so far reported in literature employ the voltage-mode control principle [1]–[6] for VRM. However, current-mode control may be preferred over voltage-mode control because VRM requires adaptive voltage positioning (AVP), which can easily be implemented in current-mode control [7]. It therefore follows that there is a need to analytically develop a digital current-mode control technique for dc–dc converters. The main difficulty in implementation of current-mode control in digital hardware lies in the fact that the switching frequency of the converter is in the range of hundreds of kHz to 1 or 2 MHz. As a result it may only be possible to sample the fast changing inductor current only once in a switching period. Otherwise it would require a very fast ADC and excessively complex digital signal processing

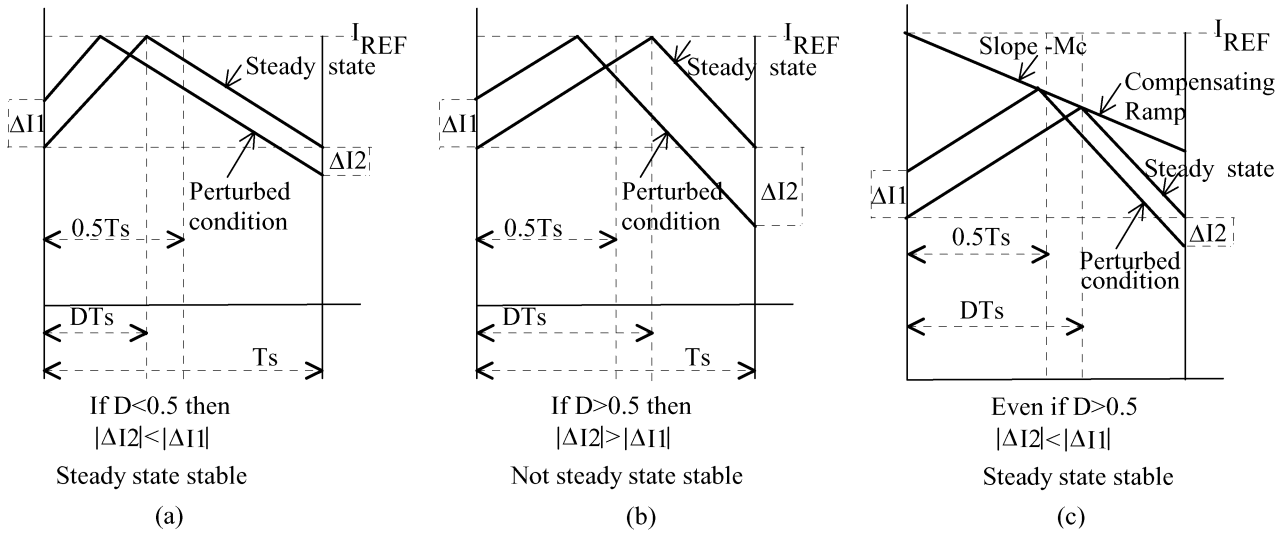
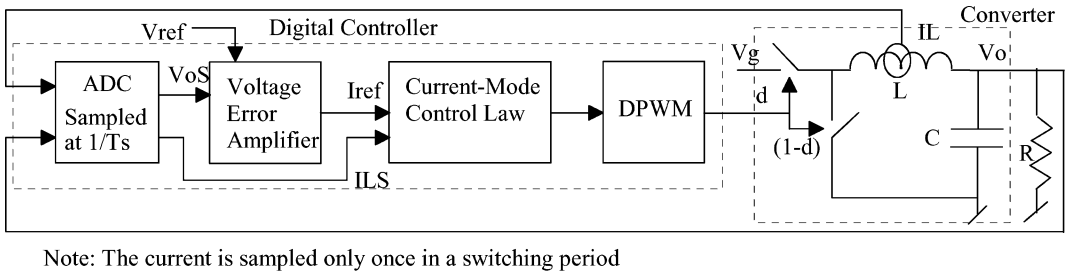


Fig. 2. (a) Operating principle of analog current-mode control. (b) The problem of steady-state stability for duty ratio greater than 0.5. (c) The use of compensating ramp to ensure stability for duty ratio greater than 0.5.



Note: The current is sampled only once in a switching period

Fig. 3. Block diagram of the digital current-mode control of dc–dc converters.

hardware. The digital control architecture proposed in [8] has implemented peak current-mode control in analog domain because of this reason. The digital current programmed control developed in [9] samples the current only once in a switching period but is based on predictive control principle requiring the usage of converter quantities in the control law, such as inductance and the input and output voltages. In contrast, the control technique proposed in this paper follows the current-mode control principle [10] directly.

In this method, the controller samples the inductor current at the rate of the switching frequency of the converter. The duty ratio of the next switching period is calculated by solving for the instant at which the sampled current becomes equal to the periodic waveform in the modulator obtained by adding the compensating ramp to the output of the voltage error amplifier. The steady-state stability analysis of the proposed digital current-mode control method gives the slope of the compensating ramp. This paper has described the three structures of the digital pulse width modulator (DPWM) that can implement peak, average and valley current-mode controls. Experimental results of a 1.5-V, 7-A buck converter switched at 100 kHz are presented to validate the proposed digital current-mode control method and the associated stability condition. In implementation, TI's general purpose DSP starter kit eZdspLF2407A is used as the digital controller.

II. Digital Controller

The block diagram of a dc–dc converter that uses analog current-mode control scheme is shown in Fig. 1. In the control structure the output of the voltage error amplifier is treated as the current reference $i_{\rm ref}$ by the modulator. Under steady-state the current reference is a dc quantity $i_{\rm ref} = I_{\rm ref}$. The modulator of the current-mode controller consists of a clock generator, an S-R F/F, and a comparator. The operating principle of analog current-mode control, the problem of steady-state stability for duty ratio greater than 0.5 and the use of compensating ramp as solution to the problem are well known. They are shown in Fig. 2(a)–(c), respectively. The corresponding block diagram for digital implementation is shown in Fig. 3. It may be noted that the digital controller samples the sensed current only once in every switching period. Therefore, the actual trajectory of the inductor current within the switching period is not known to the controller. This implies that in digital implementation a comparison of the sampled current and the current reference will produce duty ratio either 1 or 0. The method proposed in [9] uses system information such as converter topology, the inductance and the input and output voltages to estimate the slope of the current within a switching period and thereby can produce a duty ratio between 1 or 0. However, as proposed in this paper, the duty ratio d can be determined from a much

simpler current-mode control law if we add a periodic compensating ramp $i_c(t) = -mc \cdot t, 0 \le t \le T_s$ to the current reference $I_{\rm ref}$ in order to generate the modulator current expression $i_M(t) = I_{\rm ref} + i_c(t)$ and then by finding out the instant (dT_s) at which the sampled current $i_{\rm LS}$ becomes equal to $i_M(t)$ or (1) is satisfied

$$i_{\rm LS} = I_{\rm ref} - m_c \cdot dT_s. \tag{1}$$

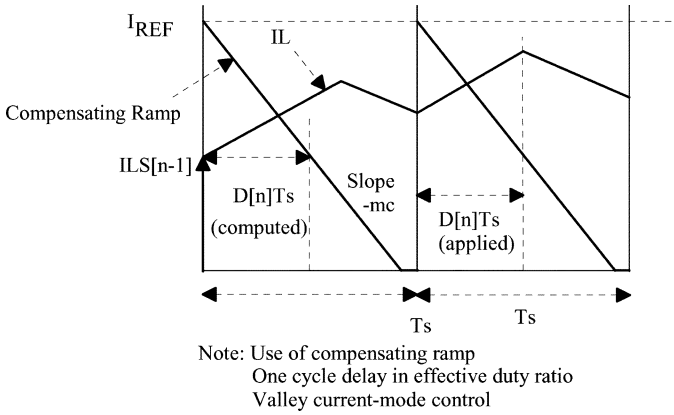
The duty ratio can therefore be expressed as

$$d = \frac{I_{\rm ref} - i_{\rm LS}}{m_c T_s}. \tag{2}$$

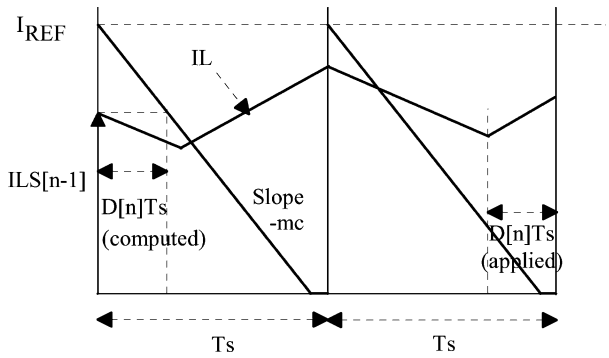
The discrete control law for the "nth" switching cycle can be derived from (2) as

$$d[n] = x[n-1] = \frac{I_{\rm ref} - i\mathrm{Ls}[n-1]}{m_c T_s}. \tag{3}$$

The previous equation indicates that current is sampled at the beginning of a control cycle, let us say "$n-1$." The period of the control cycle is equal to the switching period T_s of the converter. Subsequently in the same control cycle the digital controller computes the right hand side of (3), given by $x[n-1]$. This computation will take finite time, that may even be more than $x[n-1]T_s$, though it must be less than T_s. Therefore the value $x[n-1]$ is unsuitable to be used as the duty ratio of the period "$n-1$." We therefore equate $x[n-1]$ to $d[n]$, that is the duty ratio of the next switching period. It is depicted in Fig. 4(a) for valley current-mode control. It may be noted that in that figure $x[n-1]T_s$ is represented by "$d[n]T_s$ computed" to indicate the actual procedure and $d[n]$ in (3) relates to "$d[n]T_s$ applied." The current sampled in this method is treated as the valley current of the inductor, therefore the beginning of the control period and the turn-on instant of the switch are synchronized. However, as shown in Fig. 4(b), if we start every control period with the off-time of the switch then peak current mode control can be implemented. It is also possible to implement average current-mode control with appropriate choice of the sampling instant as shown in Fig. 4(c). In this case, the on-duration of the switch is placed symmetrically around the center of the switching period. Therefore, under steady-state, the sampled current will be equal to the average current of the inductor. This type of sampling of current has a practical advantage over the inductor current samples taken at the valley or at the peak. In a practical circuit the analog current sense signal is distorted by the noise picked up at the moment the inductor current changes its slope due to turn-on or turn-off of the switch. This transient almost dies down if the sample is taken at the instant when the inductor current reaches its average value.



(a)



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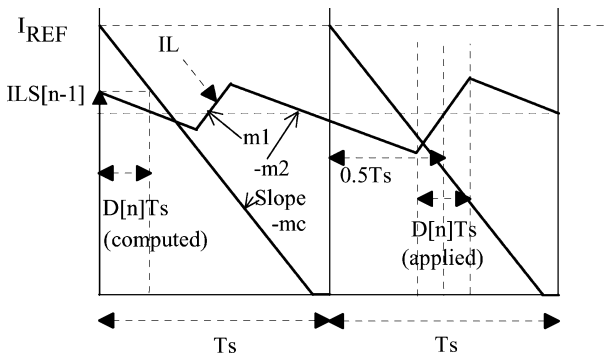


(c)

Fig. 4. Proposed digital current-mode control method for implementation of valley current-mode control.

III. Digital Pulse Width Modulator (DPWM)

The function of the DPWM is to produce in digital hardware the switching signals that correspond to the calculated duty ratio. In the proposed implementation it essentially consists of a counter and a digital comparator as shown in Fig. 5. The counter is connected to a clock generator that runs at a frequency $(F_{\rm clk})$, which is an integer multiple of the switching frequency $F_s = (1/T_s)$ of the converter. This pulse width modulator being digital in nature can only produce switching signals with discrete values of duty ratios. The duty ratio resolution is given by the ratio $F_s/F_{\rm clk}$. The output of the counter is connected to one of the inputs of the comparator. The other input of the comparator is connected to a compare-register that holds the value of duty ratio which has already been computed using (3). The loading of the compare-register is done in synchronism with the period interrupt. The counter in any one of it's counting mode (such as continuous-up or continuous up-down) produces

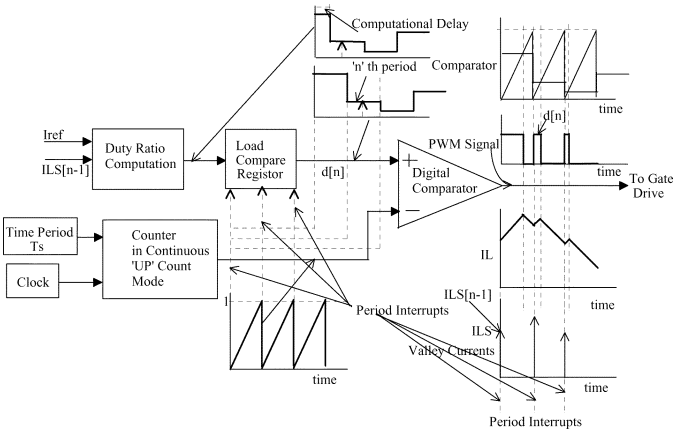


Fig. 5. DPWM structure to implement valley current-mode control.

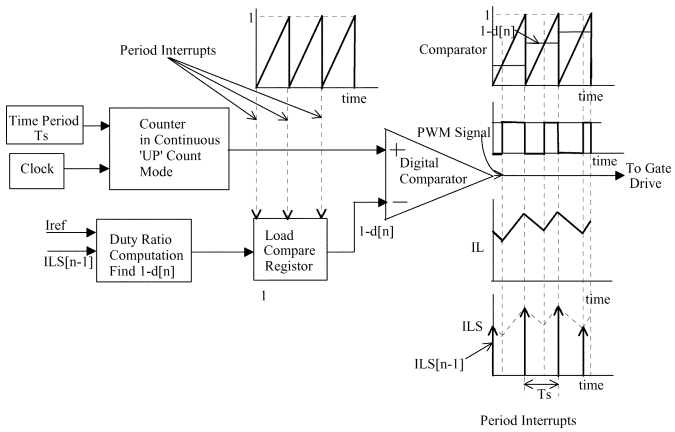


Fig. 6. DPWM structure to implement peak current-mode control.

period interrupt corresponding to the switching period of the converter.

In the connection configuration shown in Fig. 5 the counter is in continuous-up counting mode with a period value corresponding to T_s. The non-inverting terminal of the comparator is connected to the output of the compare register and the inverting terminal is connected to the output of the counter. The resultant switching pulses and the corresponding current waveforms are also shown in Fig. 5. It may be noted that this configuration of DPWM implements valley current-mode control.

However the structure of DPWM is versatile enough to implement average and peak current-mode control as well. For peak current-mode control, a value corresponding to $(1-d[n])Ts$ is loaded into the compare-register. The compare-register in this case is connected to the inverting terminal of the digital comparator. The output of the counter, that operates in the continuous-up counting mode, is connected to the non-inverting terminal. The resultant switching pulses and the corresponding current waveforms for peak current-mode control are shown in Fig. 6.

For average current mode control, shown in Fig. 7, the counter is operated in continuous-up-down counting mode with the counter loaded with a value corresponding to $T_s/2$. An integer corresponding to $(1-d[n])/(2)T_s$ is loaded to the

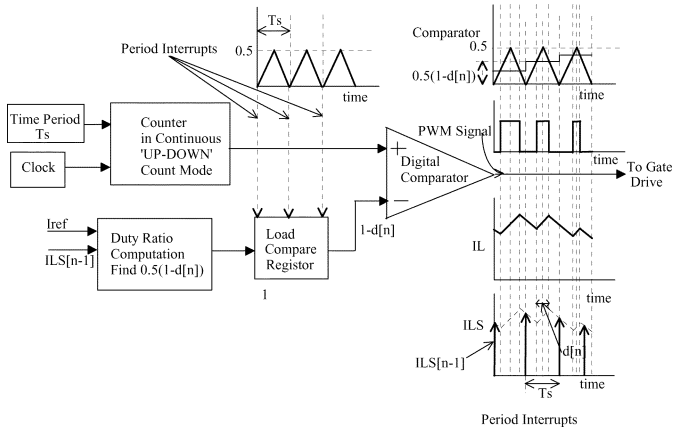


Fig. 7. DPWM structure to implement average current-mode control.

compare-register and it is connected to the inverting terminal of the digital comparator. It may be noted that though the currents are sampled at the beginning of the control cycle in all the three cases of current-mode control, still three different types of current-mode control are implemented by changing the configuration of the DPWM. These variations appear due to the placement of the on-duration of the switch at different times with respect to the period interrupt of the counter within a control cycle.

IV. Steady-State Stability Analysis

The use of a compensating ramp to ensure steady-state stability of the inductor current at duty ratio >0.5 is well known in analog current-mode control schemes. In the proposed digital current-mode control scheme the compensating ramp is a part of the basic structure, as it is required irrespective of the operating duty ratio of the converter. The slope of the ramp needs to be suitably used as a parameter to achieve steady-state stability of the inductor current. The analysis given below determines the condition that the slope of the compensating ramp m_c must satisfy in implementation of the average current-mode control.

In order to describe how a perturbation ΔI_1 in the steady-state value of the sampled inductor current $I_{\rm LS}$ would propagate through successive cycles in the proposed control scheme, we have considered five consecutive control cycles as shown in Fig. 8. The waveforms of control cycle "0" indicate steady-state condition and ΔI_1 is the perturbation in the inductor current at the beginning of the control cycle "1." The sampled currents $I_{\rm LS}, I_{\rm LS1}, I_{\rm LS1}, I_{\rm LS2}, I_{\rm LS3}$ are drawn with arrow marks placed at the instant of sampling. The corresponding duty ratios d, d_1, d_1, d_2, d_3 calculated by the digital controller in control cycles 0, 1, 2, 3, and 4, respectively, but not used as the actual duty ratios of the switch in the same cycle, are shown in the top part of the figure. It can be interpreted from the control law in (3) that the duty ratio calculated in a cycle is effective as a switch duty ratio only in the next cycle of the DPWM, as has been indicated by a dotted arrow in the bottom part of the figure. The middle part of the Fig. 8 shows the waveform of the inductor current under perturbed condition where the perturbations $\Delta I_1, \Delta I_1, \Delta I_2, \Delta I_3, \Delta I_4$ are measured from the steady-state value $I_{\rm LS}$. Let the slope of the compensating ramp

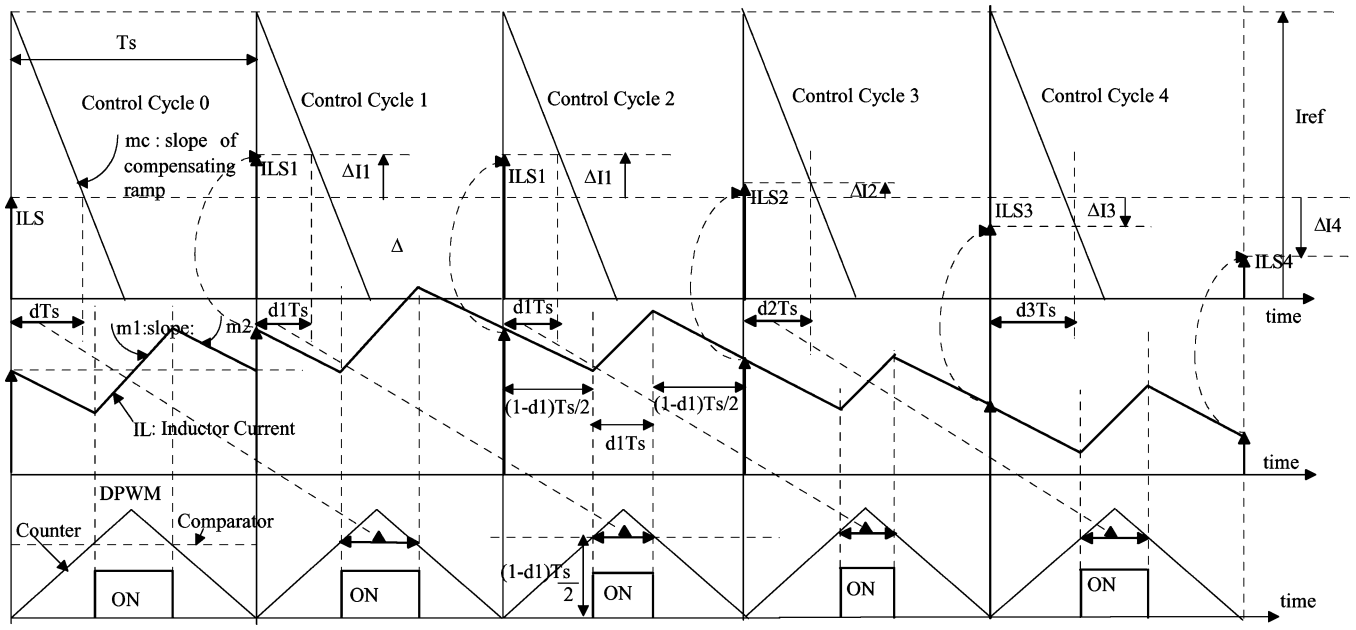


Fig. 8. Steady-state stability analysis of digital current-mode control.

be m_c, the slope of the inductor current during on-time be m_1 and the slope of the inductor current during off-time be m_2.

The steady-state condition for the inductor current is given by

$$m_1 d = m_2(1-d). \tag{4}$$

The duty ratio d in (4) is given by

$$I_{\rm LS} = I_{\rm ref} - m_c d T_s. \tag{5}$$

Let us consider control cycle "2," then d_1 is given by

$$I_{\rm LS1} = I_{\rm LS} + \Delta I_1 = I_{\rm ref} - m_c d_1 T_s. \tag{6}$$

We get (7) by subtracting (6) from (5)

$$\Delta I_1 = m_c(d-d_1)T_s \tag{7}$$

At the end of the control cycle "2" the perturbation is given by

$$\Delta I_2 = \Delta I_1 - (1-d_1)T_s m_2 + d_1 T_s m_1. \tag{8}$$

We get (9) by combining (4) and (8)

$$\frac{\Delta I_2}{\Delta I_1} = 1 - \frac{(m_1+m_2)(d-d_1)T_s}{\Delta I_1}. \tag{9}$$

We can derive (10) from (7) and (9)

$$\frac{\Delta I_2}{\Delta I_1} = 1 - \frac{(m_1+m_2)}{m_c}. \tag{10}$$

By proceeding identically for the control cycles "3" and "4" we can show that

$$\frac{\Delta I_3}{\Delta I_1} = \frac{\Delta I_2}{\Delta I_1} - \frac{(m_1+m_2)}{m_c}\frac{\Delta I_1}{\Delta I_1} = 1 - 2\frac{(m_1+m_2)}{m_c} \tag{11}$$

and

$$\frac{\Delta I_4}{\Delta I_1} = \frac{\Delta I_3}{\Delta I_1} - \frac{(m_1+m_2)}{m_c}\frac{\Delta I_2}{\Delta I_1} = 1 - 3\frac{(m_1+m_2)}{m_c} + \left(\frac{(m_1+m_2)}{m_c}\right)^2. \tag{12}$$

The generalized equation of perturbation at the end of "nth" control cycle is given by

$$\frac{\Delta I_n}{\Delta I_1} = \frac{\Delta I_{n-1}/\Delta I_1}{\Delta I_1} - \frac{(m_1+m_2)}{m_c}\frac{\Delta I_{n-2}/\Delta I_1}{\Delta I_1} \quad \text{for } n \geqslant 1, \quad \Delta I_0 = \Delta I_1, \quad \Delta I_{-1} = 0. \tag{13}$$

Let us define

$$R = \frac{(m_1+m_2)}{m_c}. \tag{14}$$

For $n=1$ to p, the corresponding values of $(\Delta I_n)/(\Delta I_1)$ are tabulated in Table I. In order to determine the convergence of the resultant series given by (13) we formulate (13) by a MATLAB code and vary R from 0.1 to 2. It is found that the series converges for $R<1$. The convergence of the series for the test case of 0.9 is shown in Fig. 9. Therefore we can conclude that the proposed digital current mode control satisfies steady-state stability condition if the compensating ramp m_c satisfies the following:

$$m_c > (m_1+m_2). \tag{15}$$

TABLE I
PROPAGATION OF THE RATIO OF CURRENT PERTURBATION IN "n" CYCLES

n	$\frac{\Delta I_n}{\Delta I_1}$
1	1
2	$1-R$
3	$1-2R$
4	$1-3R+R^2$
5	$1-4R+3R^2$
6	$1-5R+6R^2-R^3$
7	$1-6R+10R^2-4R^3$
8	$1-7R+15R^2-10R^3+R^4$
.	.....
p	$1-C_{1p}R+C_{2p}R^2-C_{3p}R^3+C_{4p}R^4+\ldots\ldots+C_{mp}R^m+\ldots.$ where, $C_{1p}=p-1$ $C_{mp}=\sum_{i=1}^{p-2} C_{(m-1)i}$, $m=2,\ldots,\frac{p}{2}$, *if p is even* $m=2,\ldots,\frac{p-1}{2}$, *if p is odd*

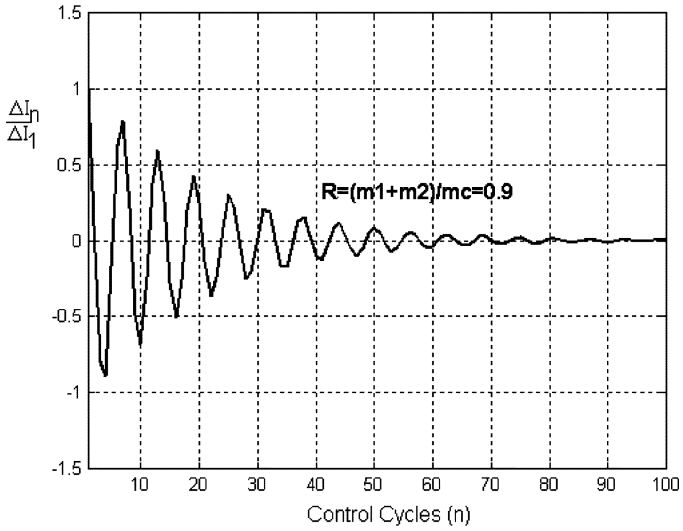


Fig. 9. Verification of steady-state stability for $R = ((m_1 + m_2)/m_c) = 0.9$.

This implies that for a buck converter (16), for a boost converter (17), and for a buck-boost converter (18) give the conditions for steady-state stability, where V_g and V_o are input and output voltages of the converter and L is the inductance

$$m_c > \left(\frac{V_g - V_o}{L} + \frac{V_o}{L} = \frac{V_g}{L}\right) \tag{16}$$

$$m_c > \left(\frac{V_g}{L} + \frac{V_o - V_g}{L} = \frac{V_g}{(1-D)L}\right) \tag{17}$$

$$m_c > \left(\frac{V_g}{L} + \frac{-V_o}{L} = \frac{V_g}{(1-D)L}\right). \tag{18}$$

It can be proved that if the control would have been without a delay of one cycle as in

$$d[n] = \frac{I_{\text{ref}} - i_{\text{LS}}[n]}{m_c T_s} \tag{19}$$

then the steady-state stability condition in terms of the slope of the compensating ramp is less stringent and is given by

$$m_c > \frac{(m_1 + m_2)}{2}. \tag{20}$$

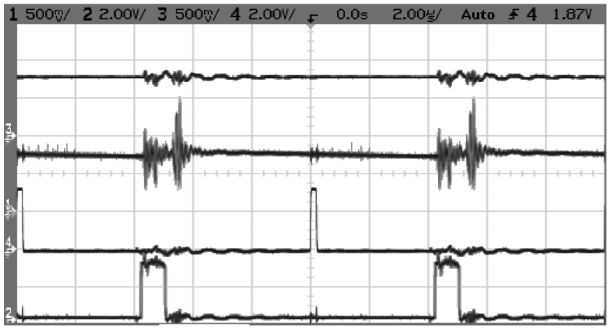
V. DIGITAL HARDWARE

A general purpose DSP board eZdspLF2407 based on Texas Instruments DSP TMS320LF2407 with internal 10 b, 500 ns conversion time ADC and DPWM hardware, is used for a compact realization of the proposed digital current-mode control method. In this case we have chosen average current-mode control for digital implementation because the noise in the current sense signal has almost no effect in this method as the current is sampled at the average value.

In the event manager module of the DSP a 16-b counter is programmed to work in the "continuous up-down" counting mode. This requires that the timer 1 period register T1PR be loaded with an integer value corresponding to the half of the switching period. In this case the DSP is clocked at 40 MHz, therefore, for a converter to be switched at 100 kHZ, T1PR is loaded with 200 because $200 * 25$ ns $= 0.5 * 10$ μs. The periodic "underflow" interrupt of the counter starts a new control cycle every time the interrupt comes. At the beginning of each control cycle the ADC is triggered to perform analog to digital conversions of the sensed inductor current and also the output voltage. Subsequently the duty ratio is computed from the digital expression corresponding to the right hand side of (3). In the algorithm the I_{ref} is replaced by $I_{\text{ref\_}D}$ obtained from the outer loop of the voltage error amplifier. It is a proportional-integral-derivative (PID) controller implemented in software. The computed value of the on-time of the switch gets loaded to the compare-register of the DPWM unit only at the next underflow condition of the counter. As a result the register value affects the duty ratio of the power switch at the subsequent control cycle.

VI. EXPERIMENTAL RESULTS

The proposed digital average current-mode control technique is tested on a $V_g = 12$-V input buck converter switched at 100 kHZ that produces nominal output of 1.5-V, 7-A. The inductance of the buck converter is $L = 27$ μH and the capacitance is $C = 100$ μF. The internal ADC of the eZdspLF2407 is 10-b and it's analog input has a conversion range of 0–3.3 V. Since the DSP has more (16 b) resolution than the ADC the output of the ADC is multiplied by a constant 8 in the code so as to reduce the effect of the truncation error in the control algorithm. Therefore, if the output voltage is 1.5 V then in the algorithm it corresponds to an integer $3720 = 8 * \text{round}((1.5/3.3) * 1024)$. The function "round" gives the nearest integer. The inductor current is sensed with an effective resistance of 0.22 Ω, therefore in the DSP algorithm the current I_L is equivalent to an integer $I_{\text{LSD}} = 8 * \text{round}(I_L * 0.22 * (1024/3.3))$. The steady-state stability condition can be calculated from (16) and for the values of L and V_g given above we get that the slope of the compensating ramp should be $m_c >$0.44 A/μs. We have chosen



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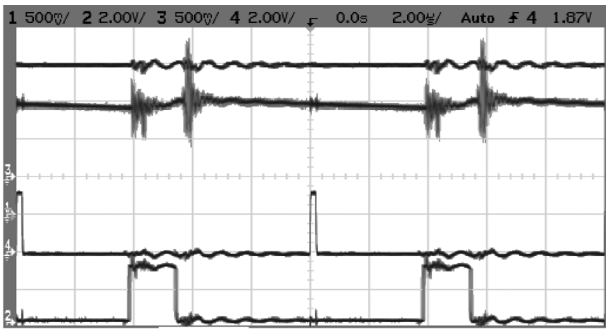
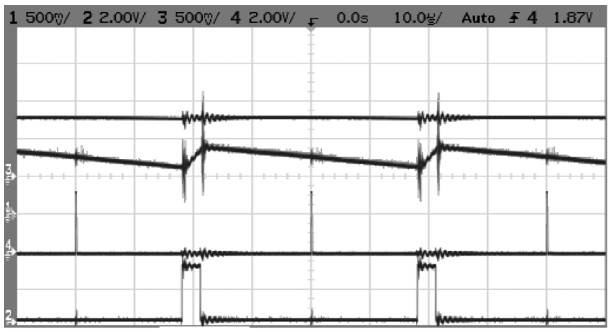


(b)

Fig. 10. Ch 1: Inductor current I_L (2.3 A/div), Ch 2: Duty ratio of the PWM pulses, Ch 3: Output voltage waveform V_o (0.5 V/div), Ch 4: Sampling instant of I_L (at positive edge): at switching frequency 100 kHz and $m_c = 0.9$ A/μs and (b) at switching frequency 100 kHz and $m_c = 0.9$ A/μs.



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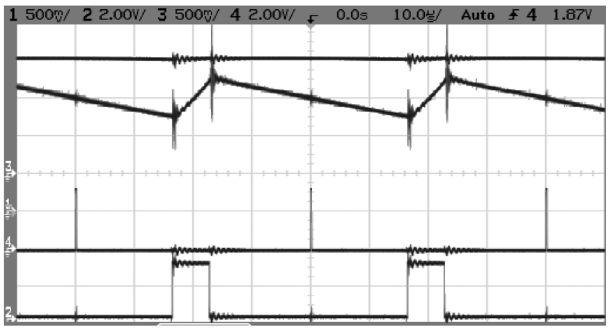

(b)

Fig. 11. Ch 1: Inductor current I_L (2.3 A/div), Ch 2: Duty ratio of the PWM pulses, Ch 3: Output voltage V_o (0.5 V/div), Ch 4: Sampling instant of I_L (at positive edge): (a) at switching frequency 25 kHz and $m_c = 0.9$ A/μs and (b) at switching frequency 25 kHz and $m_c = 0.9$ A/μs.

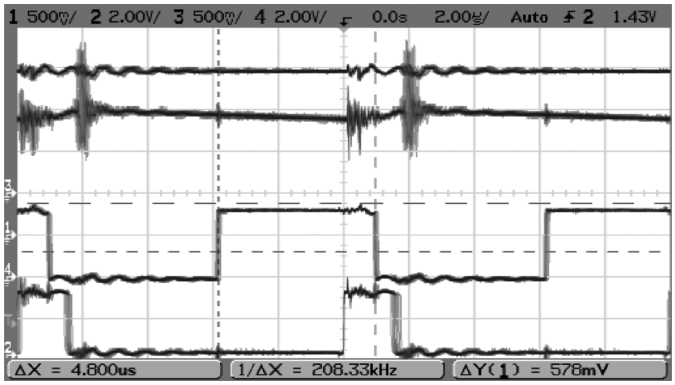

Fig. 12. Ch 1: Inductor current I_L (2.3 A/div), Ch 2: Duty ratio of the PWM pulses, Ch 3: Output voltage V_o (0.5 V/div), Ch 4: Execution time of the control algorithm is 4.8 μs (indicated by width of the high pulse).

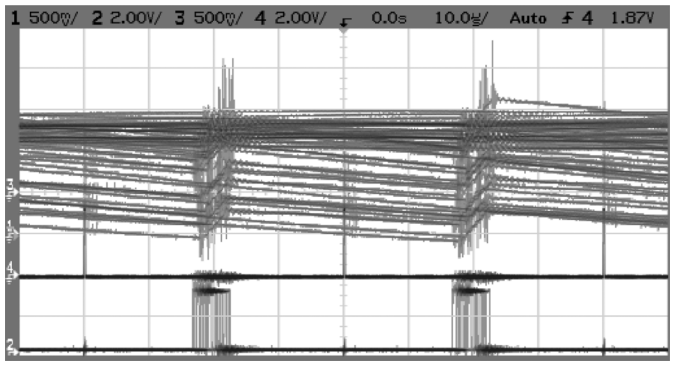

Fig. 13. Ch 1: Inductor current I_L (2.3 A/div), Ch 2: Duty ratio of the PWM pulses, Stability problem in the inductor current with $m_c = 0.37$ A/μs, or $m_{cD} = 10$.

$m_c = 0.9$ A/μs in the proposed implementation of the digital current-mode control algorithm. Since the switching period of 10 μs is equivalent to a count value of 200, that is used by the up-down counter of the eZdspLF2407, therefore the integer value corresponding to the slope $m_c = 0.9$ A/μs is given by $m_{cD} = \text{floor}(8 * \text{round}(0.9 * 0.22 * (1024/3.3))/20) = 24$. The function "floor" finds the nearest integer that is equal to or less than the value of the expression. The right hand side expression of (3) will therefore be calculated as $\text{floor}(I_{\text{ref}D} - i_{\text{LSD}}[n-1]/mcD)$ in the DSP algorithm, where $I_{\text{ref}D}$ is the output of the digital PID voltage error amplifier and the calculated integer value corresponds to the on-time of the switch.

The stability condition is experimentally verified at two different output voltages (1.5 V, 7 A) and (0.75 V, 3.5 A) by selecting $m_c = 0.9$ A/μs, as shown in Fig. 10. In Fig. 11, experimental results at converter switching frequency of 25 kHZ are presented for clear demonstration of the sampling instant in digital average current-mode control because in this case the ripple current is higher compared to the 100 kHZ case. In Figs. 10 and 11, Ch 1 shows the inductor current waveform I_L, Ch 2 shows the duty ratio of the PWM pulses, Ch 3 shows the output voltage waveform V_o, and Ch 4 shows the sampling instant (indicated by the positive edge) of the inductor current waveform or the instant at which the underflow-interrupt of DSP Timer 1 occurs. The execution time of the control algorithm is tested by setting one eZdspLF2407 port pin IOPA0 "high" at the beginning of the

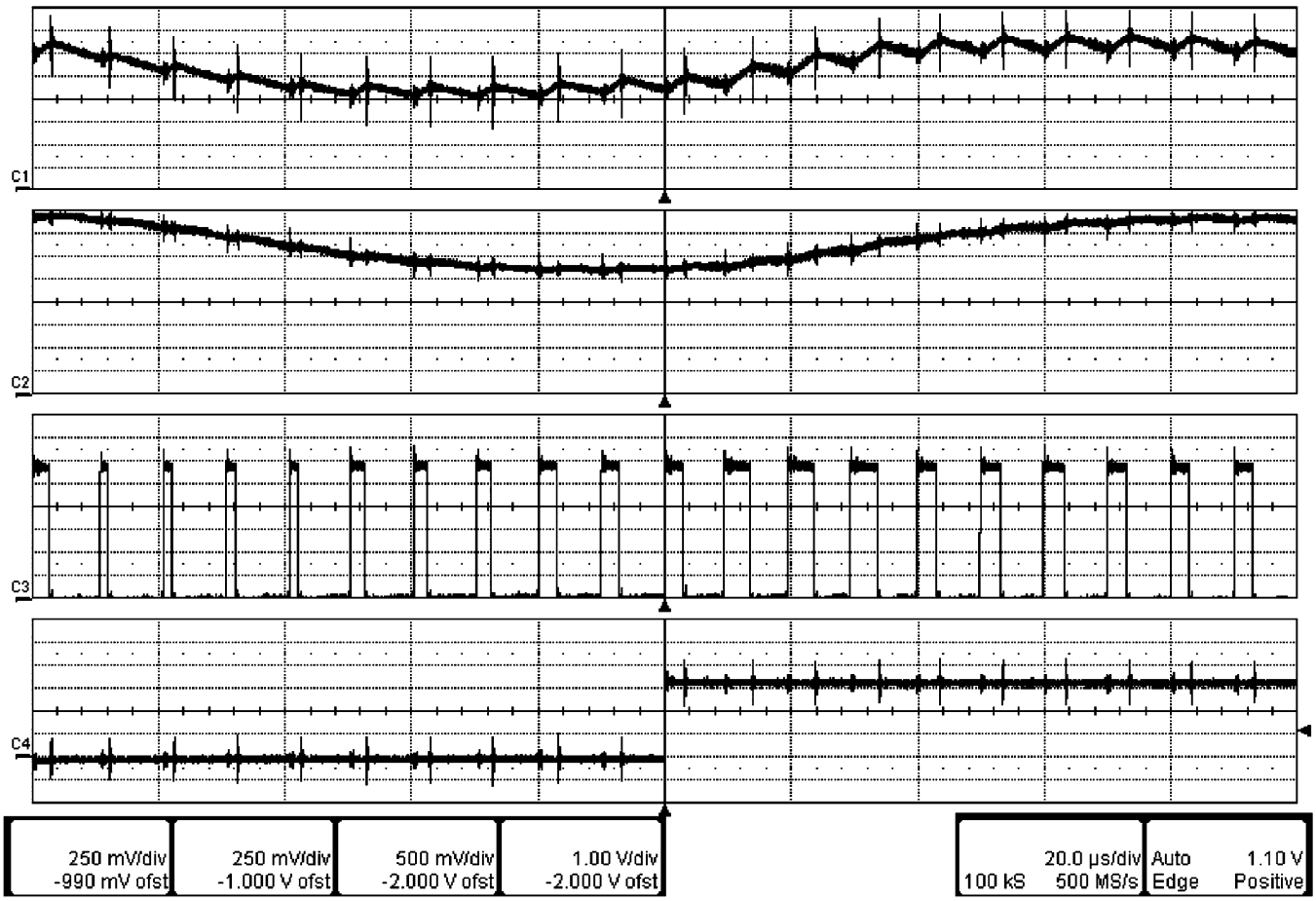

Fig. 14. Transient response of I_L with step variation in current reference from $I_{\mathrm{ref}D} = 5600$ to $I_{\mathrm{ref}D} = 7000$ (from 10.25 to 12.8 A). Ch 1: Inductor current I_L (1.15 A/div). Ch 2: Output voltage V_o (0.25 V/div). Ch 3: Duty ratio of the PWM pulses. Ch 4: Digital output indicating the instant $I_{\mathrm{ref}D}$ is changed (at the positive edge).

control cycle and then by setting it "low" at the end of the control algorithm with the last instruction of the control loop. The width of the Ch 4 waveform in Fig. 12 is found to be approximately 4.8 μs and it is considered to be the execution time of the proposed digital current-mode control algorithm. Fig. 13 shows that the digital current-mode control is unstable if we choose m_c =0.37 A/μs. In this case $m_{cD} = \mathrm{floor}(8{*}\mathrm{round}(0.37{*}0.22{*}(1024/3.3))/20) = 10$ is used as the design parameter in the expression $\mathrm{floor}(I_{\mathrm{ref}D} - i_{LSD}[n-1]/m_{cD})$ for computation of the switch on-times, thus violating the condition for steady-state stability, given by $m_{cD} > 12$. The performance of the proposed digital current-mode control technique under transient operating condition is shown in Fig. 14, where Ch 1 is the inductor current I_L, Ch 2 is the output voltage V_o, Ch 3 is the PWM pulses, and Ch. 4 is the output of a digital port. The transient response of the inner current loop is tested by keeping the outer voltage loop open and by changing the current reference command in the algorithm with a step from $I_{\mathrm{ref}D} = 5600$ to $I_{\mathrm{ref}D} = 7000$ (from 10.25 to 12.8 A) at the instant the Ch 4 waveform goes from "low" to "high" in Fig. 14. The corresponding response of the inductor current waveform is shown in Ch 1. It may be seen that the rise time of the inductor current is approximately 45 μs. In the proposed digital current-mode control, the current-loop bandwidth will decrease if the slope of the compensating ramp, m_{cD}, is increased, like analog current-mode control.

VII. Conclusion

This paper proposes a digital current-mode control technique for dc–dc converters and describes its digital implementation. The controller samples the inductor current at the rate of the switching frequency of the converter. The duty ratio of the period is determined by equating the sampled current to the equation of the modulator current that is obtained by adding the periodic compensating ramp to the output of the voltage error amplifier. The analysis presented in this paper determines the slope of the compensating ramp based on the condition of steady-state stability.

The advantage of the proposed digital current-mode controller is that in order to calculate the duty ratio of the period it is not necessary to know the value of the inductance and the input and output voltages of the converter. The computational burden on the DSP is less compared to other methods of digital current-mode control because a simpler duty ratio control law is implemented here. This means that when the same DSP is used for implementation of different current-mode controls the switching frequency of the converter can be higher in this

method. The configuration of the DPWM for implementations of all the three variations of current-mode control, namely peak, average, and valley current-mode controls, have been proposed. Experimental results of a 1.5-V, 7-A buck converter that is switched at 100 kHZ prove the validity of the proposed digital current-mode control method and also the stability condition. In implementation, TI's general purpose DSP starter kit eZdspLF2407 is used as the digital controller.

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