Design Guidelines for RCD Snubber of Flyback

Abstract
When the MOSFET turns off, a high voltage spike occurs on the drain pin because of a resonance between the leakage inductor (L lk) of the main transformer and the output capacitor (C OSS) of the MOSFET. The excessive voltage on the drain pin may lead to an avalanche breakdown and eventually damage of the MOSFET. Therefore, it is necessary to add an additional circuit to clamp the voltage. In this article, some design guidelines for RCD snubber of flyback converters are presented.

1. Introduction
One of the most simple topologies is a flyback converter. It is derived from a buck-boost converter by replacing filter inductors with coupled inductors, i.e. gapped core transformers. When the main switch turns on, the energy is stored in the transformer as a flux form, and the energy is transferred to output during the main switch off-time. Since the transformer needs to store energy during the main switch on-time, the core should be gapped. Since flyback converters need very few components, it is a very popular topology for low and medium power applications such as battery chargers, adapters, and DVD players.

Figure 1 shows that a flyback converter operates in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with several parasitic components such as primary and secondary leakage inductors, an output capacitor of MOSFET, and a junction capacitor of a secondary diode. When the MOSFET turns off, the primary current, id, charges C OSS of the MOSFET in short time. When the voltage across C OSS, V ds, exceeds the input voltage plus reflected output voltage, V in+nVo, the diode reverse recovery current.

Figure 1. Flyback converter; (a) configuration with parasitic components, (b) CCM operation, (c) DCM operation.
secondary diode turns on, so that the voltage across the magnetizing inductor, \( L_{in} \), is clamped to \( nV_o \). There is, therefore, a resonance between \( L_{lk1} \) and \( C_{OSS} \) with high frequency and high voltage surge. This excessive voltage on the MOSFET may be a main cause of its failure. In the case of the CCM operation, the secondary diode remains turned on until the MOSFET is gated on. Therefore, when the MOSFET turns on, a reverse recovery current of the secondary diode is added to the primary current, and thus, there is a large current surge on the primary current at the turn-on instance. Meanwhile, since the secondary current runs dry before the end of one switching period in the case of the DCM operation, there is a resonance between \( L_m \) and \( C_{OSS} \) of the MOSFET.

2. Snubber design

The excessive voltage due to a resonance between \( L_{lk1} \) and \( C_{OSS} \) should be suppressed to an acceptable level by an additional circuit in order to protect the main switch. The RCD snubber circuit and key waveforms are shown in figures 2 and 3, respectively. The RCD snubber circuit absorbs the current in the leakage inductor by turning on the snubber diode, \( D_{sn} \), when \( V_{ds} \) exceeds \( V_{in}+nV_o \). It is assumed that the snubber capacitance is large enough that its voltage does not change during one switching period.

When the MOSFET turns off and \( V_{ds} \) is charged to \( V_{in}+nV_o \), the primary current flows to \( C_{sn} \) through the snubber diode \( D_{sn} \). The secondary diode turns on at the same time. Therefore, the voltage across \( L_{lk1} \) is \( V_{sn}-nV_o \). The slope of \( i_{sn} \) is as follows:

\[
\frac{di_{sn}}{dt} = \frac{V_{sn} - nV_o}{L_{lk1}}
\]

where \( i_{sn} \) is the current flows into the snubber circuit, \( V_{sn} \) is the voltage across the snubber capacitor \( C_{sn} \), \( n \) is the turns ratio of the main transformer, and \( L_{lk1} \) is the leakage inductance of the main transformer. Therefore, the time \( t_s \) is obtained as follows:

\[
t_s = \frac{L_{lk1}}{V_{sn} - nV_o} \times i_{peak}
\]

where \( i_{peak} \) is the peak current of the primary current.

The snubber capacitor voltage, \( V_{sn} \), should be determined at the minimum input voltage and full load condition. Once \( V_{sn} \) is determined, the power dissipated in the snubber circuit at the minimum input voltage and full load condition is obtained as follows:

\[
P_{sn} = V_{sn} \frac{i_{peak} \cdot t_s}{2} f_s = \frac{1}{2} L_{lk} i_{peak}^2 \frac{V_{sn}}{V_{in} + nV_o} f_s
\]

where \( f_s \) is the switching frequency of the flyback converter. \( V_{sn} \) should be 2–2.5 times of \( nV_o \). Very small \( V_{sn} \) results in a severe loss in the snubber circuit as shown in the above equation.

On the other hand, since the power consumed in the snubber resistor \( R_{sn} \) is \( V_{sn}^2 / R_{sn} \), we can obtain the resistance as
follows:

\[ R_{sn} = \frac{1}{2} L_{lk1} \left( I_{\text{peak}} \right)^2 \frac{V_m^2}{V_m - n V_o} f_s \]

Then, the snubber resistor with proper rated power should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as follows:

\[ \Delta V_{sn} = \frac{V_m}{C_{sn} R_{sn} f_s} \]

In general, 5~10% ripple is reasonable. Therefore, the snubber capacitance is calculated using the above equation.

When the converter is designed to operate in CCM, the peak drain current together with the snubber capacitor voltage decreases as the input voltage increases. The snubber capacitor voltage under maximum input voltage and full load condition is obtained as follows:

\[ V_{sn} = \frac{n V_o + \sqrt{(n V_o)^2 + 2 R_{sn} L_{lk1} f_s (I_{\text{peak2}})^2}}{2} \]

where \( f_s \) is the switching frequency of the flyback converter, \( L_{lk1} \) is the primary side leakage inductance, \( n \) is the turns ratio of the transformer, \( R_{sn} \) is the snubber resistance, and \( I_{\text{peak2}} \) is the primary peak current at the maximum input voltage and full load condition. When the converter operates in CCM at the maximum input voltage and full load condition, the \( I_{\text{peak2}} \) is obtained as follows:

\[ I_{\text{peak2}} = \frac{P_{in} (V_{DC}^{\max} + n V_o)}{V_{DC}^{\max} \times n V_o} + \frac{V_{DC}^{\max} \times n V_o}{2 L_{in} f_s (V_{DC}^{\max} + n V_o)} \]

When the converter operates in DCM at the maximum input voltage and full load condition, the \( I_{\text{peak2}} \) is obtained as follows:

\[ I_{\text{peak2}} = \sqrt{\frac{2 P_{in}}{f_s L_m}} \]

where \( P_{in} \) is the input power, \( L_m \) is the magnetizing inductance of the transformer, and \( V_{DC}^{\max} \) is the rectified maximum input voltage in dc value.

Check if the maximum value of \( V_{ds} \) is below 90% and 80% of the rated voltage of the MOSFET (\( BV_{dss} \)), at the transient period and steady state period, respectively. The voltage rating of the snubber diode should be higher than \( BV_{dss} \). Usually an ultra-fast diode with a 1A current rating is used for the snubber circuit.

3. Example

In this section, an example will be shown. An adapter using FSDM311 has the following specifications: 85 \( V_{ac} \) to 265 \( V_{ac} \) input voltage range, 10 W output power, 5 V output voltage, and 67 kHz switching frequency. In the case where the RCD snubber uses a 1nF snubber capacitor and a 480k\( \Omega \) snubber resistor, Figure 4 shows several waveforms with 265 \( V_{ac} \) at the instance of the AC switch turn-on.

![Figure 4. Startup waveforms with 1 nF snubber capacitor and 480 k\( \Omega \) snubber resistor.](image)

There are the drain voltage (\( V_{ds} \), 200 V/div), the supply voltage (\( V_{cc} \), 5 V/div), the feedback voltage (\( V_{fb} \), 1 V/div), and the drain current (\( I_{d} \), 0.2 A/div) in the following order. The maximum voltage stress on the internal SenseFET is around 675 V as shown in Figure 4. However, the voltage rating of FSDM311 is 650 V according to the datasheet. There are two reasons for exceeding the voltage ratings. One is the wrong transformer design, the other is the wrong snubber design. Figure 5 gives an example of incorrect snubber design.

![Figure 5. Steady state waveforms with 1 nF snubber capacitor and 480 k\( \Omega \) snubber resistor.](image)
As mentioned above, for reliability the maximum voltage stress at the steady state should be equal to 80% of the rated voltage ($650 \text{ V} \times 0.8 = 520 \text{ V}$). Figure 5 shows the voltage stress on the internal SenseFET is above 570 V with $V_{in} = 265 \text{ V}_{ac}$ at steady state. However, the fact that $V_{in+nVo}$ is around 450 V ($= 375 \text{ V} + 15 \times 5 \text{ V}$) implies the turns ratio of the transformer is 15, which is a reasonable value. Therefore, the snubber circuit should be redesigned.

Let $V_{sn}$ be twice that of $nV_o$, 150 V. And $L_{lk1}$ and $i_{peak}$ is 150 $\mu$H and 400 mA by measuring, respectively. Then we obtain the snubber resistance as follows:

$$R_{sn} = \frac{1}{2} \frac{V_{sn}^2}{L_{lk1}i_{peak}^2} \frac{V_{sn} - nV_o}{150} f_s$$

$$= \frac{1}{2} \times 150 \times 0.4^2 \times \frac{150}{150 - 75} = 14k$$

And the power emission from $R_{sn}$ is calculated as follows:

$$P = \frac{V_{sn}^2}{R_{sn}} = \frac{150^2}{14k} = 1.6W$$

Let the maximum ripple of the snubber capacitor voltage be 10%, then the snubber capacitance is obtained as follows:

$$C_{sn} = \frac{V_{sn}}{\Delta V_{m} R_{sn} f_s} = \frac{120}{12 \times 14k \times 67k} = 10nF$$

The results with 1.4 k$\Omega$ (3 W) and 10 nF are shown in Figures 6 and 7.

The voltage stresses on the internal SenseFET are 593 V and 524 V at the startup and steady state, respectively. These are around 91.2% and 80.6% of the rated voltage of FSDM311, respectively.
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