

5V/550mA Battery Charger Solution Using AP3703

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01/19/2009

Summary of Report	
Specifications	85~264Vac, 5V/550mA
Applications	Cellphone charger or adapter
Key features	<ul style="list-style-type: none">• Primary Side Regulation (PSR) solution without opto-coupler• Pass Energy Star EPS 2.0 efficiency criteria with 5% margin• $\pm 4\%$ Constant Voltage (CV) regulation and $\pm 10\%$ constant current regulation with 1.8m AWG26 cable• Less than 150mW no load input power for universal line• Pass EN55022 Class B with over 6dB margin• High reliability guaranteed by built-in multi-protection functions, e.g. soft-start, OVP, OckP (Open Circuit Protection) and SCP (Short Circuit Protection) functions• Cost effective total charger solution, 24 components totally

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1. Introduction

This report describes a 2.75W constant voltage/constant current universal input power supply for cellphone charger or similar applications. This design was based on BCD's cost effective Primary Side Regulation (PSR) controller, AP3703. The mechanic dimensions are 45mm in length, 33 mm in width and 16mm in height.

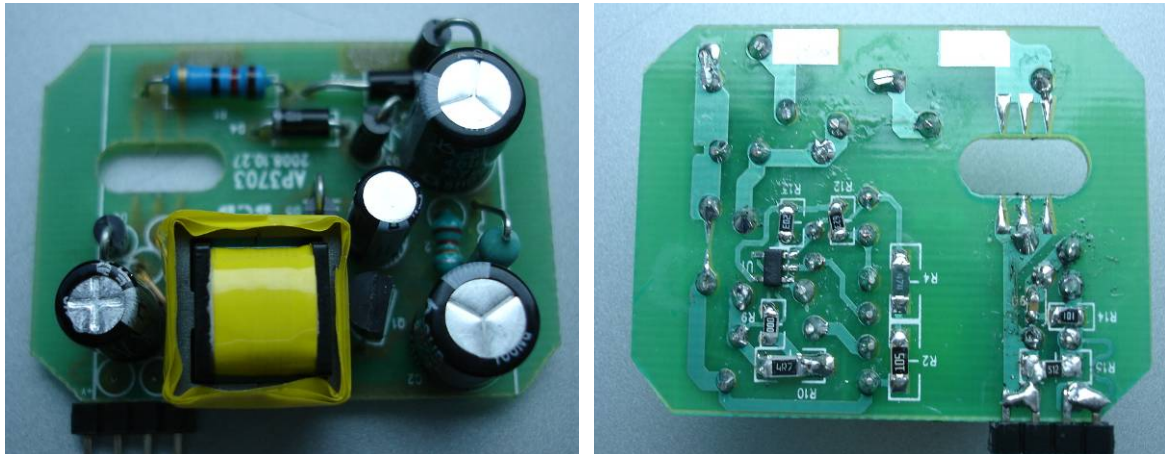


Figure 1. Photo of 5V/550mA demo board (Top view and bottom view)

The AP3703 is a general use AC/DC power supply controller for the cost effective battery charger and adapter application. It can achieve constant voltage and constant current (CV and CC) regulation without requiring an opto-coupler and secondary control circuitry. Meanwhile, it also eliminates the need of loop compensation circuitry while maintaining system stability. With the unique random frequency dithering technique, AP3703 system can get good EMI performance.

Compared with the traditional Pulse Width Modulation control for CV and CC control technique, this device uses Pulse Frequency Modulation (PFM) technique to achieve tight CV and CC regulation, which guarantees high efficiency at light loading and makes the charger system built with AP3703 easily to pass the active mode efficiency criteria of Energy Star EPS 2.0. Designed to work in Discontinuous Current Mode (DCM), the power system using the AP3703 operates with constant primary peak current and the CV regulation is realized by modulating switching frequency. So the switching frequency presents a linear characteristic with the change of the loading. The CC regulation is implemented by a fixed ratio between the conduction time and off time of the secondary schottky rectifier. The detailed operation principle can refer to the datasheet of AP3703.

The AP3703 consists of a 5V regulator, CV feedback and logic circuitry, constant peak

current setting circuit, leading edge blanking circuit, optimized BJT driver circuitry, over voltage/open circuit protection (OVP/OCP) circuitry and a PFM controller for CV and CC frequency modulation.

With the built-in soft-start, OVP, OCP and SCP (Short Circuit Protection) functions, the AP3703 can achieve high reliability in abnormal conditions without additional components and cost.

This document contains the power supply specification, schematic, BOM (bill of materials) including transformer architecture, PCB layout and key performance features with detailed test data and waveforms.

2. Specifications

Description	Min	Typ	Max	Units	Conditions
Input					
Voltage	85		264	VAC	
Frequency	47	50/60	63	Hz	
No Load Input Power			200	mW	
Output					
Output Voltage	4.75		6.5	V	bandwidth
Output Ripple Voltage			150	mVpp	
Output Current	550		950	mA	
Output Power (Pno)		2.75		W	
Output Voltage rise Time			20	ms	
Efficiency					
Average Efficiency at 25,50,75 and 100 % of Pno (EPS 2.0) ---note 1	63.7			%	Tested with 1.8m AWG 26 cable
EMI	Pass EN55022 Class B with 6dB margin				

Note 1:

The active mode average efficiency criterion of Energy Star EPS 2.0 was calculated as follow:

Table 1. EPS 2.0 Active Mode Efficiency Criteria

Low voltage Model (Nameplate $V_o < 6V$ and nameplate $I_o \geq 550mA$)	1 < to <49W	$[0.075 * \ln(Pno)] + 0.561$
Standard Model	1 < to <49W	$[0.0626 * \ln(Pno)] + 0.622$

3. Schematic

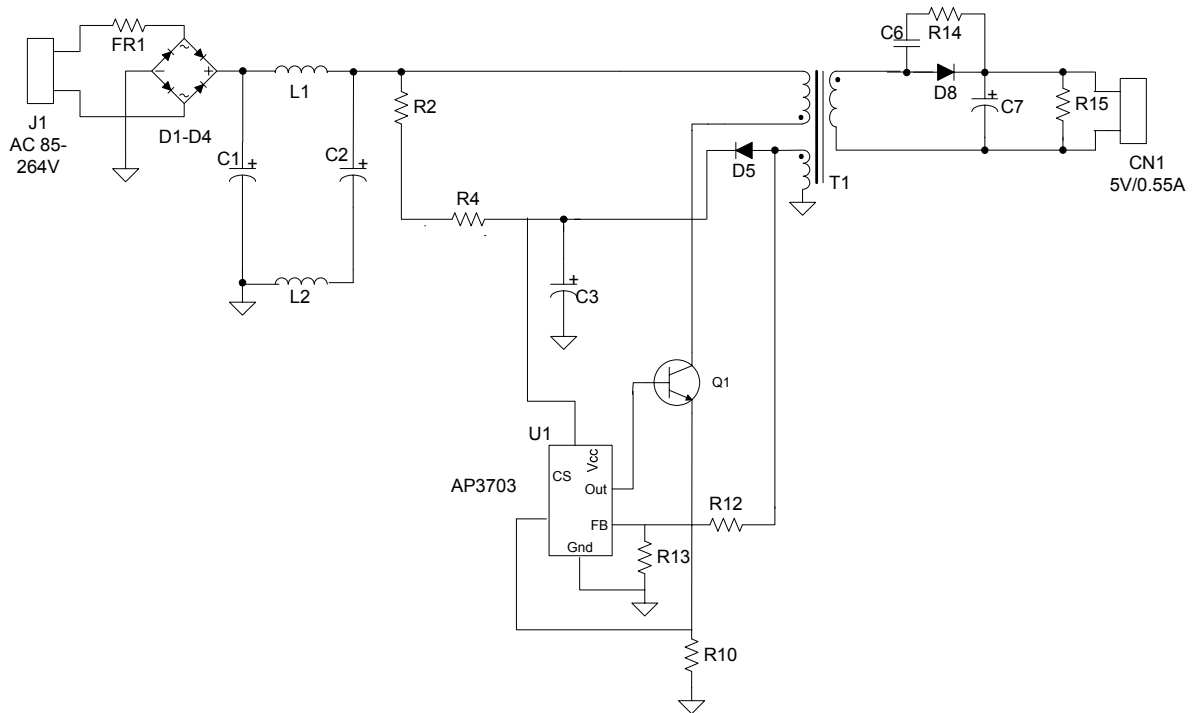


Figure 2. Schematic of 5V/550mA charger solution

4. Circuit Description

The power supply use AP3703 to realize a primary side regulation flyback converter.

4.1. AC input filter:

The AC line voltage is rectified by D1 to D4 to a DC bus voltage. C1, L1, L2 and C2 compose a Pi filter to achieve good EMI performance in attenuating the differential mode EMI noise, in which L1 are mainly to limit EMI noise in middle frequency (less than 1M). And R1 is used to limit the input surge current and also work as a fuse for ultimate protection in any catastrophic failure.

4.2. Power converter:

In the main power supply topology of a layback converter, the transformer T1 is magnetized and demagnetized by on/off control of the BJT transistor Q1. Thus the DC bus voltage in the primary side is converted to AC voltage on the secondary winding of T1. By an optimized driving circuitry within the AP3703, the maximum allowable peak voltage across

the collector of Q1 is V_{ces} , which makes the use of popular BJT transistor with 400V V_{ceo} and 700V V_{ces} feasible.

The output rectification circuitry is made up of a schottky diode D8 and an electrolytic capacitor C7. A dummy load R15 is used to control the output voltage in no load condition to an acceptable level.

4.3. AP3703 related circuitry:

A common auxiliary winding is adopted in this schematic for both CV feedback and bias supply. In the CV feedback network, R12 and R13 are required to use the resistors with 5% precision. And D5 and C3 constitute the bias supply circuitry for the AP3703. In order to ensure good driving effect for Q1, C3 should be placed as close as possible to Vcc pin of the AP3703

R2 and R4 compose the startup resistor and 1.5M ohm is recommended for the sum of these two resistors considering the tradeoff between a reasonable startup time and guaranteed reliable startup at low AC line. The primary peak current of the flyback converter is set by the current sense resistor R10 with 5% precision.

5. BOM and transformer specifications

5.1. BOM

Item	Description	QTY
C1	4.7uF/400V, 85° C, 8*12 electrolytic	1
C2	4.7uF/400V, 85° C, 8*12 electrolytic	1
C3	4.7uF/50V,105° C, 5*11 electrolytic	1
C6	1nF/100V, 0805,10%, ceramic	1
C7	470uF/16V, 6*11 electrolytic	1
D1,2,3,4	1N4007 DO-41 Rectifier Diode	4
D5	FR107 DO-41 Fast Recovery Diode	1
D8	SR260 DO-41 Schottky	1
L1	1mH,Inductor	1
L2	4.7uH,Inductor	1
R1	12 ohm, 1/2 W, Fuse resistor	1
R2	1M ohm, 5%,1206, resistor	1
R4	470k ohm, 5%, 1206, resistor	1
R10	1.8 ohm, 5%,1206, resistor	1
R12	56k ohm, 5%,0805, resistor	1
R13	36k ohm, 5%,0805, resistor	1
R14	100 ohm, 5%,0805, resistor	1
R15	2k ohm, 5%, 1206, resistor	1
T1	EE13 8pin 1.8mH 8%,Transformer	1
U1	AP3703, Sot23-5, BCD's IC	1
Q1	13003 TO-92, Power BJT	1

5.2. Transformer specifications

5.2.1. Electrical Diagram

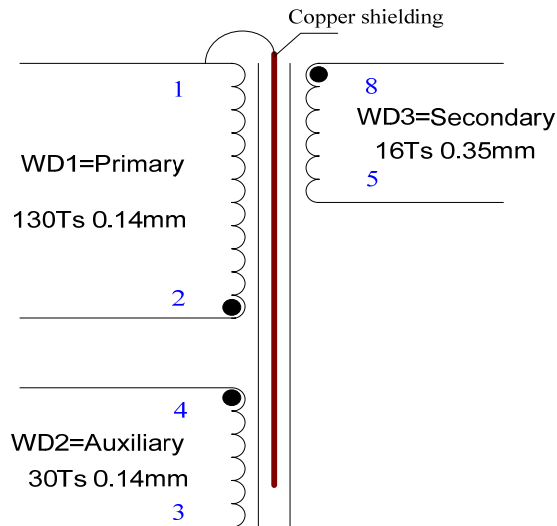


Figure 3. Transformer electrical diagram

5.2.2. Electrical Specifications

Primary Inductance	Pin2-1, all other windings open, measured at 1kHz, 0.4VRMS	1.8mH, ± 8%
Primary Leakage Inductance	Pin2-1, all other windings shorted, measured at 10kHz, 0.4VRMS	50uH (Max)
Electrical Strength	60 seconds, 60HZ, from Pin 2-1 to Pin8-7	3000Vac

5.2.3. Materials

Item	Description
[1]	Core: EE13, PC40 or equivalent
[2]	Bobbin: EE13, Horizontal, 8 Pin, (4/4)
[3]	Wire: \varnothing 0.14mm, for Primary Winding and Auxiliary Winding
[4]	Triple Insulated Wire: \varnothing 0.35mm for Secondary Winding
[5]	Tape: 0.05mm thick, 7.0 mm wide
[6]	Tape: 0.2mm thick, 1.0mm wide

[7]	Copper film: 0.05mm thick, 6.5 mm wide 31mm length
[8]	Glue: EPORITE 2095

5.2.4. Transformer Build Diagram

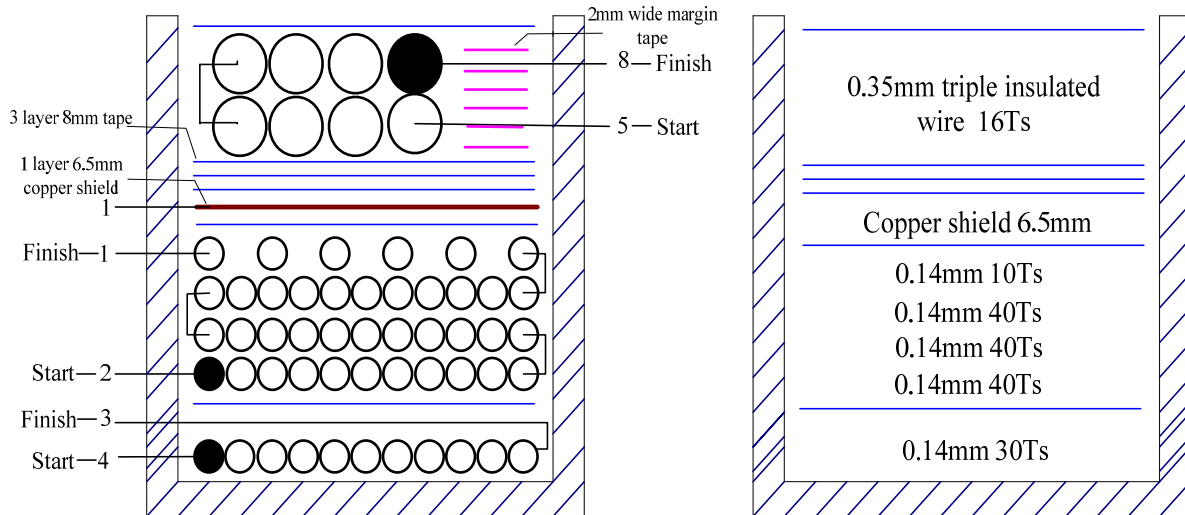


Figure 4. Transformer Build Diagram

5.2.5. Transformer Construction

Winding Sequence: Begin from the central column of the Bobbin. Primary side of the bobbin is placed on the left hand side, and secondary side of the bobbin is placed on the right hand side.	
WD 1 Auxiliary winding	Start at Pin 4. Wind 30 turns of $\varnothing 0.14\text{mm}$ wire [3] from left to right. Wind tightly & spread evenly in the middle.
Insulation	1 Layers of insulation tape [5], 0.05mm thick, 7.0mm wide.
WD 2 Primary Winding	Start at Pin 2. Wind 40 turns of $\varnothing 0.14\text{mm}$ wire [3] from left to right. Wind the next 40 turns on the next layer from right to left. Wind the next 40 turns from left to right Wind the last 10 turns from right to left on the side of primary. Finish on Pin 1. Wind tightly & spread evenly.
Insulation	1 Layer of insulation tape [5], 0.05mm thick, 7.0mm wide.

Shield	Copper shield [7], 6.5mm wide, 31mm long. Connected to Pin 1 on the side of primary.
Insulation	3 Layers of insulation tape [5], 0.05mm thick, 7.0mm wide.
Margin tape	Wind 2mm margin tape [6] on the secondary side.
WD 3 Secondary winding	Start at Pin 5. Wind 8 turns of $\varnothing 0.35\text{mm}$ Triple Insulated Wire [5] from right to left (to the opposite direction). Wind the last 8 turns from left to right. Terminate on Pin 8. Wind tightly & spread evenly.
Insulation	1 Layers of insulation tape [5], 0.05mm thick, 7.0mm wide.
Glue	Glue core and bobbin

6. PCB layout

The PCB layout rules are highlighted as follow:

1. The loop area composed by the input capacitor, the primary winding of the transformer, power transistor Q1 and current sense resistor R10 should be minimized for better EMI performance
2. The power ground and signal ground should be connected by one node.

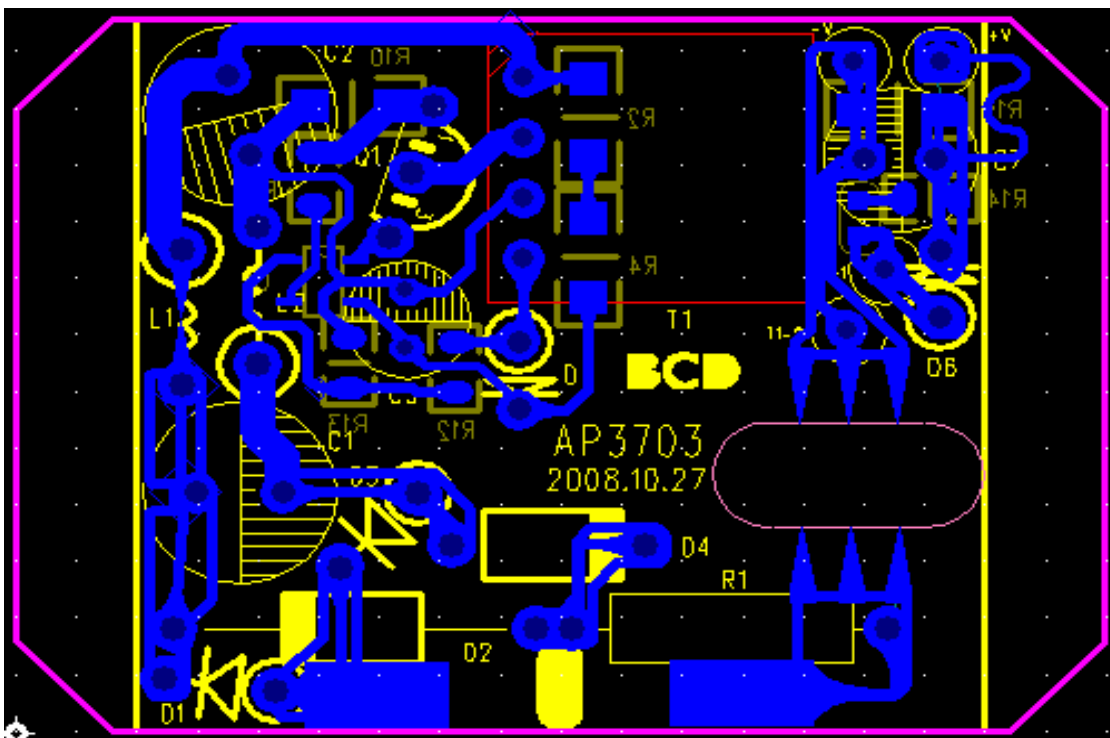


Figure 5. Printed circuit layout

7. Electrical performance

All the test results were obtained at room temperature unless otherwise specified, with 50 Hz line voltage and 1.8m AWG26 cable.

7.1. Active mode efficiency

The charger system passes active mode average efficiency criteria of Energy Star EPS 2.0 final version. The active efficiency criteria follow the formula for low voltage mode and can be calculated as 63.7%.

Table 2. Average active mode efficiency

% of Full Load	Efficiency (%)	
	115Vac	230Vac
25	73.1%	67.4%
50	73.7%	69.2%
75	72.9%	68.9%
100	72%	68.9%
Average	72.9%	68.6%
Energy Star EPS 2.0: 63.7%		

7.2. Output I-V and regulation

All the measurements were obtained in the following conditions:

1. The power supply was assembled closely into a cellphone charger case.
2. The power supply with the case was placed into a carton, which was put into a full temperature chamber. The temperature inside the carton was monitored to keep a constant ambient temperature without the airflow for the testing.
3. The readings of output voltage and current were recorded only after the power supply had worked for 30 minutes under no load condition.

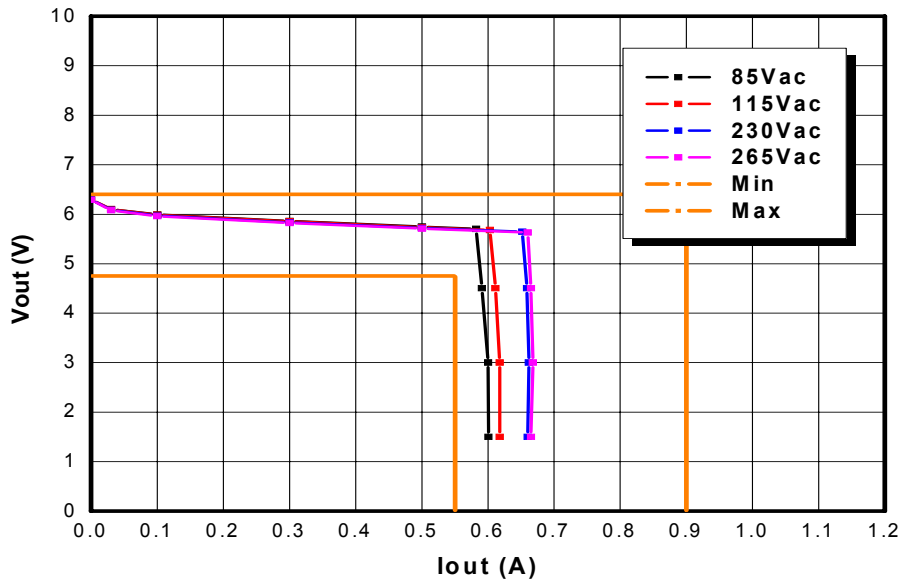


Figure 6. Typical CV/CC Characteristic @25°C

7.3. No load input power

The readings of input power were recorded only after the power supply had worked for 5 minutes under no load condition.

Table 3. No Load Input Power

Input Voltage (V)	Input Power(mW)	Less than 100mW @230Vac
85	38	
115	46.2	
145	57	
180	71	
230	99	
264	125	

8. Key Operating Waveforms

8.1. Output ripple voltage

All measurements were made with an oscilloscope with 20 MHz bandwidth and the output was bypassed at the connector with a 0.1 μF ceramic disk capacitor and a 10 μF electrolytic capacitor.

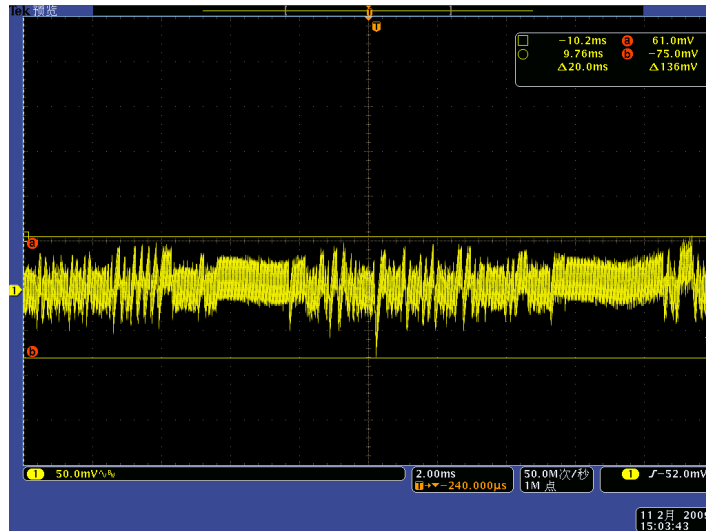


Figure 7. Ripple, Worse case@85Vac, 2ms, 50mV/div, peak-peak: 136mV

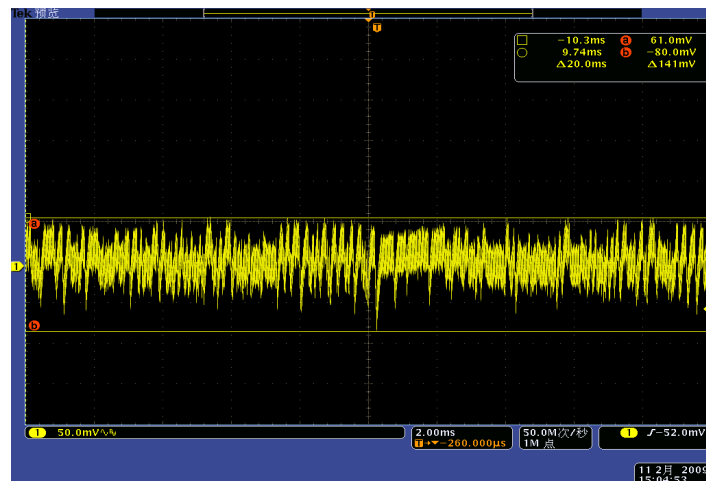


Figure 8. Ripple, Worse case@115Vac, 2ms, 50mV/div, peak-peak: 141mV

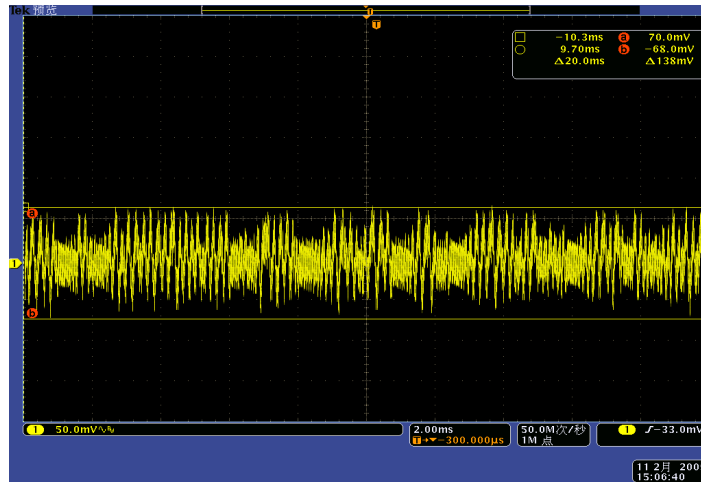


Figure 9. Ripple, Worse case@230Vac, 2ms, 50mV/div, peak-peak: 138mV

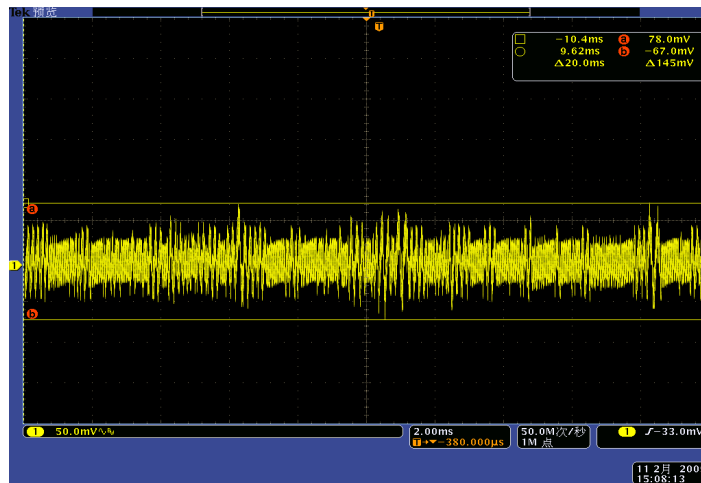


Figure 10. Ripple, Worse case@264Vac, 2ms, 50mV/div, peak-peak: 145mV

8.2. Collector voltage of power transistor

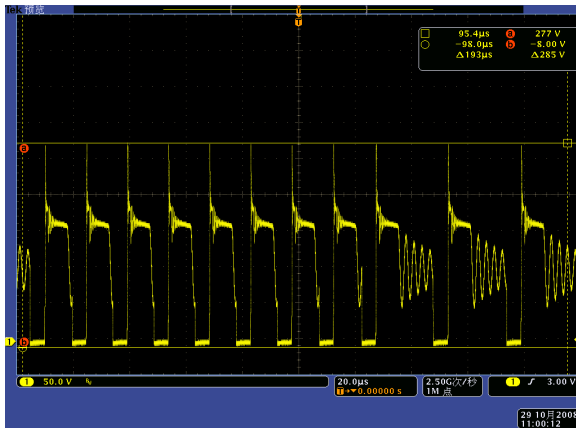


Figure 11. Collector voltage, 85Vac, Full Load, 50V, 20us/div, peak voltage: 285Vdc

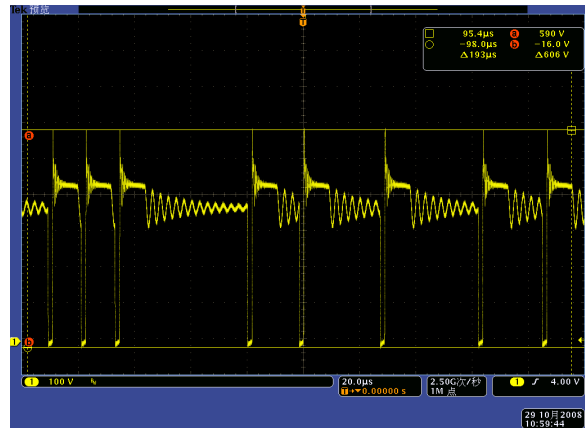


Figure 12. Collector voltage 264Vac, Full Load, 100V, 20us/div, peak voltage: 602Vdc

8.3. Startup characteristics



Figure 13. Rise time, 115Vac, Full Load, 1V, 4ms/div

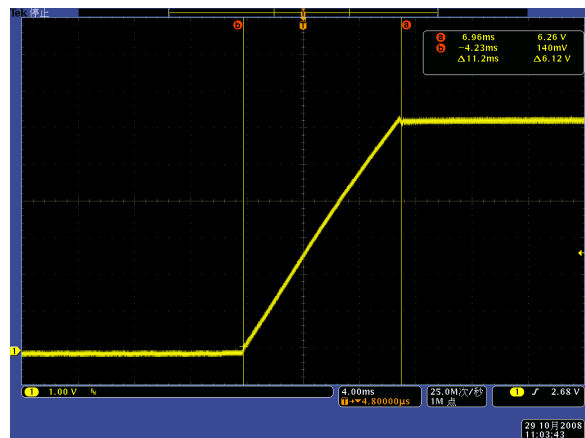
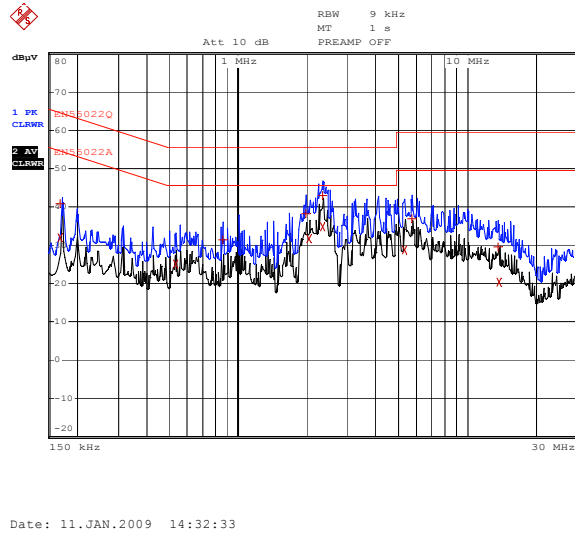


Figure 14. Rise time, 230Vac, Full Load, 1V, 4ms/div

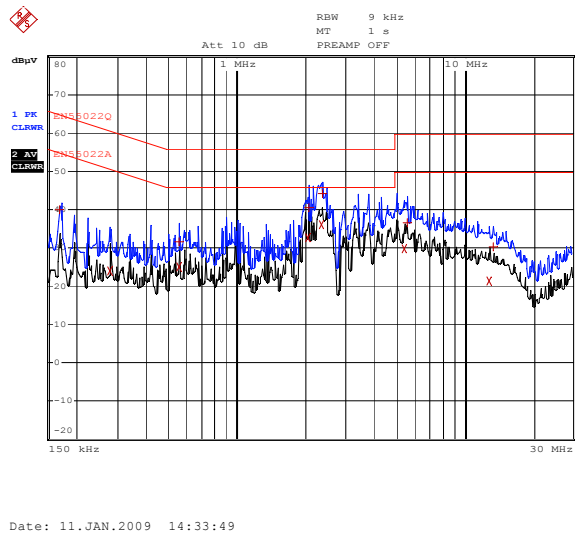
9. EMI test results

9.1. Conducted EMI



EDIT PEAK LIST (Final Measurement Results)			
TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
Trace1: EN55022Q			
Trace2: EN55022A			
Trace3: ---			
1	Quasi Peak 170 kHz	41.20	-23.76
2	Average 170 kHz	32.29	-22.66
2	Average 534 kHz	25.45	-20.54
1	Quasi Peak 870 kHz	31.70	-24.29
1	Quasi Peak 2.014 MHz	38.67	-17.32
2	Average 2.062 MHz	32.05	-13.94
1	Quasi Peak 2.382 MHz	43.27	-12.72
2	Average 2.382 MHz	35.31	-10.68
2	Average 5.426 MHz	29.20	-20.79
1	Quasi Peak 5.886 MHz	37.47	-22.52
1	Quasi Peak 13.97 MHz	30.05	-29.94
2	Average 14.082 MHz	20.88	-29.12

Figure 15. Conducted EMI, 230VAC/50Hz, full load, Neutral

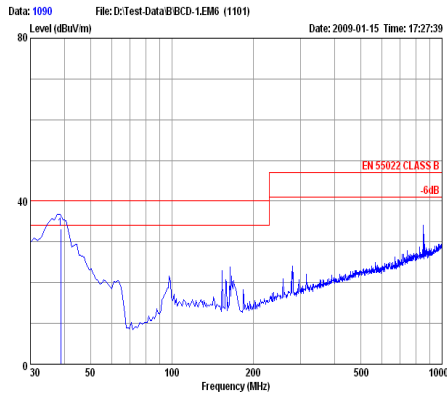


EDIT PEAK LIST (Final Measurement Results)			
TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
Trace1: EN55022Q			
Trace2: EN55022A			
Trace3: ---			
1	Quasi Peak 170 kHz	40.19	-24.76
2	Average 278 kHz	24.33	-26.54
1	Quasi Peak 562 kHz	31.96	-24.03
2	Average 562 kHz	25.19	-20.80
2	Average 2.062 MHz	32.75	-13.24
1	Quasi Peak 2.086 MHz	40.76	-15.23
2	Average 2.382 MHz	36.29	-9.70
1	Quasi Peak 2.406 MHz	44.32	-11.67
2	Average 5.494 MHz	30.04	-19.96
1	Quasi Peak 5.658 MHz	36.81	-23.18
2	Average 12.958 MHz	21.61	-28.39
1	Quasi Peak 13.482 MHz	30.42	-29.57

Figure 16. Conducted EMI, 230VAC/50Hz, full load, Line

9.2. Radiated EMI

AUDIX[®]
 Audix Technology (Shanghai) Co., Ltd.
 3F #34Bldg No.660 GuiPing Rd.,
 Caohejing Hi-Tech Park,
 Shanghai 200233, China
 Tel: +86-21-64955500 Fax: +86-21-64955491
 audixaci@audix.com



Data: 1090 File: D:\Test-Data\BBCD-LEM6 (1101) Date: 2009-01-15 Time: 17:27:39

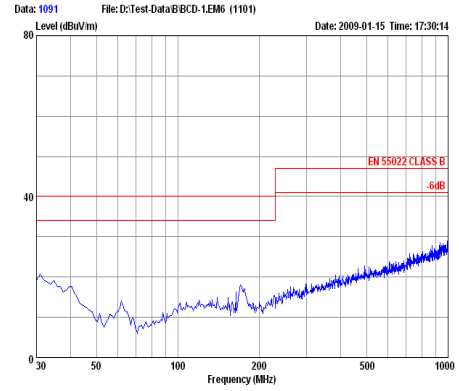
Site no : Audix ACI (3a Chamber) Data no : 1090
 Dis / Ant : 3a / CBL 6112D-2008 05 14
 Limit : EN 55022 CLASS B Ant pol : VERTICAL
 Env / Ins : 28 °C / ESVS10 Engineer : Jacky
 EUT :
 N/N : 3703
 S/N : 550mA
 Power Rating: 230V/50Hz
 Test Mode :

Freq (MHz)	Antenna Factor (dB/m)	Cable Loss (dB)	Reading (dBuV)	Emission Level (dBuV/m)	Limits (dBuV/m)	Margin (dB)
1 38.895	14.53	0.67	17.90	33.10	40.00	6.90

Remarks: 1 Emission Level= Antenna Factor + Cable Loss + Reading
 2 The emission levels that are 20dB below the official are not report.

Figure 17. Radiated EMI, 230VAC/50Hz, full load, Vertical

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Data: 1091 File: D:\Test-Data\BBCD-LEM6 (1101) Date: 2009-01-15 Time: 17:30:14

Site no : Audix ACI (3a Chamber) Data no : 1091
 Dis / Ant : 3a / CBL 6112D-2008 05 14
 Limit : EN 55022 CLASS B Ant pol : HORIZONTAL
 Env / Ins : 28 °C / ESVS10 Engineer : Jacky
 EUT :
 N/N : 3703
 S/N : 550mA
 Power Rating: 230V/50Hz
 Test Mode :

Figure 18. Radiated EMI, 230VAC/50Hz, full load, Horizontal

10. Summary of test results

Description	Min	Typ	Max	Units	Tested results
Input					
Voltage	85		264	VAC	
Frequency	47	50/60	63	Hz	
No Load Input Power			200	mW	<100mW@230Vac
Output					
Output Voltage	4.75		6.5	V	Pass
Output Ripple Voltage			150	mVpp	Pass
Output Current	300	550	950	mA	Pass
Output Power (Pno)		2.75		W	Pass
Efficiency					
Average Efficiency at 25,50,75 and 100 % of Pno (EPS 2.0) ---note 1	63.7			%	>72.9 at 115Vac; >68.6 at 230Vac (26# cable)
EMI	Pass EN55022 Class B with 6dB margin				Pass

11. Revision history

Versions	Date	Author	Description for changes	Reviewed
Version 1.0	01/19/2009	Sun Jian	Initial release	Charles Sun