Topic 3

Designing an LLC Resonant Half-Bridge Power Converter

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Agenda

1. Introduction
   – Brief review
   – Advantages

2. Design Prerequisites
   – Configuration
   – Operation
   – Modeling
   – Voltage gain function

3. Design Considerations
   – Voltage gain and switching frequency
   – Line and load regulation
   – Zero voltage switching (ZVS)
   – Steps for designing and a design example

4. Conclusions
Introduction

• Brief review of resonant converters
  – Series resonant converter (SRC)
  – Parallel resonant converter (PRC)

• Single resonant frequency
• Circuit frequency increases with lighter load

• Resonant point changes with load
• Large amount of circulating current
Introduction

• Brief review of resonant converters
  – Combination of SRC and PRC → LCC
    • Two resonant frequencies
    • Requires three elements
  – LLC: alternative LCC
    • $L_r$ and $L_m$ integrated in a transformer

• Advantages of LLC
  – High efficiency (ZVS)
  – Less frequency variation and lower circulating current
  – ZVS over operating range
**Design Prerequisites**

- **Configuration**
  - Variable-frequency square-wave generator
  - Divider formed by resonant network and $R_L$
  - Rectifier to get DC output
  - Changing frequency varies voltage across $R_L$
  - Frequency-modulated converter instead of PWM
Design Prerequisites

- Operation
  - $f_{sw}$ switching frequency
  - $f_0$ series resonant frequency ($C_r$ and $L_r$)
  - $f_{co}$ circuit resonant frequency ($C_r$, $L_r$, and $L_m$, together $R_L$)

\[
\begin{align*}
&f_{sw} = f_0 \\
&f_{sw} < f_0 \\
&f_{sw} > f_0
\end{align*}
\]
Design Prerequisites

• Modeling
  – First harmonic approximation (FHA)

\[ \begin{align*}
\text{Input and output: Square wave voltages} \\
\text{Sinusoidal current in resonant circuit}
\end{align*} \]

\[ \begin{align*}
\text{Input and output: Fundamental components to approximate FHA} \\
\text{Rectifier and } R_L \text{ equivalent to } R_e \\
\text{AC circuit method can be used}
\end{align*} \]
Design Prerequisites

- Voltage gain function
  - Expression from impedance divider

\[
M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} \approx M_{g\_sw} = \frac{V_{so}}{V_{sq}} \approx M_{g\_ac} = \frac{V_{oe}}{V_{ge}}
\]

\[
M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} \approx \frac{V_{oe}}{V_{ge}}
\]

\[
= \frac{(j\omega L_m) || R_e}{(j\omega L_m) || R_e + j\omega L + \frac{1}{j\omega C_r}}
\]

where \( \omega = 2\pi f = 2\pi f_{sw} \) and \( j = \sqrt{-1} \)
Design Prerequisites

- Voltage gain function
  - Expression (Normalization)

\[ M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} \approx M_{g\_sw} = \frac{V_{so}}{V_{sq}} \approx M_{g\_ac} = \frac{V_{oe}}{V_{ge}} \]

\[ M_g = \frac{L_n \times f_n^2}{[(L_n + 1) \times f_n^2 - 1] + j[(f_n^2 - 1) \times f_n \times Q_e \times L_n]} \]

<table>
<thead>
<tr>
<th>Normalized Gain</th>
<th>Resonant Frequency</th>
<th>Quality Factor</th>
<th>Normalized Frequency</th>
<th>Inductor Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M_g = \frac{V_o}{V_{in}/2} )</td>
<td>( f_0 = \frac{1}{2\pi \sqrt{L_r C_r}} )</td>
<td>( Q_e = \frac{\sqrt{L_r/C_r}}{R_e} )</td>
<td>( f_n = \frac{f_{sw}}{f_0} )</td>
<td>( L_n = \frac{L_m}{L_r} )</td>
</tr>
</tbody>
</table>

Eq. Load R.

\[ R_e = \frac{8 \times n^2}{\pi^2} \times R_L \]
Design Prerequisites

- Voltage gain function
  - Plots of gain magnitude, fixed $L_n = 5$
  - $Q_e$ (load current) increases $\Rightarrow$ peak gain decreases $\Rightarrow$ curves shrink

![Graph showing voltage gain function with different $Q_e$ values.](image-url)
Design Prerequisites

- Voltage gain function
  - Plots of gain magnitude, fixed $Q_e = 0.5$
  - $L_n$ decreases $\Rightarrow$ peak gain increases $\Rightarrow$ ZVS obtained but conduction losses increase

![Graph showing gain vs. normalized frequency for different $L_n$ values.](image)

- For $L_n = 3$, $5$, $10$, the gain decreases as the normalized frequency increases.
Design Considerations

• Where to base a design?
  – In the vicinity of series resonance, \( f_n = 1 \Rightarrow \) narrowest frequency variation
    \( \Rightarrow M_g \text{ able to } = 1, >1, \text{ and } <1 \)
  – Right side of the resonant peak \( \Rightarrow \) ZVS requirement
Design Considerations

• Line and load regulation
  – Properly set up $M_{g_{\text{max}}}$ and $M_{g_{\text{min}}}$
  – Frequency limit set up

\[
M_{g_{\text{max}}} = \frac{n \times V_{o_{\text{max}}}}{V_{\text{in}_{\text{min}}}/2}
\]

\[
M_{g_{\text{min}}} = \frac{n \times V_{o_{\text{min}}}}{V_{\text{in}_{\text{max}}}/2}
\]
Design Considerations

• Overload current operation
  – $Q_e = \text{max}$ to include and meet the required $M_{g_{\text{max}}}$
  – Operation still on the right side of resonant peak

![Diagram showing normalized frequency and gain with overload current operation considerations.](image-url)
Design Considerations

• Load short circuit
• Protection options
  – Increase $f_{sw}$ rapidly to reduce $M_g$ to zero
  – Operation with $f_n > 1$, i.e., $f_{sw} > f_0$ at all times
  – Independent protection function
Design Considerations

• Zero voltage switching (ZVS)
  – How ZVS is achieved?
Design Considerations

• Zero voltage switching (ZVS)
  
  – **Necessary** condition
    
    • Input impedance of the resonant network → **inductive**
    
    • Operation on the right side of the resonant peak
  
  – **Sufficient** condition
    
    • Enough energy stored in the magnetic field, mainly $L_m$
    
    • Enough time to discharge the capacitors, mainly $C_{DS}$
Design Considerations

• Why not design on the left side of the resonant peak?
  – Capacitive current results
  – ZVS lost
    → Hard switching
    → Switching losses increase
  – Body diode reverse recovery losses
    → Primary MOSFET failure
  – Higher EMI noise
  – Reversed frequency relationship to feedback loop
Design Considerations

- Design Steps – How to initially select?
  - $f_{sw}$, switching frequency
  - $n$, transformer turns ratio
  - $L_n$, inductance ratio
  - $Q_e$, series resonant quality factor
Design Considerations

• Design Steps – Switching frequency
  – Usually selected for particular applications
    • Example in off-line applications: Typical below 150 kHz
  – Selecting the switching frequency
    • f decrease ⇒ Bulkier converter
    • f decrease ⇒ Switching losses decrease ⇒ ZVS benefit decrease
    • f increase ⇒ ZVS benefits increase vs. hard switching converters
  • Very High f:
    – Component availability
    – Additional switching losses
    – Additional concerns due to parasitic effects
Design Considerations

• Design Steps – Transformer turns ratio, \( n \)
  
  – Voltage gain can be larger and smaller than unity

  – Flexibility in selecting the turns ratio, \( n \)

  – Turns ratio design with \( M_g = 1 \), initially, and nominal \( V_{in} \) and \( V_o \)

\[
n = M_g \times \frac{V_{in}/2}{V_o} = \frac{V_{in\_nom}/2}{V_{o\_nom}} \quad | \quad M_g = 1
\]
Design Considerations

- **Design Steps – \( L_n \) and \( Q_e \)**
  - \( L_n \) and \( Q_e \) to achieve \( M_{g_{pk}} > M_{g_{max}} \) for maximum load
  - Select \( L_n \) and \( Q_e \) from pre-plotted peak gain curves
  - Initial selection
    - \( L_n = 5 \)
    - \( Q_e = 0.5 \)
  - Example: Select \( L_n \) and \( Q_e \) for \( M_{g_{max}} = 1.2 \)
  - To achieve design margin – Final selection
    - \( L_n = 3.5, Q_e = 0.45 \)
    - 30% margin over
Design Considerations

- Design Steps – Trade-offs to select $L_n$ and $Q_e$
  - Different requirements for different applications
  - Fixed $Q_e$, $L_n$ decrease $\Rightarrow$ peak gain increase $\Rightarrow$ good for ZVS and avoids capacitive current
  - But, $L_n$ decrease $\Rightarrow$ $L_m$ decrease $\Rightarrow$ conduction losses increase
  - Fixed $L_n$, $Q_e$ decrease $\Rightarrow$ peak gain increase $\Rightarrow$ frequency variation increase
  - Recommend starting with $L_n = 5$, and $Q_e = 0.5$ (from design practice)
Design Considerations

• Resonant circuit design flow

Converter Specifications

\[ n = \frac{V_{\text{in}}}{2V_0} \]

Magnetizing Inductance

\[ L_m = L_n \times L_r \]

\[ L_r = \frac{1}{(2\pi f_{\text{sw}})^2 \times C_r} \]

Resonant Inductor

\[ M_g_{\text{max}} = \frac{n \times V_{0_{\text{max}}}}{V_{\text{in max}} / 2} \]

\[ M_g_{\text{min}} = \frac{n \times V_{0_{\text{min}}}}{V_{\text{in min}} / 2} \]

Resonant Capacitor

\[ C_r = \frac{1}{2\pi f_{\text{sw}} \times R_e \times Q_e} \]

Choose \( L_n \) and \( Q_e \)

Calculate \( R_e \)

\[ R_e = \frac{8 \times n^2}{\pi^2} \times R_L = \frac{8 \times n^2}{\pi^2} \times \frac{V_0^2}{P_{\text{out}}} \]

Are Values Within Limits?

\[ M_g_{\text{max}} \quad M_g_{\text{min}} \]

\[ f_{n_{\text{max}}} \quad f_{n_{\text{min}}} \]

\[ Q_e = 0.52 \quad f_{n_{\text{max}}} = 1.02 \]

\[ Q_e = 0.47 \quad f_{n_{\text{min}}} = 0.65 \]

\[ Q_e = 0.45 \quad M_g_{\text{max}} = 1.3 \]

\[ Q_e = 0.5 \quad M_g_{\text{min}} = 0.99 \]

\[ f_{n_{\text{min}}} = 0.65 \]

\[ L_n = 3.5 \]

\[ L_n = 3.0 \]

\[ L_n = 2.5 \]

\[ L_n = 2.0 \]

\[ L_n = 1.5 \]

\[ L_n = 1.0 \]

\[ L_n = 0.5 \]

\[ L_n = 0.0 \]

\[ Q_e = 0 \]

\[ f_{n_{\text{min}}} = 0.65 \]

\[ L_n = 3.5 \] by interpolation

\[ M_g_{\text{ap}} = 1.56 \]

\[ Q_e = 0.45 \]

\[ L_n = 3.0 \]

\[ L_n = 2.5 \]

\[ L_n = 2.0 \]

\[ L_n = 1.5 \]

\[ L_n = 1.0 \]

\[ L_n = 0.5 \]

\[ L_n = 0.0 \]
Design Considerations

• Design example

  – Specifications

    • Rated output power: 300 W
    • Input voltage: 375 to 405 VDC
    • Output voltage: 12 VDC
    • Rated output current: 25 A
    • Efficiency \( (V_{\text{in}} = 390 \text{ VDC and } I_{\text{o}} = 25 \text{ A}) \): >90%
    • Switching frequency: 70 kHz to 150 kHz
    • Topology: LLC resonant half-bridge converter
Design Considerations

• Design example
  – Proposed converter circuit block diagram
Design Considerations

• Design example – UCC25600 Features
  - 8-pin SOIC package
  - Programmable:
    • dead time
    • \( f_{\text{min}} \) and \( f_{\text{max}} \)
    • soft start time
  - Protection
    • OCP: hiccup and latch-off
    • VCC UVLO and OVP
    • OTP
  - Burst operation
Design Considerations

- Resonant circuit design flow

Converter Specifications

\[ n = \frac{V_{in}}{2V_o} \]

Magnetizing Inductance

\[ L_m = L_n \times L_t \]

Resonant Inductor

\[ L_t = \frac{1}{(2\pi f_{sw})^2 \times C_r} \]

Resonant Capacitor

\[ C_r = \frac{1}{2\pi f_{sw} \times R_c \times Q_c} \]

Choose \( L_n \) and \( Q_e \)

Check \( M_g \) and \( f_n \) Against Graph

Are Values Within Limits?

\[ M_{g_{max}} \]
\[ f_{n_{max}} = 1.02 \]
\[ M_{g_{min}} = 0.99 \]
\[ f_{n_{min}} = 0.65 \]

Gain, \( M_g \)

\[ Q_e = 0 \]
\[ f_{n_{max}} = 0.65 \]
\[ M_{g_{max}} = 1.3 \]
\[ Q_e = 0.52 \]
\[ f_{n_{max}} = 1.02 \]

\( L_n \) = 3.5
\( Q_e = 0.45 \)

\( n = 16 \)

\( L_m = 210 \) \( \mu \)H

\( L_t = 60 \) \( \mu \)H

\( C_r = 27.3 \) nF

\( \frac{8 \times n^2 \times V_o^2}{\pi^2} \times R_c \times Q_c \)

\( \frac{8 \times n^2 \times V_o^2}{\pi^2 \times P_{out}} \)

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Design Considerations

- Design check

![Graph showing normalized frequency and gain values with specific points marked for different frequencies and gains.]

- $L_n = 3.5$
- $Q_e = 0$
- $Q_e = 0.47$
- $Q_e = 0.52$
- $M_{g_{\text{max}}} = 1.3$
- $M_{g_{\text{min}}} = 0.99$
- $f_{n_{\text{min}}} = 0.65$ (80.9 kHz)
- $f_{n_{\text{max}}} = 1.02$ (126.9 kHz)
- $f_{n_{\text{max}}} = 1.02$ (126.9 kHz)
- 70 kHz
- 150 kHz
Design Considerations

• Design check
  – Verification with computer-based circuit simulation
  – Design reiteration, if needed
  – Size/select components
  – Build the board
  – Verification with bench tests
  – Re-spin the board/design, if needed
Design Considerations

• Experiment results (L_m = 280 µH, L_r = 60 µH, C_r = 24 nF)
Test Result versus FHA from the Design

- In the vicinity of $f_0$, FHA-based result very accurate to the final test result ($L_r = 60 \mu H$ and $C_r = 24 \text{nF}$)

- Away from $f_0$, less accuracy from FHA-based result

- Equation (18)

\[
M_g = \frac{V_{oc}}{V_{ge}} = \frac{jX_{L_m} \parallel R_e}{(jX_{L_m} \parallel R_e) + j(X_L - X_C)} = \frac{(j\omega L_m) \parallel R_e}{(j\omega L_m) \parallel R_e + j\omega L_r + \frac{1}{j\omega C_r}}
\]
Conclusions

• FHA-based method approximately, while effectively, converted complicated LLC resonant-converter circuit to standard AC circuit – greatly simplified its analysis and design

• Method results effective for LLC converter design, especially for initial parameters determination

• Design example with comprehensive design considerations in procedural design steps demonstrating method effectiveness

• Possibility of FHA-based approach for other resonant converters